Effect of Pt thickness on the gate sinking in a pHEMT device

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The standard gate metal stack in the GaAs integrated circuit (IC) processes is Ti/Pt/Au/Ti from bottom to top. Starting from the bottom, the first metal layer of the gate stack is Ti to ensure good adhesion at the semiconductor surface. Next, the Pt layer is used as a barrier to stop Au diffusion through the bottom Ti layer and into the semiconductor. In a delta gate structure, Au can deposit on the side walls of the gate stack during metal deposition. This unwanted Au can also diffuse into the semiconductor in the subsequent processes and severely impacts the device performance and reliability [1]. In order to reduce the gate sinking, the device characteristics with varying Pt barrier thicknesses are studied.

Three groups of pHEMT devices with delta gates (0.5 µm) are manufactured using the standard double recess GaAs integrated circuit process flow. The gate metals are deposited on an InGaP etch stop layer after the gate recess. In the first group of wafers, the Pt thickness is about 200Å. In the second and third groups of wafers, the Pt thicknesses are about 500 and 1000Å, respectively. All wafers are processed together before and after the gate metal deposition to keep other processing conditions consistent. After finishing all process steps a Keithly production test stand is used to test the standard 200 µm FETs.

The pinch off voltages (Vp) are measured at 2.5% of Idss of the devices and are shown in figure 1. All the wafers with different Pt thicknesses show median pinch off voltages around -1.1V. The devices with 200 Å of Pt show a slightly higher Vb2 (~ 20 V) measured at 1 mA/mm compared to the other devices. The devices with 500 and 1000 Å of Pt show similar Vb2 of around 17 - 18V. The on resistances measured at the drain source linear zone at a gate bias of about 0V are about 1.25 Ohms mm for all the devices, which indicates that the different Pt thicknesses in the gate metal stack do not change the device characteristics [2].

One wafer from each group is annealed at 300°C for 10, 20 and 30 minutes to study the gate sinking. The wafers are tested after each anneal to record the change of the critical FET parameters. The change in the pinch-off voltage (delta Vp) and the on resistance (delta Ron) is the difference between the prior anneal Vp/Ron values and the post anneal Vp/Ron values. These are calculated after each anneal of 10, 20 and 30 minutes.

Figure 2 (a) shows the box plot of delta Vp for the wafers with different Pt thicknesses in the gate metal stack. The positive shift indicates that the Vp is lower (less negative) after each anneal. The Vp for the 1000 Å Pt devices shifts about 45 mV which is much greater compared to the shifts for the 200 and 500 Å Pt devices. The shift for 200 and 500 Å of Pt is negligible. As the annealing time increases, the values of delta Vp also increase for all of the devices. A bigger increase is observed in the devices with 1000Å of Pt.

The box plots of delta Ron and gate drain leakage current measured at -7 V are shown in figures 2 (b) and (c). The delta Ron exactly follows the trend of the delta Vp. The bigger shift in Vp and the increase in Ron are likely due to the diffusion of gold into the semiconductor during each anneal. Therefore, the gate metal (gold)/semiconductor interface moves closer to the channel with the increase of annealing time which means the gate requires less voltage to turn off the channel. The diffusion of gold into the semiconductor during thermal annealing is also responsible for the increase of the leakage current [3].

In order to confirm the Pt thickness and gold diffusion in the semiconductor, focussed ion beam induced (FIB) scanning electron micrographs are taken from the devices with different Pt thicknesses. Figure 3 shows the cross-sections of the gates before and after the annealing of the devices. The picture clearly shows the different Pt thicknesses (200, 500 and 1000Å) in the gate metal stack. The diffused gold is also visible at the edge of the gates of the devices after annealing. More gold diffusion is seen in the devices with 1000Å of Pt. This observation agrees very well with the bigger shift of Vp and Ron in the devices with 1000 Å of Pt. The EDS mapping is also used to confirm the gold diffusion.

The higher shift of all the critical FET parameters in the wafer with 1000Å of Pt could be due to the high stress during Pt deposition, which pulls the resist and increases the aperture of the photoresist opening. The increase in the opening enhances the probability of Au deposition on the side walls of the stack. This also increases the possibility of the Au touching the semiconductor surface which, in turn, can increase the leakage current and contribute to gate

sinking (more shift in Vp and Ron). The lower Pt thickness reduces the possibility of gate sinking due to lower stress during deposition.

[1] C. Canali, G. Donzelli, F. Fantini, M. Vanzi, and A. Paccagnella, "Goldbased gate-sinking enhanced by inhomogeneities in power MESFETs," *Electron. Lett.*, vol. 23, pp. 83–84, 1987.

[2] L. Luu-Henderson, L. Rushing and S. Tiku, "Reduction of Platinum Metal Usage in GaAs IC Metallization" CS MANTECH Conference, Vancouver, British Columbia, Canada, pp. 137 – 140, April 24-27, 2006

[3] James Oerth, Christopher Doucette, Sushila Singh, Sean Doonan, "Yield Improvement Methodology in a pHEMT GaAs Fabrication Facility" CS MANTECH Conference, Chicago, Illinois, USA April 14-17, 2008.

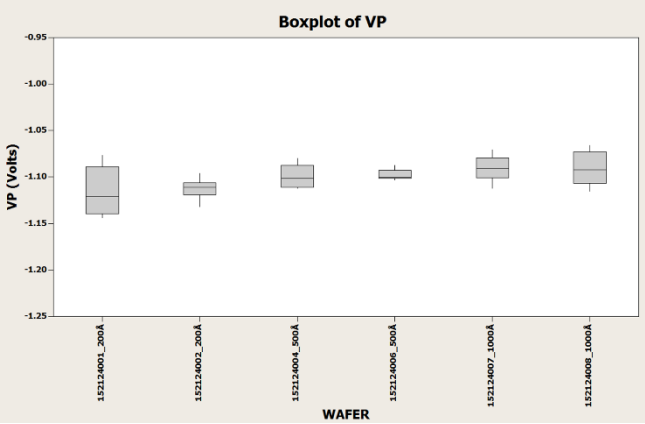

Fig. 1. Pinch off voltages measured at 2.5 % of Idss of the devices

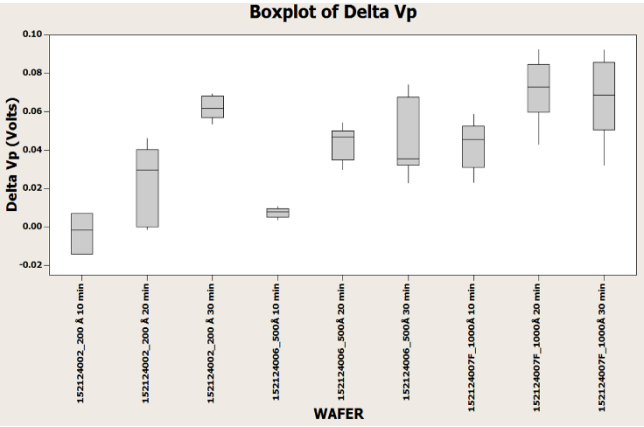

Fig. 2(a). Box plot of delta Vp for varying Pt thicknesses

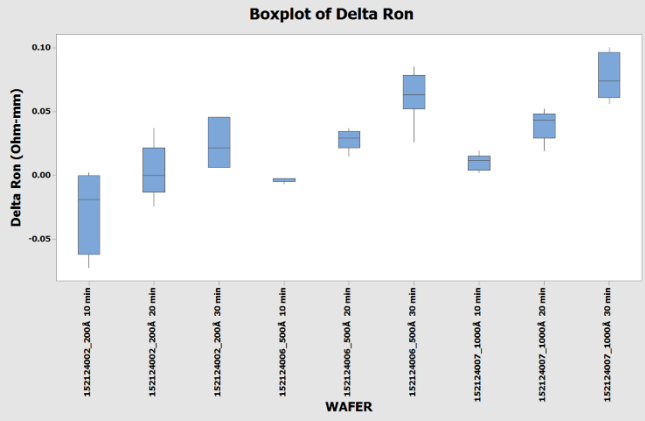

Fig. 2(b). Box plot of delta Ron for varying Pt thicknesses

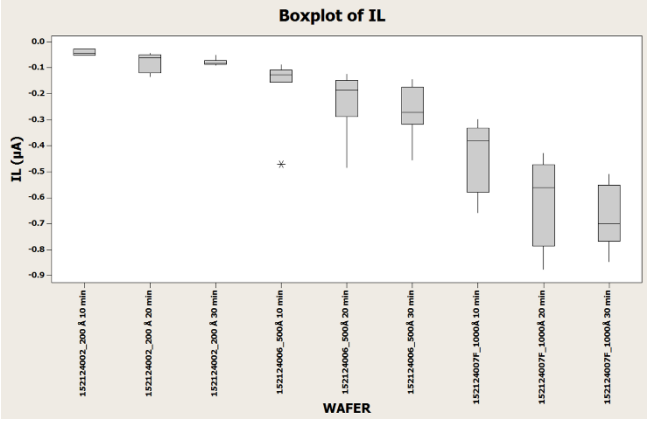

Fig. 2(c). Box plot of the gate drain leakage current measured at -7 V

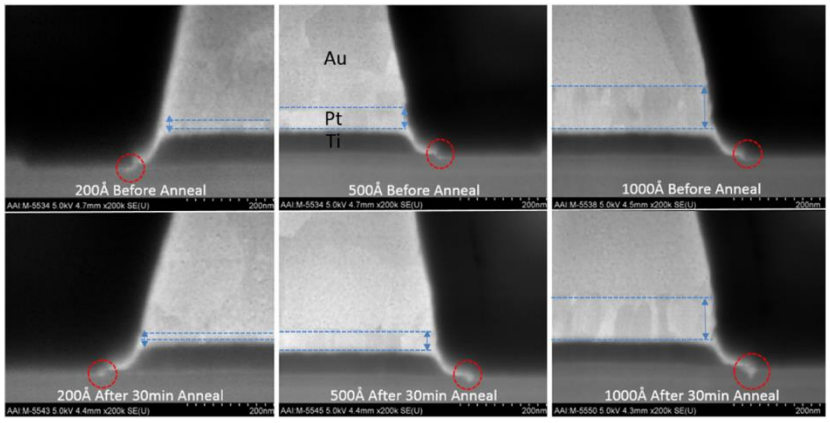

Fig. 3. FIB cross-sections of the gates before and after the annealing of the devices