Improved Thermal Stabilities in Normally-off GaN MIS-HEMTs

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GaN based power transistors, with the merit of operating at elevated junction/ambient temperature and high switching frequency, are suitable for high-performance compact power converters. For the GaN transistors with metal–insulator–semiconductor (MIS) structure, their high temperature stability can be hindered by the challenges of V_{TH} instability originating from the thermal electron emission of trap states at the dielectric/III-N interface [1,2]. To address this issue, a thinned barrier layer is proposed to bring the deep interface traps below the Fermi level at pinch-off so that they become inactive [2]. In this work, the normally-off MIS-HEMTs featuring a partially recessed (Al)GaN barrier were realized by a fluorine-plasma implantation/etch technique. The partially recessed barrier leads to improved thermal stability, while the fluorine implantation can convert the device from D-mode to E-mode without completely removing the barrier and sacrificing the high mobility heterojunction channel [3].

The schematic cross-section of the normally-off MIS-HEMT is shown in Fig. 1. Both the fluorine ion implantation and gate recess were carried out using CF_4 plasma. By properly adjusting the power level of the RF source driving the fluorine plasma, we are able to obtain two desirable results: 1) a well-controlled slow dry etching for gate recess; and 2) effective shallow implantation of fluorine ions into the AlGaN barrier. Fluorine plasma implantation at a higher RF power level of 200 W resulted in a well-controlled slow etching process with an etching rate of 2-nm/min. Meanwhile, a lower RF power of 150 W only induced insignificant etching of the barrier layer [4]. After 6 minutes of F-implantation/etch, a recess depth of ~12 nm and a smooth etched surface were obtained. After removing another 2-nm AlGaN by a digital etching [5], 20-nm Al_2O_3 was deposited by ALD with an in-situ nitridation process [6].

The proposed MIS-HEMT exhibits a threshold voltage (V_{TH}) of +0.6 V at a drain current of 10 μA/mm, a maximum drive current of 730 mA/mm, an on-resistance of 7.07 Ω·mm (Fig. 2), and a hysteresis of ~0.3 V between the up- and down- V_{GS}-sweep with a relatively fast sweeping rate (0.7 V/s). Three-terminal off-state breakdown measurement of a MIS-HEMT with L_{GD} = 15 μm yields a breakdown voltage of 703 V at a drain leakage of 1 μA/mm with the substrate grounded (Fig. 3(a)).

Fig. 3(b) shows the temperature (T)-dependent transfer characteristics of a MIS-HEMT. When temperature increases from 25 ^{o}C to 200 ^{o}C, an increase of 3 orders of magnitude is observed in the OFF-state drain leakage due to increased buffer leakage, while the drain current exhibits an decrease (e.g. from 240 mA/mm to 200 mA/mm at V_{GS} = 4 V). By using a current criteria of I_{DS} of 10 μA/mm, V_{TH} shifted by 0.5 V negatively.

The dynamic properties of fabricated MIS-HEMTs were evaluated by high-drain-bias transient switching test and on-wafer hard switching measurement performing at temperature ranging from 25 ^{o}C to 200 ^{o}C (Fig. 4). A dynamic R_{ON} degradation (×1.58) for an OFF-state drain bias stress of 600 V (Fig. 5(a)) indicates effective suppression of current collapse for the room-temperature operation of proposed MIS-HEMTs. At elevated temperatures, the degradation of dynamic R_{ON} for V_{DS} stress up to 200 V is suppressed (Fig. 5(b)). During the hard switching test under high-frequency and high-temperature conditions (Fig. 5(c)), the increase of dynamic R_{ON} is less than 18% and shown negligible temperature dependence.

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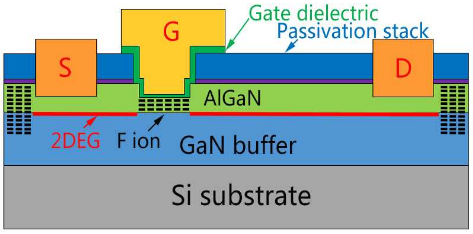

Fig. 1: Cross-sectional schematic of a fabricated E-mode MIS-HEMT.

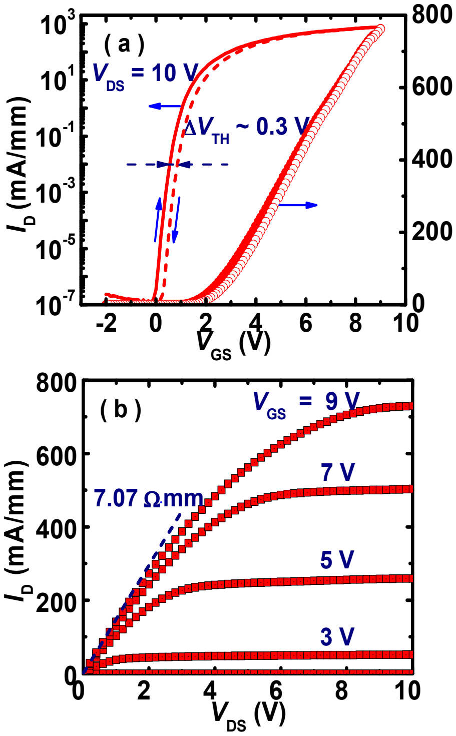

Fig. 2: (a) Transfer and (b) output characteristics of a MIS-HEMT with $L_G = 1.5$ μm and $L_{GD} = 10$ μm.

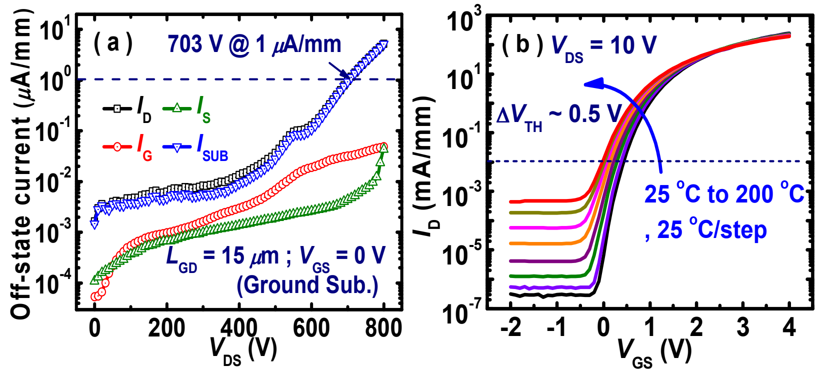

Fig. 3: (a) The off-state I-V characteristics of a MIS-HEMT with a gate-source voltage of 0 V and a grounded substrate. (b) Temperature (T)-dependent transfer characteristics of a MIS-HEMT with $L_G = 1$ μm and $L_{GD} = 2$ μm at T increasing from 25 °C to 200 °C.

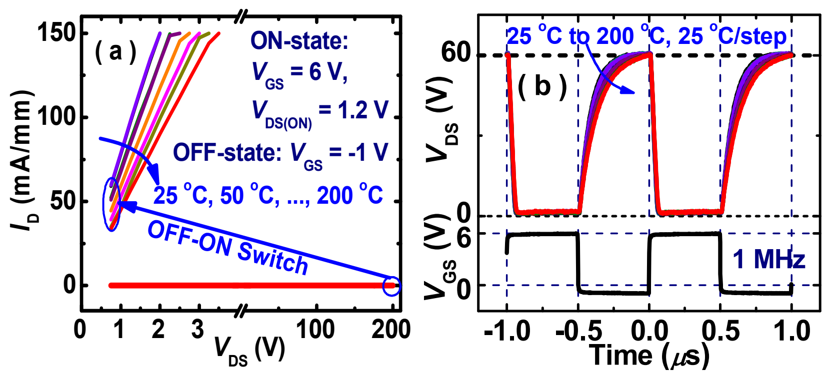

Fig. 4: (a) ON-wafer transient switching I_D-V_{DS} characteristics of a MIS-MEMT with $L_{GD} = 10$ μm at T ranging from 25 °C to 200 °C. The ON-state features V_{GS} and V_{DS} bias of 6 V and 1.2 V, respectively. The switching time is ~0.1 s. (b) Switching waveforms of a MIS-HEMT operated at 1 MHz with 50% duty cycle. V_{GS} is switched from -1 V to +6 V and the maximum V_{DS} is 60 V.

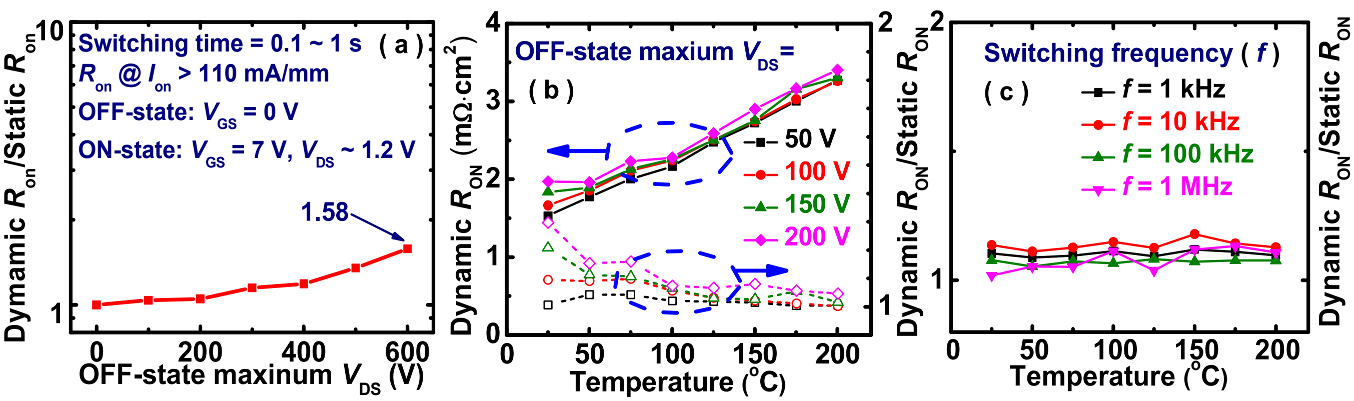

Fig. 5: Ratio of dynamic R_{ON} and dc static R_{ON} obtained by (a) low-speed high-voltage switching measurement at 25 °C, (b) T-dependent low-speed transient switching test with various OFF-state V_{DS} stress (50 V to 200 V) and (c) high-frequency (1 kHz to 1 MHz) hard switching characterization at temperature increasing from 25 °C to 200 °C.