# Fabrication of III-V virtual substrate on 200 mm silicon for III-V and Si devices integration

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By integrating III-V material with Silicon, it is possible to combine RF and photonic devices together with Silicon CMOS in order to create new functionalities[1,2]. Although a III-V layer grown on a III-V substrate can be directly bonded to a silicon substrate[3], the size of the III-V layer is limited by the donor III-V substrate. Thus, the direct growth of III-V material on Silicon is needed in order to achieve higher wafer size. The growth of III-V devices on Silicon is challenging due to the lattice mismatch, the thermal expansion coefficient mismatch between the silicon substrate and the III-V material and by the polar on non-polar material interface.

The purpose of this work is to obtain a 200 mm III-V virtual substrate with an excellent crystalline quality, a low dislocation density and a low bowing. Such virtual substrate can then be used to fabricate III-V electronic devices.

We use a MOCVD reactor to grow the III-V layers on silicon. First, a Ge intermediate layer is grown using the two-step growth technique [4], then a GaAs layer is grown. Subsequent III-V layers, such as InAlAs ternary alloy with a graded In composition are then grown in order to reach a higher lattice constant.

We will show our recent results on the growth of III-V materials on 200 mm Silicon wafers. First, the growth of GaAs on silicon using an intermediate Ge layer will be presented. The optimized growth process results in an anti-phase domain free GaAs layer with a smooth surface (RMS roughness < 10A). Then we will present the growth of an InAlAs graded buffer in order to increase the lattice constant, up to the InP lattice constant. The influence of the process parameters (temperature, grading rate, final composition) on the crystallographic and mechanical properties of the graded buffer will be presented. III-V layer on insulator on silicon are fabricated as well using direct fusion bonding. Preliminary electrical results of the III-V device grown on silicon will be presented.

[1] Kazior T E, LaRoche J and Hoke W 2013 (Invited) Heterogeneous Integration of III-V Devices and Si CMOS on a Silicon Substrate *ECS Trans.* **50** 1039–45

[2] Tanabe K, Watanabe K and Arakawa Y 2012 III-V/Si hybrid photonic devices by direct fusion bonding. *Sci. Rep.* **2** 349

[3] Czornomaz L, Daix N, Cheng K, Caimi D, Rossel C, Lister K, Sousa M and Fompeyrine J 2013 Co-integration of InGaAs n- and SiGe p-MOSFETs into digital CMOS circuits using hybrid dual-channel ETXOI substrates *2013 IEEE Int. Electron Devices Meet.* 2.8.1–2.8.4

[4] Lee K H, Jandl A, Tan Y H, Fitzgerald E A and Tan C S 2013 Growth and characterization of germanium epitaxial film on silicon (001) with germane precursor in metal organic chemical vapour deposition (MOCVD) chamber *AIP Adv.* **3** 092123

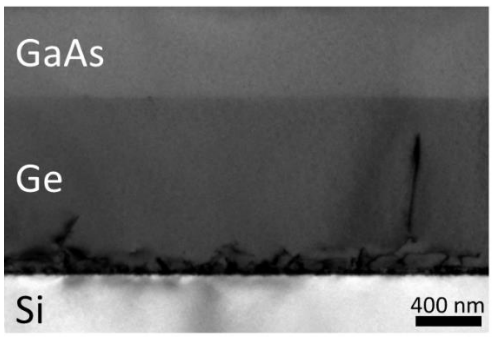


Figure 1: Cross-sectionnal TEM picture of a GaAs/Ge stack on Silicon substrate showing a low dislocation density and the absence of anti-phase boundary in the GaAs layer.

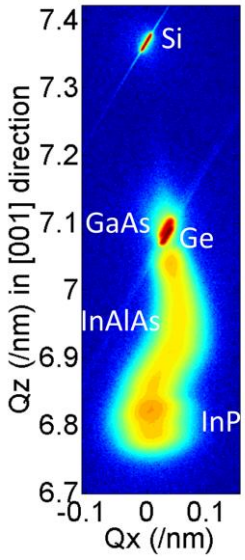


Figure 2: Reciprocal space mapping obtained using X-ray reflection around the (004) plane of the following structure: InP/InAlAs/GaAs/Ge on Silicon substrate.

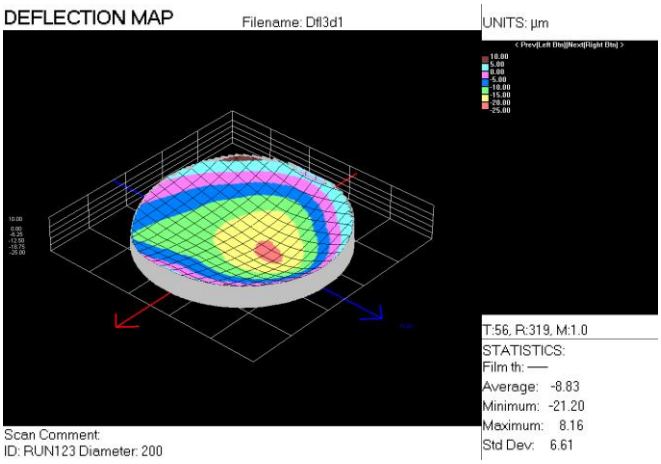


Figure 3: Bowing map of a 200 mm III-V on Si wafer showing a reduced bow of -8.83µm