Optimizing the SiC Plasma Etching Process for Manufacturing Power Devices

H. Oda, P. Wood, H. Ogiya, S. Miyoshi, and O. Tsuji

Research and Development Department, Samco Inc.,
36 Waraya-cho, Takeda, Fushimi-ku, Kyoto 612-8443, Japan
075-621-7841, pwood@samcointl.com

Abstract:

Compared to the mainstream semiconductor, Si, the wide band-gap semiconductor, SiC, has outstanding physical properties, such as a high dielectric breakdown field intensity and high thermal conductivity. Thanks to these characteristics, SiC is getting a lot of attention as a next generation material used for miniaturization and energy saving in power devices, and it is currently the focus of increased research and development aimed at practical implementation.

A broad range of technology is necessary to manufacture SiC power devices, but SiC plasma etching technology is essential when manufacturing device structures. However, while SiC has outstanding properties, it is a challenging material to etch, due to a low etching rate, low etch mask selectivity, the difficulty in managing the etched feature shape, and surface roughness after etching. In this paper we report on the optimization of some of the key parameters for successful SiC plasma etching of power device structures.

In developing SiC plasma etching technology, we utilized the SAMCO Model RIE-600iP, which is a single wafer processing system specifically aimed at etching challenging materials, such as SiC, using wafers up to 150 mm in diameter. The RIE-600iP employs a unique, planar ICP coil, which can deliver up to 3KW of 13.56 MHz power to the plasma. By using a high-capacity vacuum system and employing a lower substrate electrode that can be raised or lowered, it is possible to increase and decrease the distance between the wafer and the plasma source, and expand the process window.

One key plasma etching process technology required in SiC power device manufacturing, is SiC trench etching, which is essential in creating the SiC trench MOSFET structure. The following are required for successful, production SiC trench etching: a high SiC etching rate (> 500nm/min), a high SiC to oxide etch mask selectivity (SiC/SiO₂ > 5), good etching shape (vertical sidewalls, without micro trenches at the bottom) and sidewall smoothness.

It is not difficult to satisfy the requirements listed above with a SiC etching rate less than 100 nm/min. Figure 1 shows the result of SiC trench etching at a low SiC etching rate. However, when the SiC etching rate is pushed above 500nm/min., the degree of difficulty goes up in meeting the other etching objectives.

**Figure 1.** SiC trench etching using a low SiC etching rate. SiC etching depth = 2.52µm, SiC etching rate = 126nm/min, selectivity (SiC/SiO₂) = 8.1

Figure 2 shows the relationship between bias power, SiC etching rate, and selectivity (SiC/SiO₂). It is possible to have a high SiC etching rate and avoid micro trenches by raising the bias power, but the selectivity (SiC/SiO₂) goes down.

In order to obtain a high selectivity (SiC/SiO₂) with a high SiC etching rate, it is necessary to use a low bias power and adjust the process pressure and process gas flow ratios. Figure 3 shows the relationship between process pressure, SiC etching rate, and selectivity (SiC/SiO₂). In order to achieve the desired results, after taking into account the relationships between SiC etch rate, selectivity (SiC/SiO₂), etching shape, sidewall smoothness, and the etching parameters (ICP power, bias power, process pressure, and process gas flow ratios), we had to adjust our
etching parameters repeatedly to fine tune the trench characteristics.

**Figure 2.** SiC etch rate and SiC/SiO\textsubscript{2} selectivity versus the bias power.

The results of the optimization of the etching parameters for SiC trench etching with the RIE-600iP are shown in Figure 4. At this stage in our process development, the SiC etching rate is approaching 800 nm/min, and the maximum selectivity (SiC/SiO\textsubscript{2}) is 11.2. The sidewalls of the trenches are vertical and reasonably smooth and micro-trenching is absent.

**Figure 4.** Results of SiC trench etching with SAMCO Model RIE-600iP. SiC etching depth = 2.37 µm, SiC etching rate = 789 nm/min, selectivity (SiC/SiO\textsubscript{2}) = 11.2

In summary, the optimization of the etching of SiC for MOSFET trench structures for production of power devices involves an iterative process of tuning the substrate bias power, process pressure, and gas flow ratios in order to obtain acceptable SiC etch rates, high SiC/SiO\textsubscript{2} mask selectivity, and vertical sidewall profiles, while avoiding micro-trenching.

The main aspect of SiC trench etching that we continue to study is the SiC trench sidewall smoothness. In order to achieve a smoother SiC trench sidewall, we are re-examining factors that include the SiO\textsubscript{2} mask etching. Also, we are looking at the influence of the SiC trench sidewall condition on the electrical characteristics of SiC trench MOSFETs, and are working to clarify the smoothness required for the SiC sidewalls for these types of devices.

**Figure 3.** SiC etch rate and SiC/SiO\textsubscript{2} selectivity versus the process pressure.