Stress and Characterization Strategies to Assess Oxide Breakdown in High-Voltage GaN Field-Effect Transistors

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As the demand for more energy efficient electronics increases, GaN Field-Effect Transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN transistors are ready for commercial deployment [1],[2]. Our work focuses on gate oxide reliability and in particular, in contributing fundamental understanding behind the physics of time-dependent dielectric breakdown (TDDB) of the gate oxide, a catastrophic condition that arises after prolonged high-voltage gate bias stress. Towards this end, we are investigating stress-characterization techniques that allow transistor characterization during stress experiments. We leverage a rich body of work that has been carried out on silicon MOSFETs with regards to TDDB [3].

Our research is carried out on industrially prototyped experimental AlGaN/GaN MIS-HEMTs with a device breakdown voltage >600 V. There are several challenges involved in carrying out TDDB studies in these devices. First, the gate stack contains multiple layers and several interfaces. This gives rise to a somewhat uncertain electric field distribution. Second, there are complex dynamics involved as there is potential trapping in the AlGaN barrier, in the gate oxide and at their interface, and the inversion layer at the AlGaN/oxide interface is known to respond rather slowly. The complex dynamics result in a rather unstable and fast changing V_T, a significant complication in these types of experiments. Finally, with the current state of maturity of the technology, it is not obvious how to develop a characterization suite that is at the same time comprehensive and benign so that it can be used repeatedly without damaging the device. This abstract describes our research in developing suitable experimental techniques to characterize the physics of TDDB and our early results. More extensive results will be presented at the conference.

Fig. 1 shows the evolution of the gate current, I_G, in a typical constant-voltage TDDB experiment at $V_{Gstress}$=13.5 V. Oxide breakdown takes place at around 600 s. Other than time to breakdown and the observation of Stress-Induced Leakage Current (SILC), there is little insight gained from this type of experiment. We enhance this technique by pausing the TDDB stress and periodically characterizing the device by examining the I-V characteristics, as depicted in the inset of Fig. 2b. To validate this approach, we exploit a unique feature of TDDB identified in silicon MOSFETs that the charge to breakdown of a MOS gate stack, Q_{BD}, is constant, regardless of stress conditions [3]. By extension, under constant stress voltage the time to breakdown, t_{BD}, should also be a constant. We carry out TDDB experiments to verify this hypothesis following the conventional approach, and also under the new scheme with stress interruptions every 30 s where we measure the I-V characteristics at V_{DS}=0.1 V, shown in Fig. 2. The statistical results for t_{BD} in the Weibull plot of Fig. 3 exhibit a classic shape and indicate that the added complexity has not affected the breakdown measurements. Our new scheme provides new insights. In the subthreshold characteristics obtained during a typical experiment (Fig. 2a) we observe an initial large positive V_T shift followed by a slower negative V_T shift as the stress continues. The subthreshold swing (Fig. 2b) also exhibits an immediate increase from the virgin state right after the stress has been applied, but it then stays roughly constant for the remainder of the stress experiment. This suggests interface state generation early in the stress experiment perhaps coupled with electron trapping in the oxide or the AlGaN barrier.

Closer probing of the early stages of stress can be gained through a step-stress experiment where $V_{Gstress}$ is stepped up (inset of Fig. 4b). The evolution of I_G during stress, Fig. 5, reveals that for low values of $V_{Gstress}$, I_G tends to drop with time during a given stress step. This can be attributed to electron trapping in the oxide or the AlGaN barrier. Beyond around $V_{Gstress}$ ~12.5 V, I_G *increases* during each stress phase. This is known as SILC and in our case correlates with the turnaround of the V_T shift which initially is positive but at around $V_{Gstress}$ =12.5 V, begins to turn negative (Fig. 4a). We also see an increase in the subthreshold swing (Fig. 4b) as the step-stress progresses, but its most notable degradation takes place after $V_{Gstress}$ = 12.5 V. From these results, we can postulate that below $V_{Gstress}$ =12.5 V, electron trapping in the oxide or the AlGaN are the dominant effects, while for higher values of $V_{Gstress}$, trap generation at the oxide/semiconductor interface and in the oxide take place and the oxide is eventually driven into breakdown.

We have sought to further the information that we extract from TDDB experiments by introducing C-V characterization. We accomplish this by using the Capacitance Measurement Unit (CMU) of our measurement system to both apply stress and to characterize the device. This scheme allows us to monitor the capacitance evolution during the stress portion of the experiment, and also to carry out detailed C-V measurements when the stress has been paused. The capacitance evolution during the stress phase of multiple constant stress experiments at $V_{Gstress}$ =13.5 V is shown in Fig. 6. At this high value of V_G, the capacitance as well as capacitance frequency dispersion increase as the stress time increases. Both effects are consistent with charge trapping in newly created states in the oxide with the measurement frequency impacting the distance into the oxide that traps can respond to the AC signal. Similar C-V characterization during a step-stress experiment in Fig. 7 portrays a very rich picture. For low $V_{Gstress,}$ oxide trapping induced V_T shift produces a rapid drop in C_{GG} during each stress step. We can still, however, trace out the C-V characteristics for $V_G > 0$ V by looking at C_{GG} at the beginning of each stress step, before significant V_T shifting has occurred. This correlates with measured C-V characteristics up to V_{GS}=13 V as shown in the inset of Fig. 7. At higher $V_{Gstress}$, the capacitance increases during stress just as I_G did in the identical step-stress experiment of Fig. 5. This is another manifestation of the effect observed in Fig. 6 and reveals large trap formation in the oxide that precedes device breakdown.

In summary, we are developing new techniques to study TDDB in high-voltage GaN MIS-HEMTs. Our approach allows us to isolate the different roles of V_T shift, oxide trap formation and trapping, interface state generation, SILC and eventual breakdown. More results will be given in the full manuscript.

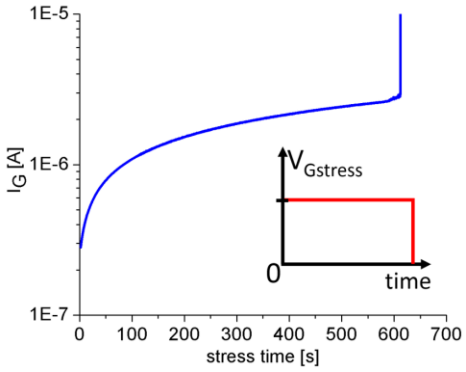

Fig. 1. Gate leakage current as a function of stress time during a constant $V_{Gstress}$ TDDB experiment. The FET is held at V_G=13.5 V until the device breaks down. V_{DS}=0 V.

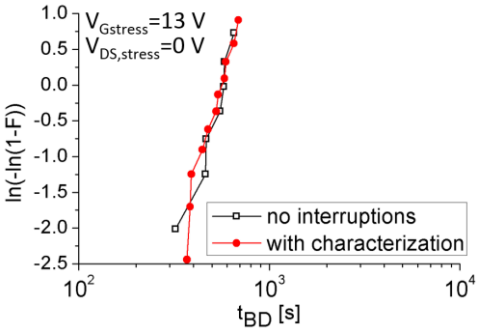

Fig. 3. Weibull plot of device breakdown for experiments with constant $V_{Gstress}$ and no pauses for characterization (black), and also experiments that utilize pauses during stress to characterize the device (red). F is defined as the fraction of devices that have reached breakdown.

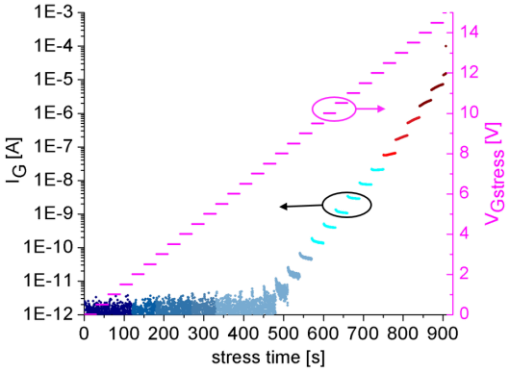

Fig. 5. I_G vs. stress time during a V_G step-stress experiment. $V_{Gstress}$ is shown on the right axis for scale. V_{DS}=0 V.

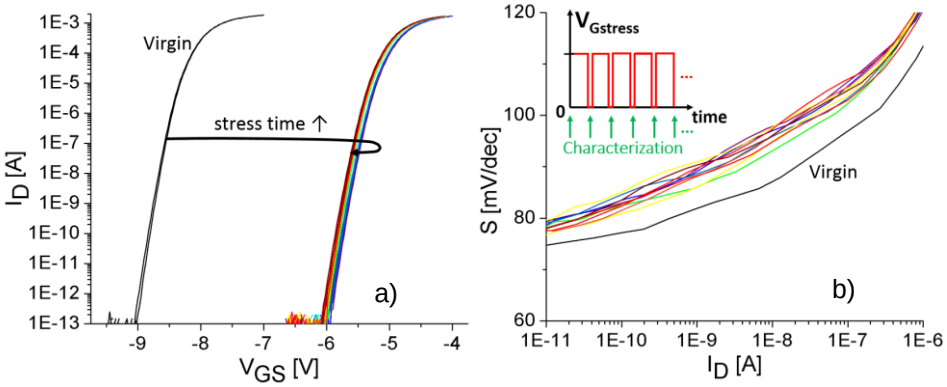

Fig. 2. a) Subthreshold characteristics at V_{DS}=0.1 V, for a TDDB experiment at $V_{Gstress}$ = 13.5 V. b) Corresponding subthreshold swing, from the average of each hysteresis sweep of the transfer characteristics. There is a fixed degradation of S at the beginning of the experiment, which then stays roughly constant until breakdown. I-V characterization is performed every 30 s.

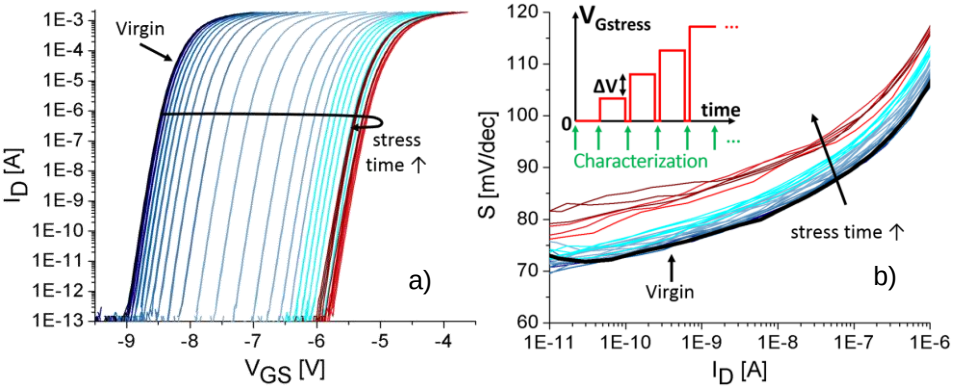

Fig. 4. a) Subthreshold characteristics and b) corresponding subthreshold swing for a TDDB step-stress experiment. S is acquired from the average of each hysteresis sweep of the transfer characteristics. $V_{Gstress}$ begins at 0 V and increases in 0.5 V increments every 30 s until the device breaks down. V_{DS}=0.1 V.

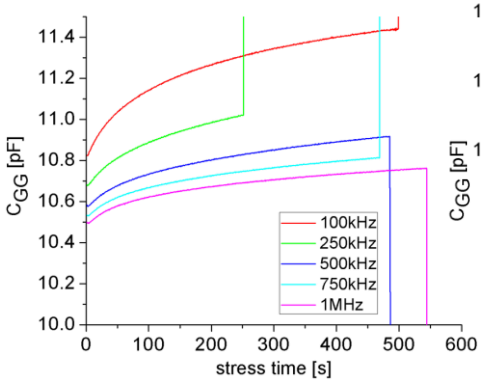

Fig. 6. Gate capacitance evolution over stress time at various frequencies in a constant V_G stress experiment. C_{GG} is measured at $V_{Gstress}$=13.5 V.

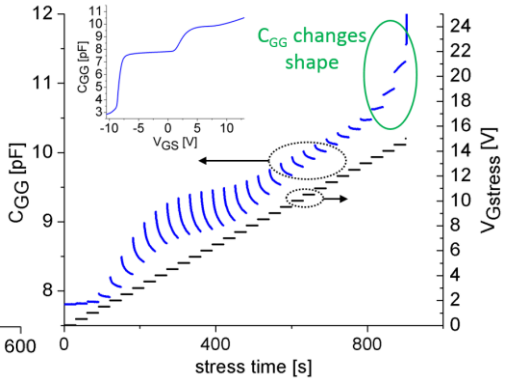

Fig. 7. Gate capacitance evolution at 550 kHz vs. stress time during a V_G step-stress experiment. C_{GG} is measured at $V_{Gstress}$ which is increasing by 0.5 V every 30 s. At $V_{Gstress}$ ~13.5 V, the shape of C_{GG} changes. Inset is of 500 kHz C-V characteristics on an identical device up to 13 V.

References
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[3] J. F. Verweij et al., Microelectronics J., vol. 27, no. 7, pp.611-622, 1996.