Improving Return on Invested Capital (ROIC) in PHEMT Technology

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INTRODUCTION

The semiconductor sector has been fairly volatile in the past three decades. When the PC market was expanding dramatically in the 90's, venture capital firms poured funding into semiconductor companies, and tech IPO's were regularly offered in NASDAQ. However in the recent years, venture capital has all but evaporated and the semiconductor sector has seen many consolidations, signaling that companies are facing ever increasing difficulties. A few recent examples are found here [1][2]. Due to the recent tumultuous times, many working in semiconductor fabs are asking why all this is happening and what were the main causes for this.

This paper will not try to answer these questions; instead we rely on experts that are well acquainted with the semiconductor sector---McKinsey. According to [3], the correct metric for evaluating semiconductor fab should be return on invested capital (ROIC), rather the typical metrics such as fab utilization or market share, or year-to-year revenue growth. ROIC takes account of the earning in context of the capital expenditure, whereas other metrics do not take in account the cost side of the equation. According to [3], while many firms have managed to secure funding for ever-more advanced fabs with greater capacity and at smaller lithography, few have managed to earn enough income to make the investment worthwhile. This is because while all capital expenditures (such as installing advanced tools or R&D of a new technology) are well-intentioned with attractive growths and profitability, it is difficult to predict its success due to the accuracy of market projections and competitors in this market. In fact much of the investment had been wasted without seeing any revenue. This has caused venture capital to seek more profitable investments elsewhere, and fabs that suffered losses faced shutdowns or acquisitions.

In order to generate more ROIC, the Qorvo Greensboro fab has been actively finding ways to reduce cost and increase yields. The motivation to seek more return on existing processes is felt throughout the organization. This paper seeks to document just two yield improvement projects. We have 1) improved PHEMT wafer uniformity by working with the epi vendor, and 2) improved adaptive metal selection to fine-tune critical parameters at the product die. We use KGD and PCM data to show the yield improvements, and use ADS simulation to understand the sources of variation in circuits. In keeping with the philosophy of ROIC, we will estimate the potential benefit as well as the cost needed to achieve them, and evaluate their success on an incremental ROIC. In order to make this industry-relevant, we created a "typical GaAs Fab" financial model using reported data on revenue, profit margin, etc.

SECTION I: IMPROVED WAFER UNIFORMITY

The need for wafer uniformity improvement was first noticed in a particular mask where failed KGD die were always on the wafer edge (Figure 1).

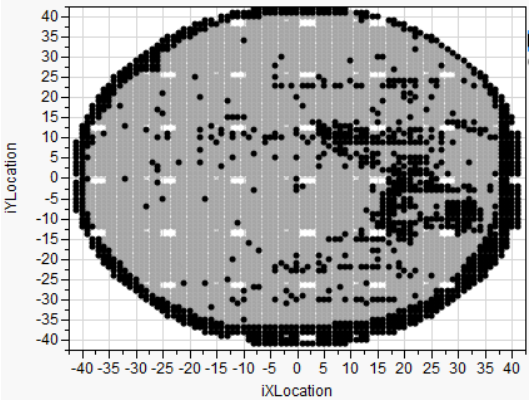

Figure 1. KGD map of a typical low-yield PHEMT wafer where the failed die concentrated at the wafer edge.

We began a series of steps to understand this failure signature. First, we tested every PCM site for a few wafers to see if anything was out-of-family on wafer edge. Immediately it was apparent that Vpo was more positive and sheet resistance was low on the wafer edge. Through ADS simulation outlined in [4], we confirmed that the root cause to KGD failure was the Vpo being shifted too positive, causing bias currents to be shifted too low. Confident that we can pinpoint failure to the epi and not the process, we began a series of meetings with epi vendors, to bring this to their attention and worked with them to investigate the cause of epi non-uniformity.

Initially as a DOE, we tried a variety of different platen conditions, and we found that KGD yield improved by 8%. Similar epi studies can be found in [5]. We immediately settled on the best condition and grew more wafers to run in a different maskset. The KGD yield results are shown in Figure 2, where the new epi wafers (red circles) were significantly better in yield than historical values (black dots). On average the new epi wafers were 5% higher in yield; however at this point it is not apparent how much the overall KGD yield improvement was going to be, since different mask would have different products and applications and therefore different failure signatures. In order to go to full production, we settled on a solution that modified some of the existing platens while purchased new ones. The cost to modify existing platens was minor however the cost of new platens was expensive, and therefore the epi vendor tried to modify existing platens as much as possible.

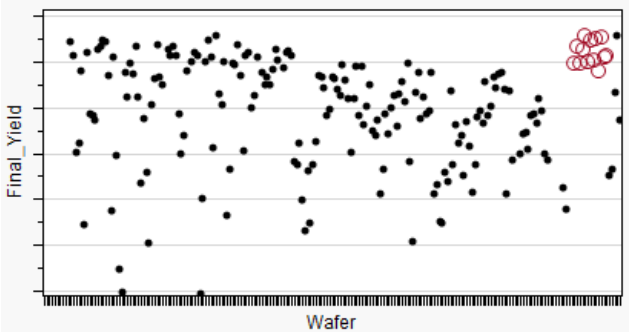

Figure 2. KGD trend chart of a PHEMT maskset, x-axis is by wafer for the past year time frame. Circles are wafers with the improved epi growth.

As we started to implement the epi growth improvement during volume production, a few minor adjustments and control processes had to be made, and after a period of three months of monitoring by engineering, the epi growth have become stable enough to hand over to production. After some time when approximately a thousand wafers of new and old epi were run, the average yield increased by 2%. As we depleted the old epi, the overall yield continues to hold at this level.

SECTION II: THE MOTIVATION AND IMPLEMENTATION OF ADAPTIVE TOP METAL

With respect to KGD yield improvement, sources of variation such as TFR, beta, or Vpo interact within the circuit to create a complex behavior; oftentimes it is desirable to focus on variations that have the most impact. ADS DOE program allows one to quantify the impact of each source of variation; although it is a tool mainly for designers to optimize circuits, yield engineers can also find it helpful to determine which fab related parameters impact yield the most and therefore should be the main focus for improvement. The procedure is as follows. First it begins with hypothesis on different design variables that can change the final yield. Using voltage regulator as an example, possible variables could be TFR, Vpo, Gm, and device width. Then the DOE corner values for each have to be determined either from PCM or process data. We have used +3/-3 sigma values as corners. Then DOE goal has to be specified, and in this case, it is the steady-state DC output of the regulator that most impacts yield. DOE simulation results are shown in Figure 3, which determines that D-mode Gm, TFR sheet resistance, and E-mode Vpo all contribute to regulator variation; while D-mode Vpo and device width do not contribute much to regulator variation. D-mode Gm is the largest contributor which is responsible for 50% of the regulator voltage variation. However TFR is a close second with 35%.

The difficulty with fab yield improvement is that there are a diverse set of masksets, each with their own sensitivities. Oftentimes it is risky to re-center any process; for example, adjusting TFR might increase yield for some masks while decreasing yield for other masks. Process tightening is therefore highly desired; however it is not clear that effort spent on process improvements (for example, TFR Rsh control) will succeed. Usually a short-loop or trial experiments can seem very promising, however when they are rolled into full production there are many unforeseeable hurdles. Also at some point the process variation is due to fundamental limitations of the tools and materials being used, and further improvement requires new capital investments. If there are no more "low hanging fruit" left for TFR improvement, a new evaporator would be needed. As for D-mode Gm variation, either a new epi reactor is needed, or a completely different characterization tool to better differentiate each epi layer. As previously explained about the ROIC, new expenditure means increased invested capital and therefore additional income is expected to justify the cost; the cheaper and equally good solution is always desired.

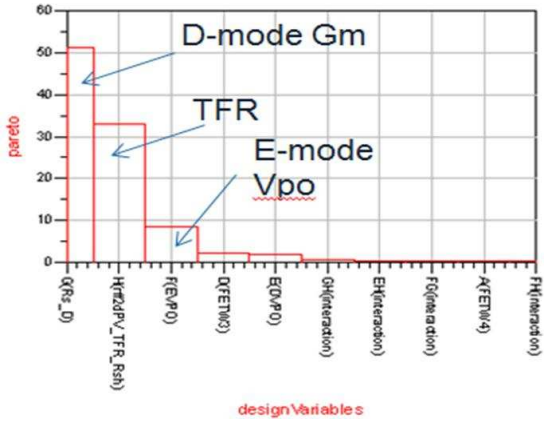

Figure 3. ADS DOE to find sources of variation that impact the voltage regulator, in pareto.

Another way we reduce variation is the concept of adaptive mask; essentially there are additional top metal plates that we can choose from that will give us reduced variation. We offer "high", "nominal", or "low" top metal masks for adaptive. The difference between these three masks is mainly the shorting or opening of certain resistors that can adjust the bias up or down. The process for adaptive mask is summarized in Figure 4. The wafer is PCM tested at FITST(first-interconnect level) for device parameters such as Vpo or TFR Rsh. In addition to the standard structures we have also added "mini" circuits inside the PCM which is also tested. These "mini" circuits could be a biasing circuit, or a regulator; they use the same PCM testers, the test conditions are set based on how these circuits are used in the product. Essentially at FITST we have an idea whether a wafer is "high", "nominal", or "low" with respect to where it sits in the overall distribution. At top metal photo step, an algorithm based on a set of criteria is used to determine whether the "high", "nominal", or "low" mask will be better yield. Then once top metal deposition is complete and dielectric is opened

for probing, the wafers are tested at final test (FNTST) to verify that adaptive is performed correctly.

The same regulator circuit is selected as an example for adaptive mask. First, the designers determined how much to adjust the VREG based on the expected process variation, then regulator circuits were added into PCM area to be tested at FITST and FNTST. Next the algorithm needs to be implemented. In this case we determined that the "low" mask is used when FITST-VREG measured less than 2.97V, "nominal" mask is used when it is between 2.97V and 3.07V, and "high" mask is used when it is higher than 3.07V.

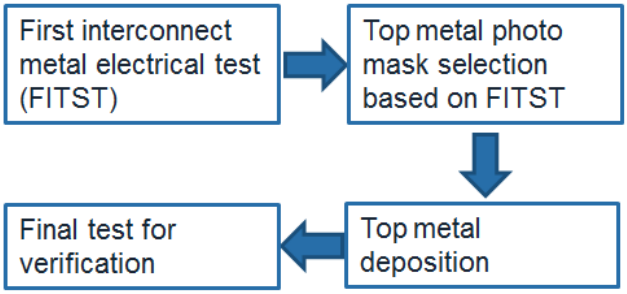

Figure 4. Basic procedure of the adaptive metal.

Traditionally, adaptive mask can be set based on typical PCM parameters such as beta, Vpo, etc, and we have observed significant yield impact in both HBT and PHEMT technologies. Adaptive mask based on circuits within PCM is now setup for several PHEMT products, and product groups have reported significant yield improvements. At this point there are not enough data to give a full illustration of how circuit adaptive works, and therefore we again use ADS Monte Carlo simulation for this purpose. This regulator simulation has been carefully calibrated and verified, and published in CSMANTECH 2014 [5]. Figure 5 illustrates how the adaptive mask should work. The X-axis shows the VREG at FITST, and Y-axis shows the VREG at FNTST. Without adaptive the VREG remains the same at FITST and FNTST. However with adaptive mask, values with VREG less than 2.97V were increased by 70mV, and VREG greater than 3.07V were decreased by 70mV. Therefore the original Gaussian distribution of VREG have the tails "folded" back into the nominal values, thus tightening the overall sigma from 45mV to 25mV. This reduction in sigma is why adaptive is so effective in improving yield. Depending on how poor the original Cpk is, the yield improvement can be up to 25% with adaptive. Based on data from a wide portfolio of HBT masks using beta as adaptive parameter we estimate about 3% average yield improvement.

The cost of adaptive mask needs to be accounted for. This requires 2 additional masks to be purchased for each maskset, which is trivial. However suppose we want to find our highest volume products and implement adaptive mask then there would be considerable effort to redesign and entire masksets need to be re-ordered. As for implementing the top metal mask selection at photo step, IT support and technicians and operators would also need to be involved. The cost of implementing this change is shown in discussion section.

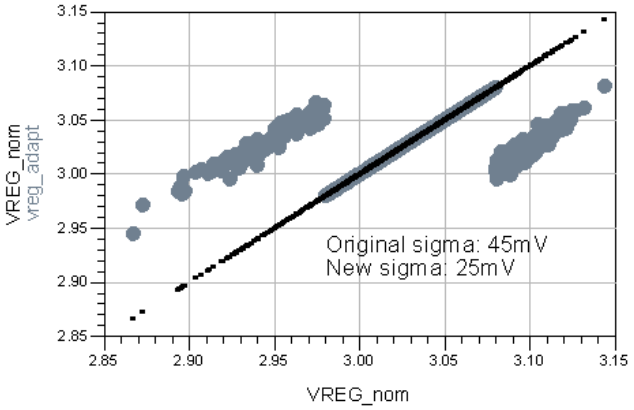

Figure 5. The impact of VREG adaptive mask, illustrating what the original distribution was (in blue dots) and how the tails are folded back into the distribution (in red circles, with adaptive).

SECTION IV: DISCUSSION

Many technical papers begin with stating the problem and then end with problem solved or observations made. However, the "was it worth it?" questions were not always asked. Did the effort to arrive at the solution and the cost of the solution itself make sense financially? In other words what is an acceptable return on that investment (ROIC)? From CAPM model[7], the expected rate of return can be calculated based on the return on a riskless investment (i.e., treasury bonds), and market equity return (i.e., stock market return). The generally acceptable rate of return ranges from 6-9% for a well-diversified investment. However for individual projects that are subject to many more risks, the acceptable rate of return is closer to 12-15%, in order to justify the additional risk.

In order to calculate the ROIC we need manufacturing statistics such as wafer volume, price per wafer, processing cost, etc. Since company-specific information can't be discussed in the broad community, a "generic GaAs foundry" is created based on conference publications, US Bureau of Labor Statistics and public financial reports of the top semiconductor foundries. This foundry model will represent an "average" GaAs fab, as a means to treat the fab as an independent unit and thus assess its financial strengths. There is no certainty in this analysis since companies don't divulge all business detail, the forecast numbers can be wrong, and broad estimations are sure to create errors. Nevertheless, this is still the common practice by investors (for example, see [7]). It is better to have an inaccurate model based on best-guess estimates than to have no model at all.

Details from [8] provide an estimate on the total usage of GaAs wafers (and annual growth), the amount of major

competitors. Dividing the total GaAs wafers by the total number of competitors one can get a "typical" fab volume. The average price of GaAs wafers and estimated cost of fab are found through the financial statements of major GaAs foundries. Reviewing several companies' statements the general trend is that at 70% utilization rate the fab is about breaking even (net income is zero). Given these parameters, a generic GaAs fab model is generated.

Table 1. Parameters used in the generic GaAs fab model.

Total yearly GaAs wafer demand (ksi)	29900
Major competitors	5
Price per wafer	$1,600
Cost of building GaAs fab	$200,000,000
Fab capacity	66,000
Fab fixed cost	$42,000,000
Fab variable cost per wafer (% of wafer price)	40%
Marginal tax rate	38%

For brevity, we will not show the entire spreadsheet of ROIC calculations, but we make the following observations. First is that fab utilization rate directly affects the revenue and income. Therefore the return on invested capital will rise as utilization rate rises. In this model, as fab utilization increased from 80% to 94%, the fab ROIC increased from 4.2% to 8.5%. In the context of expected return of 6-9% this increase causes the fab to go from under-perform to market-perform (meeting investors' expectations). However if significant additional capital is invested to achieve the 94% then the ROIC would not be so lucrative.

Given this fab model, we can now estimate the impact of the two yield projects described earlier. The methodology is largely based on the incremental cash flow analysis given in [7]. The major difference between stated income and cash flow is that cash flow adds back depreciation and subtracts out "maintenance" capital expenditure. For the wafer uniformity project, the total investment was $35,000, the amount saved by 2% yield difference in PHEMT technologies amounted to $122,000. Thus the ROIC for this project was calculated to be ~300%, dramatically exceeds the expected return. However, this project did not appreciably increase the fab ROIC, since $122,000 was minor in comparison with the nearly $17million cash generated from operating activities.

For the adaptive mask project, we calculate the ROIC as if this fab decides to implement retroactively on all major production masks. We assume reasonable cost to redesign using adaptive, purchase new masksets, cost of IT support, fab logistics, and we estimated $495,000 was needed. Much of this cost is due to ordering new masksets of existing products; however, if only new mask adopts adaptive mask then within 2-5 years it would be a large majority of fab volume anyway. Then the cost would be much lower since only two additional top-metal plates are needed. We assume a slow ramp to implement this across all masks by year 6, and the fab yield improvement by then is 3%. By year 6 the annual savings from this yield improvement would have grown to $1.8 million, more than 10% of the total income of $17 million. Even being very conservative in cost and ramp rate, the ROIC for this project was almost 350%, and since this impacted the entire fab the overall fab ROIC increased from 8.5% to 9.4%. This 0.9% increase in fab ROIC shows that implementing adaptive mask makes sense financially. Due to the low mask cost, ordering two additional top metal plates to improve yield is well worth its cost.

Section VI: Summary

We have discussed two yield activities, namely improvement in wafer uniformity and adaptive mask. Then we evaluate whether these projects exceed or don't exceed the expected return. In this case we have chosen to use ROIC as the framework for finance evaluation, the process was discussed, and it was found that both projects gave adequate returns on investment. Through this process, we also have found many challenges in assessing the true returns of a project. Nevertheless, the exercise has helped us to become more mindful of how efficient we invest our time and resources.

Section VII: Acknowledgement

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Section VII: Reference

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ACRONYMS

EVM: Error Vector Magnitude
KGD: Known-Good Die
PCM: Process Control Monitoring
FEM: Front-End Module