Using GaAs Diesort Methods for Efficient High Volume Capacitor Testing

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Abstract

Diesort multi-site probe cards and methodologies for GaAs integrated circuit die have been used for multi-faceted characterization of MIM capacitor leakage currents and ramp-to-breakdown voltages for processes under development. By transforming the die inside the bond pads with taps into that circuit's capacitors and also using those same bondpads for designed arrays of capacitors, we have been able to do both overvoltage stress and ramp to breakdown testing on almost 100 thousand capacitors per wafer (over 25 cm^2 of total capacitor area) in a short time, enough volume to allow us to characterize accurately capacitor defects at a sub-0.1% level, something impossible with normal capacitor PCM test quantities.

…and good men's lives
Expire before the flowers in their caps,
Dying or ere they sicken.
Shakespeare, Macbeth, Act IV, Sc.3

INTRODUCTION

Our caps, Metal-Insulator-Metal (MIM) capacitors, should certainly not "die before they even sicken". They have been the subject of frequent study in the compound semiconductor world because of their critical importance for circuit performance and reliability. [1] However, as capacitor fabrication has improved, reliability problems have become rarer and thus harder to characterize with Process Control Monitors, which would normally only be present in the range of 5 – 25 sites per wafer on production masks. At the same time, the actual MIM capacitors in the product chips are usually inaccessible for on-wafer DC leakage testing, the usual means of evaluating capacitor reliability.

Most fabs do on-wafer 100% DC die testing to keep known bad die out of multi-chip module assembly. We set out to use those dense test site maps (typically greater than 10 thousand die per wafer) as a means to get adequate samples to detect capacitor defects at very low levels with either direct capacitor leakage measurements before and after over-voltage stress or with controlled voltage ramp to breakdown testing.

TEST METHODOLOGY

The capacitors in bond pads in a typical GaAs PA in our fab are shown in Fig. 1. This dual-band circuit has about 50 capacitors in it, ranging in size from 200 to about 28,000 square microns. None of those capacitors are accessible to test in normal DC diesort.

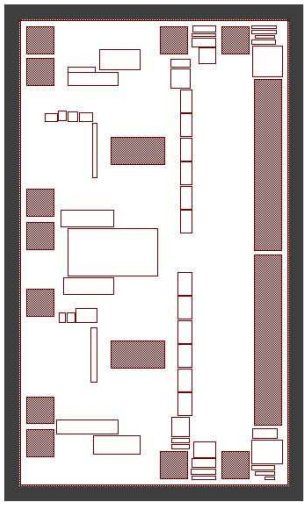

Fig. 1 A typical PA's Capacitors (open) and Bondpads (filled)

The mask was altered to bring 7 capacitors and the Device-Under-Test (DUT) ground out to bondpads for test with our systems [2] in which each DUT is assigned 10 Source – Measurement Units (SMU's). In most cases, several neighboring capacitors were connected together to increase tested capacitance area for more easily measured leakage currents.

The mask went through the complete normal HBT fab process to accurately represent our processing conditions. It is important to test many capacitors situated as they are in real production die to survey a relevant sample of physical phenomena which might not be immediately apparent, such as interacting topography and stress effects. Production AVI (automated visual inspection) can also be implemented on these die, allowing us to rapidly characterize failure modes, and to evaluate the effectiveness of AVI screening.

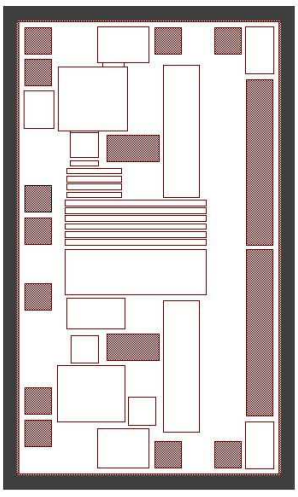

Fig. 2 Special test chip with Capacitors (open) and Bondpads (filled)

In addition, using the same bond pad footprint to allow for normal testing with our DC diesort testers and multi-site probe cards, we created a second variant chip with a variety of capacitor layouts, as shown in Fig. 2. This allows us to look at

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capacitor layout properties of particular interest like numbers of corners, area, shape, etc.

The 8 capacitor layout variations in the second chip are reviewed in Table 1. The two kinds of chips are differentiated by test results and by position on the wafer so both chips are tested in a single pass on the test systems.

TABLE I
CONTENTS OF SPECIAL CAP TEST CHIP

Cap	Layout Description	Area (um2)
1	Rectangle in upper right die corner.	9375
2	Vary Contact2 size & spacing, Cap Top Plate has inside corners	58578
3	3 large area rectangles	57280
4	1 large rectangle with C-B diode ESD protection	33250
5	1 large rectangle	33250
6	Increased enclosure of top plate by bottom plate and increased top plate enclosure of Contact2.	51903
7	Rectangle in lower right die corner.	9375
8	11 large perimeter rectangles.	43485

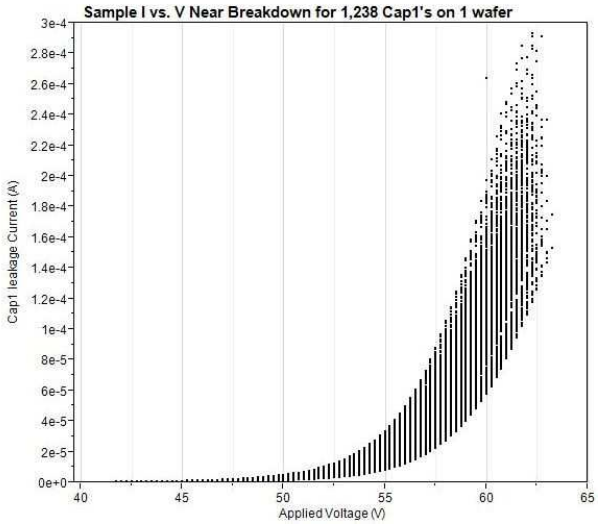

Fig. 3 2.5 V/sec I-V curves for 1,238 Capacitors, Each with Area of 9375 μm^2, on a Typical Wafer

We either tested all caps on a wafer in one way or (more commonly) divided the wafer into a large section of 13,307 DUTs (97,229 capacitors with total area of 23.6 cm^2) for overvoltage leakage testing (4 V, 27 V, 42 V, then 4 V again) and smaller stripes of 1,238 DUTs (9,098 capacitors with total area of 2.29 cm^2) for (destructive) ramp to breakdown voltage testing. Both maps include both circuits (Figs 1 and 2). Ramp to breakdown data could either be recorded as the complete I-V curve on a adjustable ramp rate, typically 2 -5 V/sec, up to a voltage above expected breakdown V, or more simply as the voltage values where the capacitors broke down, defined as reaching compliance currents of 3.0 mA. A set of 1,238 I-V curves near breakdown is shown for one capacitor variant on a sample wafer in Fig. 3.

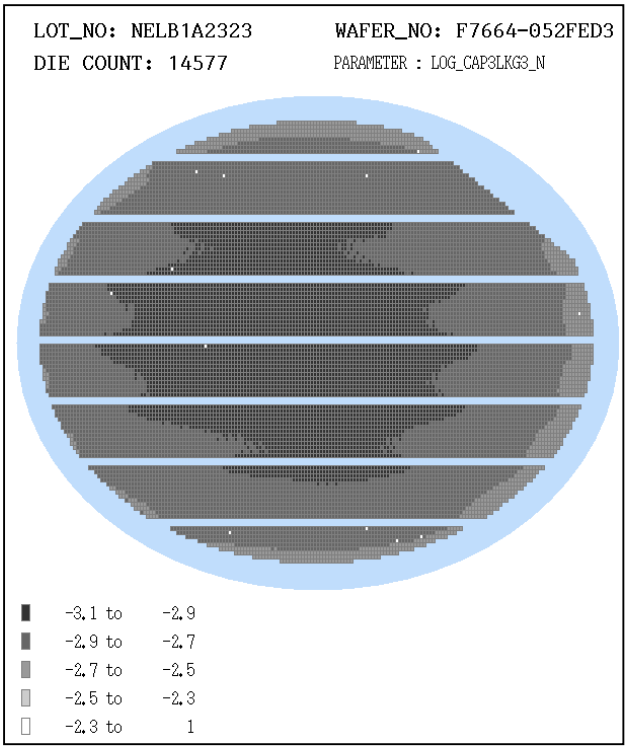

Fig. 4 Wafer map of log capacitor leakage current (A/cm2) at 42 V for Cap 3 (Table I)

Ramp breakdown voltage is a property which allows extraction of field acceleration factors which can then be used to establish the appropriate short-time high-voltage constant stress condition which represents usage lifetimes of interest. Once acceleration factors are known (from ramp testing at multiple ramp rates) and the short constant stress condition is established, constant stress can be used to collect defect density statistics of large populations.

RESULTS OF TESTING – CAPACITOR PROCESS EXPERIMENTS

A useful characterization is how capacitor leakage varies over a wafer. Figure 4 shows a high-resolution (14,577 point) wafer map of capacitor leakage current at 42 V. All areas have low leakage but lower leakage is seen in the wafer center. In this map, defective capacitors are seen as white. The map also shows the stripes of DUTs on the wafer reserved for destructive ramp to breakdown testing.

The most basic MIM Capacitor property is the dielectric layer thickness. High voltage leakage and breakdown are widely reported [1] to be very sensitive to that property. Fig. 5 shows one example of a cumulative probability plot of log (leakage) vs. Silicon Nitride dielectric thickness, showing the expected trend.

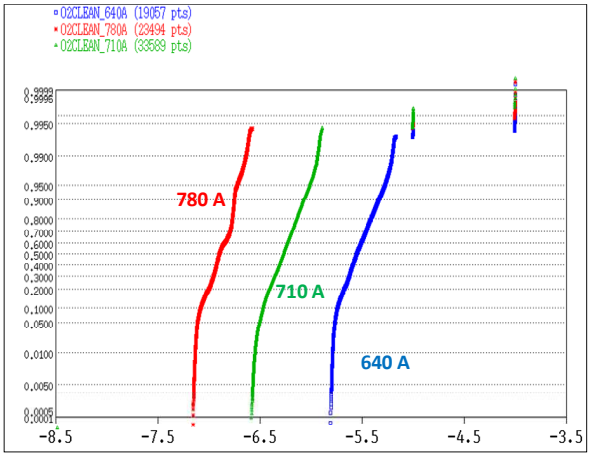

Fig. 5 42 Volt Cap Leakage vs. SiN thickness for Cap3

Figure 6 shows a cumulative probability plot of ramp breakdown voltage (BV) for capacitor bottom plates made with 1.0 and 0.3 µm Au films. As expected, and as widely reported [1], the thinner Au film has a smoother surface resulting in higher ramp BV.

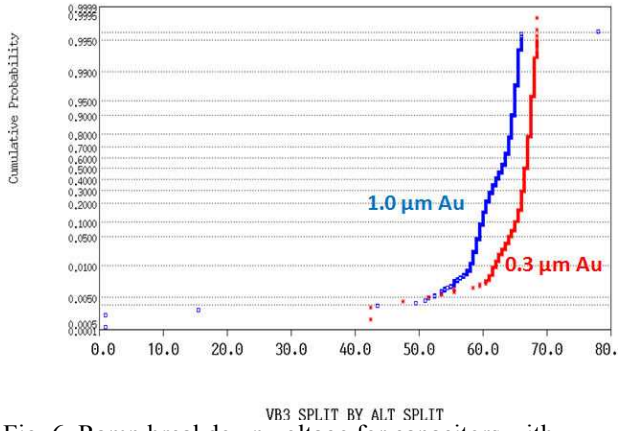

Fig. 6 Ramp breakdown voltage for capacitors with different bottom plate Au thicknesses

As a final example, it has been reported [3] that lower NH_3 flow rates for a fixed SiH_4 flow rate in the PECVD deposition of silicon nitride capacitor dielectrics (giving slightly Si rich films) result in much higher high voltage leakage currents. We were able to confirm and quantify that trend, as shown in Figure 7.

SUMMARY AND CONCLUSIONS

By adapting and extending standard DC diesort testing for a special capacitor test mask, we have been able to test sufficiently large quantities of MIM capacitors to assess the low levels of capacitor failures expected in modern GaAs HBT fab processes. Data from testing like this can be and has been used to continuously improve our MIM capacitor uniformity, robustness, and reliability.

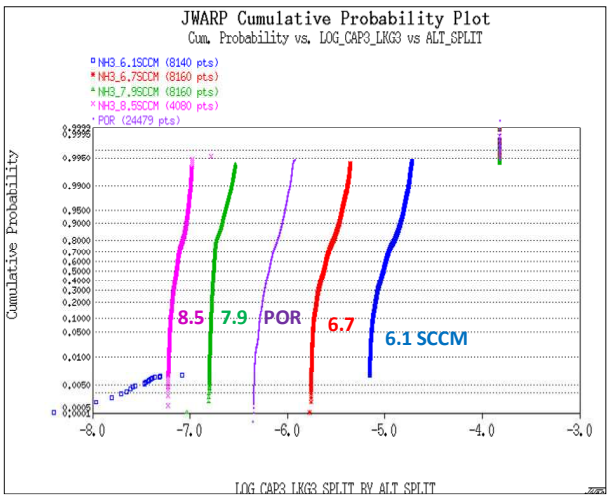

Fig. 7 42 V Cap3 Leakage vs. NH3 Flow (POR = Process of Record)

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REFERENCES

[1] S.A. Chevtchenko, S. Freyer, L. Weixelbaum, P. Kurpas, and J. Würfl, 2014 CS Mantech Technical Digest, pp. 131 – 134, May 2014
P. Leber, M. Hollmer, D. Shcrade-Köhn, J. Thorpe, R. Behtash, H. Blanck, H. Schumacher, 2011 CS Mantech Technical Digest, pp. 275-278, May 2011
D. J. M. Hamada and W. Roesch, 2008 Reliability of Compound Semiconductors Workshop, pp 57-71
S. Horiuchi, K. Matsumoto, M. Sakachi, T. Ooki, H. Nakamura, K. Adachi, M. Shinohara, 2006 CS Mantech Technical Digest, pp. 97-100, April, 2006
M.J. Brophy, A. Torrejon, S. Petersen, K. Avala, L. Liu, 2003 CS Mantech Technical Digest, pp. 57-59, May 2003
[2] M.J. Brophy, B. Bergeson, R. Grover, K. Quick, V. Woerdeman, A. Pronin, and P. Griffiths, 2014 CS Mantech Technical Digest, pp. 297 – 300, May 2014
[3] S. Habermehl and C. Carmignani, "Correlation of Charge Transport to Local Atomic Strain in Si-rich Silicon Nitride Thin Films", Appl Phys. Lett., 80, 261-263 (2002)

ACRONYMS

AVI: Automated Visual Inspection
BV: Breakdown Voltage
DUT: Device Under Test
HBT: Heterojunction Bipolar Transistor
MIM: Metal – Insulator – Metal
PA: Power Amplifier
PCM: Process Control Monitor
PECVD: Plasma Enhanced Chemical Vapor Deposition
SMU: Source – Measurement Unit