Rapid Production Readiness Through Process Margin Study: How to Isolate the Epi and Fab Parameters That Really Matter

S. Hurtt, D. Schwartz, J. Yang, S. Nedeljkovic, T. Henderson, F. Pool
Qorvo, Inc. 2300 N.E. Brookwood Parkway, Hillsboro, Oregon 97124
Phone: (503) 615-9691 Email: Sheila.Hurtt@tqs.com

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Abstract

In 2014, Qorvo developed a new HBT high performance power amplifier technology for cellular and infrastructure applications. The critical challenge during process development was to deliver a high performance technology rapidly and with high yield at release. The margin studies we designed accelerated yield learning and revealed areas for focused process improvement to enable a stable, high-yielding process prior to launch.

INTRODUCTION

Rapid development cycle times are beneficial in bringing new RF technologies to market. Fast development cycles must be aimed at product intercepts and scheduled to coincide with customer timelines. However, faster development can mean added risk for yield since there is less time and fewer wafers run to find yield issues. Qorvo has mitigated this risk by using more extensive margin studies than in past development. But how can margin studies, which have been used extensively throughout this and other industries, be done in the most meaningful way?

PURPOSE

This paper describes a process margin study methodology as part of an overall program to deploy new epi and fab process flows for a new InGaP HBT technology. Epi, etch, metals, and photo processes were varied in an attempt to discover how much parametric variation could be attributed to each unit process in Qorvo's new process flow. As part of developing a new HBT technology, the Qorvo development team:

(A) Identified test parameters dependent on process variables in fab and epi

(B) Ran experiments to gather sensitivity of parameter vs. process input variables, including epi, etch, metals, and photo processes affecting emitter, base, collector or subcollector. Inputs were changed by more than +/- 3σ to ensure parametric shifts beyond ordinary process variation

(C) For device parameters with high sensitivity to an input, and whose variation is critical for either circuit performance or for yield, took action to reduce variation

The best use of margin studies is to map the process input space to device performance. Margin studies can then be referenced after production begins to minimize data mining, redundant margin experiments during volume manufacturing and validate the product performance response to the volume process variation. In the description below we present a means to summarize many simultaneous margin studies to achieve a more comprehensive evaluation of the technology to be released.

EXPERIMENTAL METHOD

Margin studies were done on each individual critical layer in the epi stack, including layers within the emitter, the base, the collector and subcollector. Epi parameters were typically varied much more than the expected production variation so that parametric changes would be larger than measurement error. Doping, thickness and composition were varied. Likewise, photo, etch, metal deposition, dielectric, planarization and alloy steps were varied by more than +/- 3 standard deviations. Focus was placed on the steps that presented yield challenges in the past on HBT processing, or on steps that were changed in the new process flow. Cross-terms between epi and fab steps including base metallization and emitter layer thickness, base metallization and base thickness and doping, and emitter overetch time and emitter mesa thickness were performed. Ultimately, the goal was to understand whether the new Qorvo HBT process presented an improvement over the previous one. A sample margin study will be covered here: epi emitter layer thickness and base metal alloy depth.

To understand the impacts of each process input shift, multiple sets of data were taken and correlated back to the underlying experiment. In line fab metrology data were collected and used to evaluate the margin for key fab steps like photo and etch. For the more subtle epi and cross-term experiments, the team relied on large and small unit cell devices measurements in extended DC and RF PCM. Full over power, bias and temperature characterization is ongoing for a subset of variants that need to be understood further, and which will ultimately be used to build a statistical model for designers.[1] The overall goal of the exercise is ultimately to discover process parameters that drive variation

in circuit level performance metrics PAE, gain and linearity; to drive down variation where possible; and to transmit information about expected variation to circuit designers so they can design around process variation where possible.

This paper will focus on the emitter and base cross-term experiment where base metal depth and emitter layer thickness were variables. The experimental design is shown in Figure 1. The new HBT process uses an InGaP emitter layer with a base metal contact that is alloyed into the base layer. To characterize the process corners, the experiment included deep base metal with thin InGaP and shallow base metal with thick InGaP. Adding the center condition for base metallization while varying just the InGaP thickness provided a separate sensitivity value for epi and base metal variables.

		Fab: Base metal depth		
		-23%	POR	+23%
Epi: InGaP emitter layer thickness	-10%	X	X	X
	POR		X	
	+10%	X	X	X

Figure 1: Emitter layer thickness and base metal depth variants and cross-terms

Figure 2 shows the emitter-base sidewall leakage dependence on emitter layer thickness. The data shows that base metal depth has no impact on leakage, but emitter layer thickness variation of +/-20% changes leakage by more than one order of magnitude. Likewise, for Re, Bvebo and Cbe, base metal depth had no impact on parametric variation, but epi layer thickness had a strong impact.

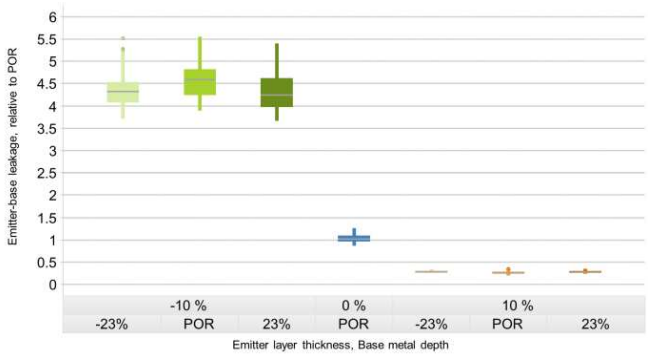

Figure 2: Emitter-base leakage for each emitter layer and base metal depth combination.

Historically, base contact resistance and Vbc variation resulted from base metal alloy depth variation on the last generation HBT process. Figures 3 and 4 show that little variation can be attributed to the metal alloy depth. Other variables were examined for variation due to metal depth, but none were observed. This result represents a clear improvement over the prior generation HBT.

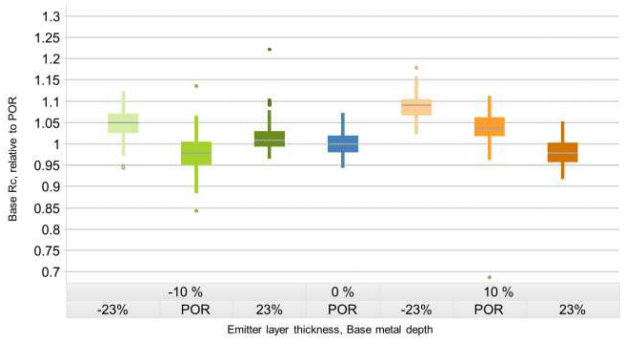

Figure 3: Base contact resistance for each emitter layer thickness and base metal depth combination. Note that for emitter layer thickness POR+10%, Rc Base appears to be correlated to base metal depth, but at POR-10%, it does not.

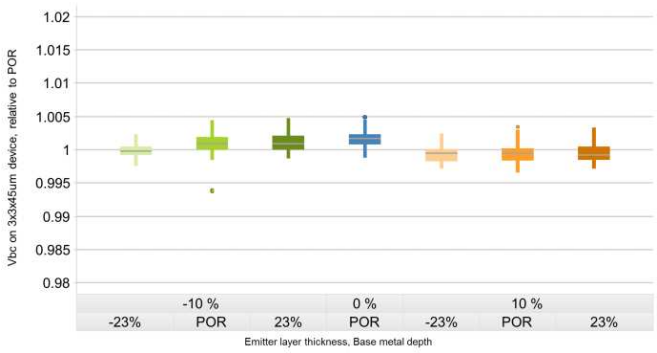

Figure 4: Base collector turn on voltage over process margin variants.

DATA INTERPRETATION

In each process margin study, the slope ΔPCM / Δprocess input of PCM parameter vs. process variable was calculated from a linear curve fit. Figure 5 shows the example of emitter-base breakdown vs. emitter layer thickness. Separately, the process input $1\sigma_{process}$ has been characterized. For example, $1\sigma_{process}$ could be a layer thickness, etch time, or metal deposition thickness. The projected PCM variation due to process input variation is

$$\sigma_{projected} = [1\sigma_{process}] \cdot [\Delta PCM / \Delta process\ input]$$

To benchmark sources of variation before production begins, the margin figure of merit is used:

$$\text{Margin FOM} = [\sigma_{projected}/\sigma_{parametric}]$$

In this connection, $\sigma_{parametric}$ is the observed parametric 1σ based on the prior production HBT process. This value was calculated for over 40 parameters measured in DC and RF test.

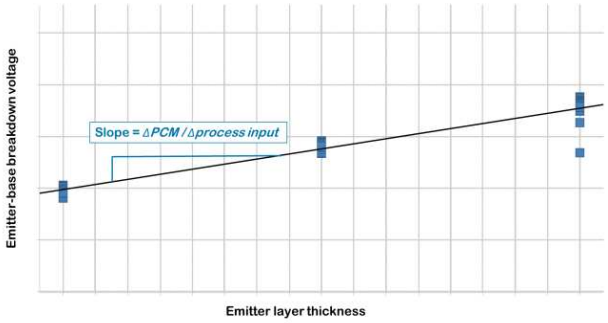

Figure 5: Example of how emitter-base breakdown changed with emitter layer thickness in the process margin study.

While Cpk or process capability to specification limits is also a useful metric, for new processes there may not be enough data to evaluate process variation correctly. Additionally, because the Cpk calculation depends on the specification limits, for PCM parameters Cpk isn't the best way to compare sources of variation in margin studies. For these reasons, the margin FOM is a better way to compare process variation from multiple process margin studies at the time of process release than using Cpk.

Table 1 shows the margin FOM for each PCM parameter correlated to either emitter layer thickness or base metal alloy depth.

Device measurement	**InGaP thickness**	**Base metal alloy depth**
Beta at 1kA/cm2	5%	0%
Emitter-base leakage	2%	0%
Emitter-base BV	66%	0%
Cbe on large area device, 0V	127%	0%
Re on small device	9%	0%
Base contact resistance	0%	2%
Δβ(10kA/cm2-1kA/cm2)	0%	0%
Δβ(1kA/cm2-0.3kA/cm2)	7%	0%
fMax on RF device	7%	0%
Small signal gain, RF device, 8GHz	10%	5%
Cbe on RF device at Vc=0, Vb=0	2%	0%
Cbe on RF device at Vc=5V, Ic= 12mA	1%	0%

Table 1: $[\sigma_{projected}/\sigma_{parametric}]$ for all parameters found to correlate to either emitter layer thickness or to base metal alloy depth.

Table 1 has a few noteworthy conclusions. First, Cbe variation is shown to be strongly related to emitter layer thickness variation, which is well-known. In this case, the projected total process variation due to assumed emitter layer thickness variation exceeds the observed parametric variation so margin FOM > 100%. Measurement error in the layer thickness variation or in the correlation between Cbe and layer thickness are likely contributing factors. However, the exact value of the margin FOM is not what matters; the relative value can still be used to rank probable causes of variation. Emitter layer thickness clearly drives large area device Cbe. In contrast, Cbe measured at RF test after process completion does not correlate strongly to emitter layer thickness. Cbe RF measurements are performed at wafer level on much smaller devices. The process margin study clearly reveals that the RF device variation is nearly independent of emitter layer thickness variation. Following Cbe, in Table 1 the next strongest DC performance variation correlation is emitter-base breakdown voltage, which is also well-known. However, InGaP layer thickness does impact other device measurements that correlate to RF performance, namely Re, Fmax and gain.

By contrast, few device measurements are predicted to vary in production with normal base metal alloy depth variation. In this study, only base metal contact resistance and small-signal gain were impacted, and then only weakly. Base alloy metal depth sensitivity is greatly improved over the prior process generation.

In practice, after all margin studies were compared, margin FOM had to be at least 20% to warrant further action. In several cases, strong correlations between process input and device variables were found, but the strong correlation didn't necessarily translate into a high value of margin FOM. For example, emitter-base leakage was clearly dependent on emitter layer thickness when the thickness was changed well beyond +/-3σ as shown in Figure 2. However, the actual variation in layer thickness and in the production emitter-base leakage distribution show that the emitter layer thickness is not the root cause for leakage variation.

After the process margin studies were completed, further actions to drive down important causes of variation were taken. For epi process inputs like layer thickness and doping, the process control from the epi supplier was already very good. A few parameters needed uniformity or reproducibility improvements, but for those parameters that did, the epi suppliers were able to tune process uniformity. While process control improvements are usually not free, they are more easily justified with margin study data. For fab process parameters, further DOEs to map the process space were used to find an appropriate process center to drive down variation.

CONCLUSIONS

Process margin studies can often be performed for individual unit processes in a complex process flow like Qorvo's next generation HBT. However, to compare sources of variation, process cross-terms and uniform metrics are needed. This paper covered one such methodology for releasing new production flows rapidly and with high initial yields. The key metric for comparing process input impacts on device performance variation is margin FOM = $[\sigma_{projected}/\sigma_{parametric}]$, which can be used to rank-order process inputs needing further work to drive down variation.

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REFERENCES

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
PCM: process control monitor, refers to standard inline device testing on large area and RF devices
FOM: figure of merit
PAE: power added efficiency
Cbe: base-emitter capacitance