High Aspect Ratio Individual Source Through Wafer Vias for High Frequency GaAs pHEMT Processes

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ABSTRACT

Through wafer via holes play a major role for the III/V – semiconductor electronics. The GaAs etch processes for these high aspect ratio structures are well understood and applied. However, the benefits of a slot via configuration for source connections of high power and high gain pHEMT processes for high frequencies lead to a performance improvement of the transistor by significantly reducing the source inductance. In this work, the process characterization of dry chemical via hole etching in GaAs including via slope and aspect ratio limitations are discussed. Benefits of the perpendicular via hole process will be compared to a tapered one regarding process stability and integration. The electrical characterization of the via holes, as well as the performance of a 150nm pHEMT power process will be shown. Hereby, the inductance has been extracted from S-parameter measurements on via hole modeling structures, as well as on the new process technology PPH15X-20 of UMS.

WEAKNESS OF TAPERED VS PERPENDICULAR VIA PROCESS

The via hole etching in GaAs is performed on temporary bonded and thinned wafers on sapphire carrier wafers. The chlorine dry etch of GaAs is mainly chemically driven. In order to get reproducible quality of via holes in GaAs, the chamber conditioning is very important. The selectivity of GaAs to resist plays a major role for the process stability. Furthermore, the via holes are defined by profile, sidewall roughness and the presence of micro masking defects inside the via hole. In the case of a tapered via hole process, the GaAs wafer surface, resist stability, resist slope and the pre cleaning steps before chlorine etching have to be understood and reproducible. The control of all these process steps in a production environment takes significant effort. By implementing a process with a perpendicular resist profile for via holes, both the GaAs surface after grinding and the requirement for the resist reflow for the tapered via can be ignored. Furthermore, the size of via patterns adapted to the MMIC design can be varied for a perpendicular via approach. The tapered via hole process has to be optimized for one via pattern and size.

OPTIMIZATION OF RESIST MASK

The success of a GaAs via hole process depends strongly on the requirements of the resist softmask process. In order to withstand the chlorine plasma etch chemistry in the ICP etching tool, the resist slope should not show any deformation during the plasma etch process. Usually, a post development bake is applied in order to get the resist stable for the following dry chemical etching. Unfortunately, the bake changes the resist slope and the result would be a rounded resist profile that does not meet the required profile in the post etch GaAs. Therefore, another technique for resist stabilization is applied. The resist stabilization after development is done before the GaAs etching step insitu in the ICP etch tool. A fluorine based insitu pre treatment before the Cl etch step builds a thin PTFE (Polytetrafluoroethylene) layer that stabilizes the resist slope. This technique is called the PRIST method (Photo Resist Image Stabilization Technique) [2]. In this work a CF_4 ICP plasma is applied for the resist polymerization. However, CHF_3 or SF_6 gases can also be used. The insitu PRIST step is performed at 20 mTorr pressure and moderate ICP power with no platen RF power for 2 minutes. In order to get effective polymerization the bias to the wafer has to be as low as possible. Furthermore, it is worth noting that the ratio between resist volume and applied temperature after the resist stabilization has to be taken into account. This means, that with an increasing resist thickness the polymerized layer may not be strong enough to keep the resist stable. In this work we showed that a resist slope of 78° of a 19µm thick resist remains constant up to a bake temperature of 140°C for 5min. on a PRIST plasma treated wafer.

GAAS ETCHING PROCESS CHARACTERIZATION

The through wafer vias in GaAs are etched in an ICP etch system with a chlorine based chemistry. The requirements for the via etch are high etch rate of GaAs with high selectivity to the resist mask. The above mentioned resist thickness is limited because of the working principle of the resist stabilization technique(PRIST). Depending on length and width of the slot vias there is a RIE lag effect.

Due to this, a slot via structure depicted in Figure 1 is applied for etch process characterization. The etch process is developed and optimized for 70um thick wafers.

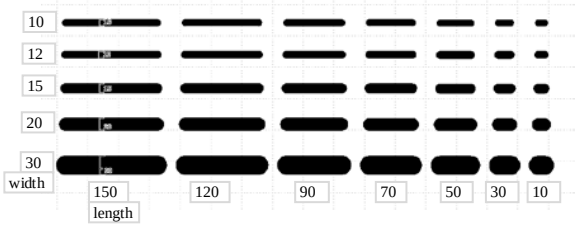

Figure 1 - Slot via etch pattern for plasma process characterization (all values in µm)

During the etch process characterization, optical defects like via hole fraying, grass formation and side wall attack occurred depending on the process parameters including pressure, platen RF power and etch time. The fraying effect is an under etching of the resist mask with an etching of the upper via hole slope. This effect can be seen at high pressure, low platen RF power and high gas flow. The fraying begins after approximately 15min of etch time. It is assumed to be an effect of high selectivity. This leads to low resist consumption, and therefore, to high surface tension of the resist at the end of the narrow slots causing resist delamination (Figure 2).

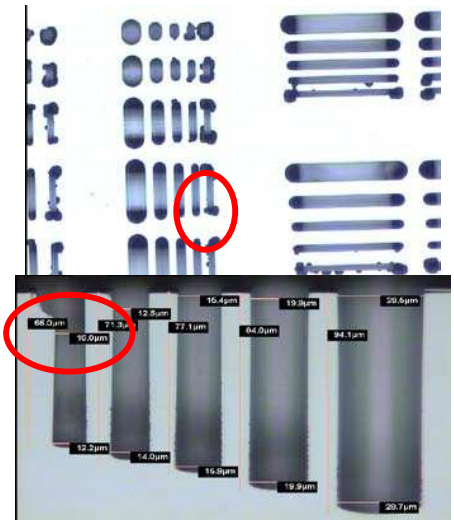

Figure 2 – Fraying of slot via holes of 10 µm width

The side wall quality is defined by the stability of the side wall passivation. Figure 3, picture a) shows a side wall with no etch attack and picture b) a via hole with an attacked side wall passivation layer. By analyzing the data the etch selectivity of GaAs to resist plays a major role for the side wall quality. An etch selectivity greater than 9 shows that the side wall passivation is strongly attacked by the dry etch chemistry.


a)

b)

Figure 3: Characterzation of side wall quality depending on low a) and high b) pressure and bottom power

Table 1 describes the impact of the process parameters on the optical defects and the process characteristics.

	trend	fraying	grass	side wall quality	GaAs etch rate	resist etch rate	selectivity
pressure	↑	↑	↓	↑	↑	No impact	↑
bottom power	↑	↓	↑	↓	No impact	↑	↓
etch time	↑	↑	NA	↓	↓	No impact	↓
slot width	↓	↑	No impact	↓	↓	No impact	↓
slot length	↓	↑		NA	↓		↓

Table 1 – Process characteristics depending on process parameters

The stability of the side wall passivation strongly impacts the via hole profile. To quantify this phenomenon, we introduced the VH form factor that describes the tapering or broadening of the slot via holes (Figure 4). The lower the width of the slot the smaller the form factor will be. A positive or negative form factor describes a tapering or a broadening of the slot via, respectively. Process pressure and platen RF power are optimized for getting a VH form factor greater or equal to 0. The VH form factor strongly depends on the slot via width. At a slot via width of 10 and 12 µm the results show factors equal or less than 0.

$$VH\ form\ factor = \frac{x - y}{x}$$

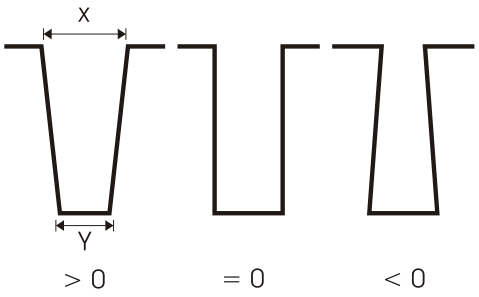

Figure 4 – VH form factor definition x = cd at top y = cd at bottom of via

After the characterization of the profile and optical quality of the vias, the etch rate depending on the aspect ratio and etch time was plotted for the process in Figure 6. The aspect ratio is the via depth of 100µm divided by the slot via width.

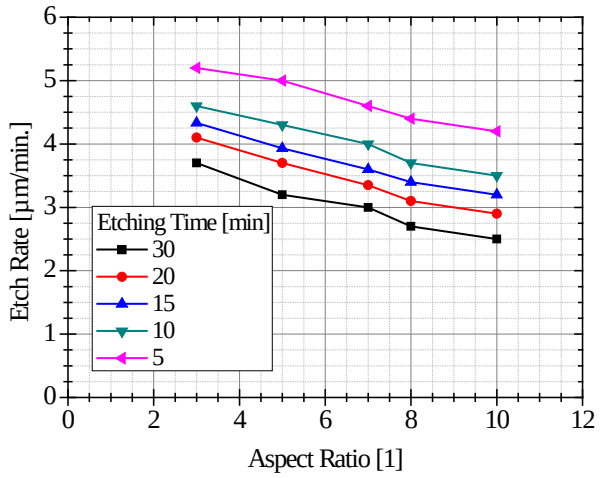

Figure 6 – GaAs etch rate of slot via patterns depending on aspect ratio and etch time

Finally, the restriction for the slot via length is determined by a cross section of the target process through the 15µm wide via chain (Figure 7). The result is good via hole quality in terms of optical defects and a constant GaAs etch rate for a slot via length of greater than 50 µm and an aspect ratio of less than 7. The etch rate depending on slot length may not deviate more than 10%.

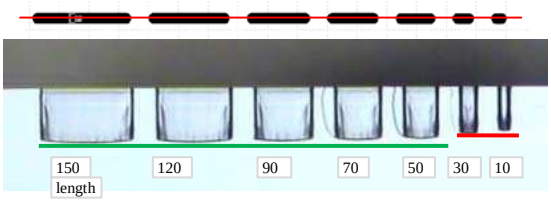

Figure 7 – Cross section along the slot via holes at a width of 15µm – constant etch depth at slot width greater than 50um

METAL CONFORMITY INSIDE SLOT VIA

The next step in the process flow is the seed layer deposition for the thick electroplated back side Au metal. The metal conformity is checked by cross section through a 70 µm long slot via chain of 15µm width. Figure 8 shows the cross section of the perpendicular slot via compared to the tapered circular via holes of 30 µm in diameter.

The measurement of the Au conformity is defined as the Au thickness on the via side wall at the lower part of the via hole divided by the Au thickness on the wafer back side. The metal conformity of tapered vias result in around 0.5 compared to the slot vias of 0.6. The reduced roughness of the via side wall improves the metal conformity of the electroplating process. This can be explained by the enforced reaction of the plating solution on the rough GaAs via side wall at the via top region.

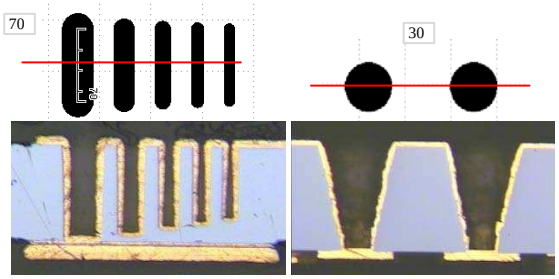

Figure 8 – Metal conformity in slot via holes of 70µm in length a) compared to tapered vias of 30µm in diameter b)

ELECTRICAL CHARACTERZATION

At the end of the back side process after the de bonding of the wafer from the sapphire, the electrical contact resistance is measured. Figure 9 shows the normalized electrical contact resistance map of a perpendicular via hole of 30 µm in diameter compared to the electrical contact resistance of the tapered 20 µm via hole for a 70 µm thick wafer. The contact resistance of the tapered via shows a non uniformity of around 26% compared to the perpendicular one of 8%. This can be explained by the impact of the metal conformity variation inside the via hole depending on variation of via slope and side wall roughness on the wafer.

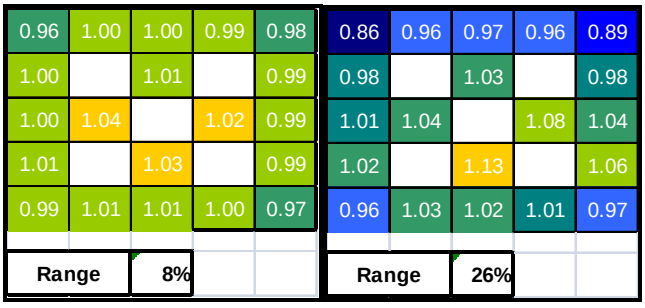

Figure 9 – Via contact resistance mapping of perpendicular a) and tapered via holes b) of a 70µm thick wafer

S-parameters have been measured up to 40 GHz on a test vehicle shown in Figure 10. The test is performed with a de-embedding of the feed lines to the via contact.

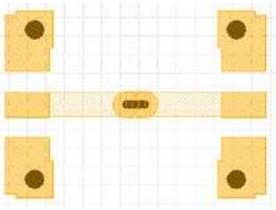

Figure 10 – Test vehicle for S-parameter measurement up to 40 GHz and via inductance extraction

The inductance is extracted from S-paramater measurements of different test patterns by varying slot width and length and circular vias with different diameters. The inductance is plotted versus the circumference of the via. The chart in Figure 11 shows a clear impact of the circumference of the via pattern, the wafer thickness and the via slope on the via inductance. The circular or slot via patterns show no impact on via inductance.

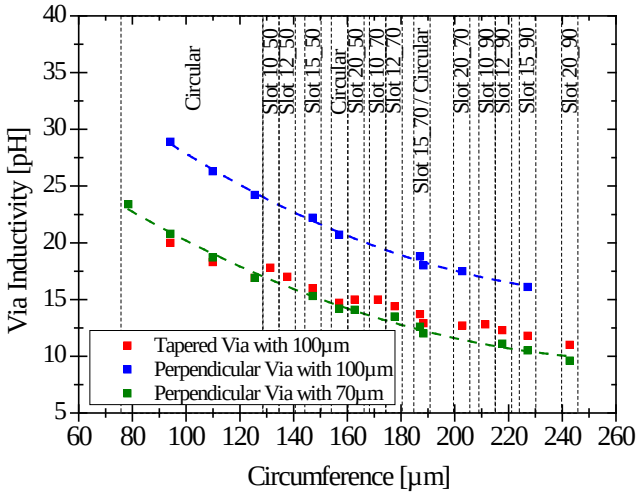

Figure 11 – Extracted inductance from S-parameter measurements up to 40GHz (slot_width_length)

For the same circumference, the implementation of a perpendicular slot via approach for the PPH15X-20 process technology shows no difference or drawbacks to the gain performance compared to tapered vias. However, due to the slot pattern, the gate pitch can be reduced in order to optimize the transistor cell size.

Conversely, for the same gate pitch, the circumference can be increased which results in a reduction of the inductance by maximum of 10pH.

CONCLUSION

This work shows a detailed integration and evaluation of a process concept in a compound semiconductor manufacturing process. The use of slot vias introduces an additional degree of freedom for power transistor design that reduces the gate pitch for the same inductance, or the inductance for the same pitch. Additionally, the implementation of perpendicular slot vias results in a more reproducible via hole etch process. The methodologies used in this process development are a good example of process integration in the compound semiconductor industry.

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ACRONYMS

ICP: Inductive Coupled Plasma
RF: Radio Frequency