An Integration of On-Chip High-Q Inductors by Cu Redistribution Layer (RDL) with Bumping for InGaP/GaAs HBT MMIC

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Abstract

InGaP/GaAs HBTs have been widely used in power amplifier (PA) design for wireless communications because of their high linearity and high efficiency. To fulfill the demand of portable devices in recent years, high functionality of a power amplifier across various applications and frequency bands is required. Chip size becomes a critical part of a PA products ability to reduce package size. High integration density of power amplifiers can be obtained using a Cu redistribution layer (RDL) to achieve a stacked structure for more layout flexibility. An on-chip high-Q inductor not only saves space on the module board, but it also minimizes the power loss at the same time. This work presents a 30% Q factor improvement and a 23% MMIC die size reduction by utilizing a RDL process with Cu pillar bumps.

INTRODUCTION

The high integration of a RF front-end module is becoming a trend to fulfill the multiple functionality needs of a smart phone. Not only to eliminate the signal loss, but also to increase the density of a single package. Therefore, the 3D packaging techniques have recently been developed [1]. Specifically examining the GaAs MMIC; an on-chip high Q inductor becomes a popular solution to simultaneously achieve lower power loss and smaller chip size.

This work presents an integrated GaAs HBT MMIC by implementing a copper redistribution layer process with bumps. The quality factor comparison between a conventional back-end-of -line inductor process and a high Q inductor by Cu redistribution layer is shown.

DEVICE FABRICATION AND FEATURES

This work was done with WIN's 4th generation InGaP/GaAs HBT process [2], [3]. The 4th generation HBT process, so called HBT4, includes two interconnection metal layers (M1and M2) and a thick SiN layer as the dielectric layer between M1 and M2. Using a thick SiN film instead of using Polyimide as an interlayer dielectric can provide better mechanical and moisture protection. The thicknesses of the Au metal interconnect layers are 1um evaporated and 4 um plated for M1 and M2, respectively. MIM capacitors with unit capacitance of 570 pF/mm^2, stacked MIM capacitors with unit capacitance of 870 pF/mm2, and thin film resistors with sheet resistance of 50 Ohm/sq can be used for MMIC designs.

Fig. 1 shows a typical cross-section of a GaAs MMIC with Cu redistribution layer. After the standard HBT4 front-end process is finished, a low-k material is then spin-coated onto the SiN protection layer. The thickness of this low-k material layer is 10um which is discussed in previous work [4]. Low-k material is used as the dielectric polymer to minimize the interaction by the Cu re-distribution metal layer and components underneath. It also allows the RDL to re-route the signal path from the original I/O on top of a 10um dielectric layer.

Using the low-k material, via-holes are directly patterned on the low-k material by optical lithography for establishing electrical contacts with the MMIC. The Cu RDL, which has a thickness of 8um, is fabricated by electroplating. A second low-k material layer is then deposited to passivate the Cu RDL. Lastly, the copper pillar bump process provides 40um of plated copper and 25um of plated Sn cap metal for flip-chip mounting utilizing a solder reflow process.

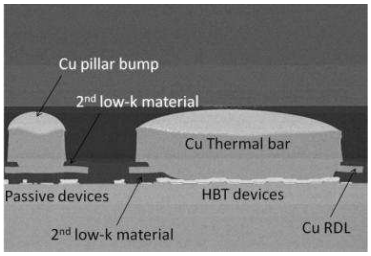

Fig. 1 Device cross-section composed of a MMIC, low-k isolation layer, and RDL metal layer with Cu pillar bump.

DESIGN OF COPPER RDL METAL LAYER

To determine the thickness of Cu RDL metal layer, the process limitation and electrical performance needs to be taken into consideration. Compared to a Silicon substrate, GaAs has superior resistivity minimizing the substrate loss for a better quality factor of an on-chip inductor. However, the inductor performance is still mainly dominated the by skin effect [5]. This work adopts a 10um low-k dielectric layer for minimizing inductor interaction and then optimizes the Cu RDL metal thickness by ADS EM simulator. In the EM simulation, a 4-turn square inductor with a coil width of 10um, inductor spacing of 10um, and inner core diameter of 60um with various metal thickness is analyzed.

EM simulations at 0.9GHz and 5.8GHz are presented in Fig. 2. When the frequency is 0.9GHz, the Q factor is improved simultaneously while increasing the Cu RDL metal thickness. In contrast, when the frequency is higher at 5.8GHz, the Q factor degrades while increasing the thickness, which is dominated by the skin effect. Results indicate an optimal inductor thickness depends on the specific application. In this work, due to the process limitations, an 8um Cu RDL metal thickness is chosen for the final thickness.

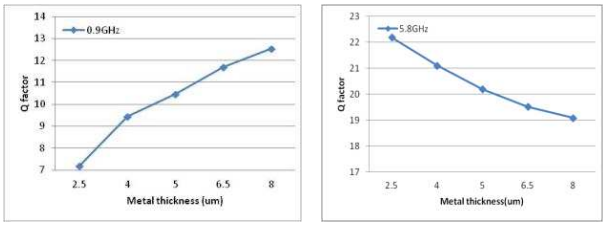

Fig. 2 Q factor simulation results of various RDL metal thicknesses. (Left: frequency at 0.9GHz; Right: frequency at 5.8GHz)

MEASURING METHODS AND DEVICE TEST STRUCTURE

In this study, the devices were measured(DC & Small Signal) on the front-side using a G-S-G microwave probe with a co-planar waveguide pad. Fig. 3 shows a typical test structure of a 2-turn square inductor for characteristic extraction. Fig. 4 shows a typical test structure of a HBT power cell device consisting of 4 sets of unit cells. Each unit cell is composed of three 3um by 40um emitter fingers.

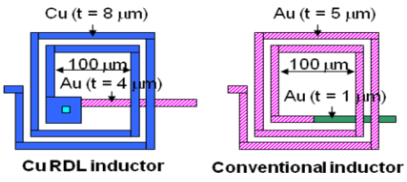

Fig. 3 Illustration of both a conventional inductor and a Cu RDL inductor. Inductor thickness of a Cu RDL and a conventional inductor are 8um and 5um, respectively.

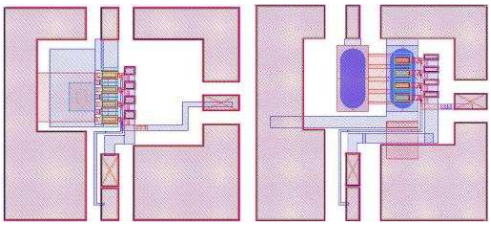

Fig. 4 Illustration of a HBT power cell test structure for a conventional through wafer via with direct Cu pillar bumps, and a RDL with Cu pillar bumps.

INDUCTOR PERFORMANCE AND HBT I-V CHARACTERISTIC

Fig. 5 shows a 2-turn square inductor comparison between measured and simulated results. The simulated results are well matched with measured results for both inductance and quality factor. An on-chip high Q inductor formed by an 8um Cu RDL layer demonstrates a better Q factor than a conventional inductor across frequency. Table 1 shows greater than 30% improvement in quality factor for the same inductor size at 2GHz.

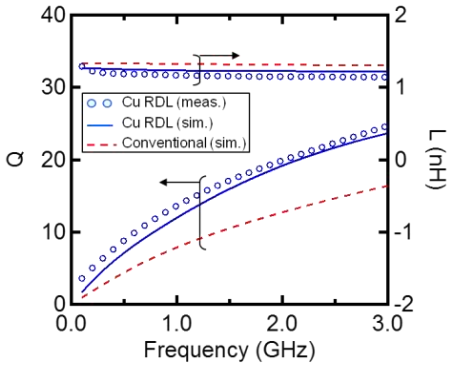

Fig. 5 Comparison of quality factor between a conventional inductor and a Cu RDL inductor. The Cu RDL inductor exhibits a higher Q-factor.

Table 1 Comparison of quality factor between a conventional inductor and a Cu RDL inductor.

Device	Q-factor@2GHz	Q-factor@3GHz
RDL inductor	19	23.5
Conventional Inductor	13	16.5

In comparison to a traditional through wafer via device, having a copper bump directly on top of the emitter electrode exhibits excellent thermal dissipation which leads to better current handling and performance of a HBT device as shown previously [6]. In this work, an additional copper re-distribution metal layer demonstrates a superior improvement in thermal dissipation of the HBT as shown by I-V curves in Fig. 6. At Ib=5mA, Vcc=3.4V, the DC beta value of the traditional through wafer via device and the RDL with Cu pillar bump device are 59 and 70, respectively.

This result indicates that the thermal resistance (Rth) of the RDL process with bumps is significantly improved.

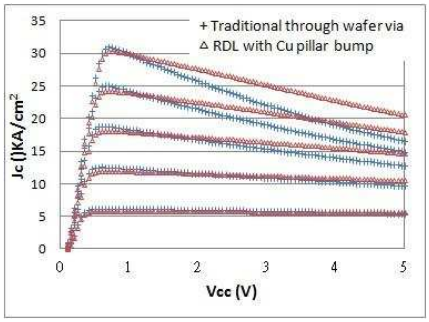

Fig. 6 Comparison of I-V characteristics among traditional through wafer via direct Cu pillar bump, and Cu RDL bump devices. The device using a Cu RDL shows the best thermal dissipation characteristics.

MMIC CHIP SIZE REDUCTION DEMONSTRATION

Fig. 7 shows a chip size comparison between WIN's standard HBT4 process and a Cu RDL process using a 1000um*1000um two stage MMIC as a reference. This work enables a 23% MMIC die size reduction by implementing the Cu RDL process with bumps as shown in Table 2. With the Cu RDL process, the original bond pad size can be minimized and re-routed by the Cu re-distribution layer on top of the 10um dielectric layer. Combining a high-Q Cu RDL inductor with Cu pillar bumps enables higher density power amplifiers and further reduces footprint on a module board.

Fig. 8 shows a Scanning Electron Microscope (SEM) image of a MMIC using WIN's standard HBT4 process with a Cu redistribution process with Cu pillar bumps.

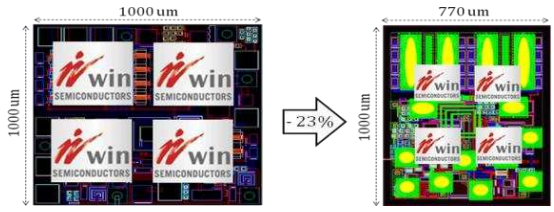

Fig. 7 MMIC layout example of chip size reduction by implementing a Cu RDL process.

Table 2 Comparison of MMIC area.

Device	Width	Length	Total area
Traditional TWV MMIC	1000um	1000um	1 mm^2
Cu RDL MMIC	770um	1000um	0.77 mm^2

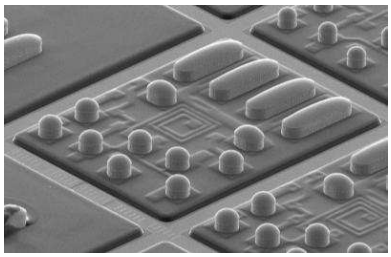

Fig. 8 Device surface morphology of a MMIC using a Cu redistribution layer with Cu pillar bump process.

CONCLUSIONS

In conclusion, this work demonstrates a Cu redistribution layer process integrated with WIN's standard HBT4 process on GaAs MMICs. An 8um thick on-chip high Q inductor shows 30% improvement in quality factor as compared to a standard inductor. While achieving approximately a 23% MMIC chip size reduction, this proposed process provides better thermal dissipation, smaller chip size, and a highly integrated an on-chip high Q inductor.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
MMIC: Monolithic microwave integrated circuits
RDL: Redistribution layer
SEM: Scanning Electron Microscope