Packaging Trends in the Wireless Industry

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Abstract

The primary drivers for packaging technology development in the wireless industry are performance, size, cost, and time-to-market. There is continuous market pressure to drive improvements in each of these areas at both the component level and the module level. In contrast, there is a constant requirement to maintain standards for high quality product, which requires extensive reliability testing and tends to extend development timelines. This presentation will highlight the challenges and potential solutions in implementing packaging improvements in a short time-to-market environment.

INTRODUCTION

Wireless device content continues to expand in a wide range of consumer products. RF functionality and band proliferation are increasing, yet the end product requirements demand smaller, thinner modules. Materials and geometries are prime determinants of meeting RF specifications like gain, isolation, linearity, impedance matching, etc. While working to shrink dimensions and lower cost, RF characteristics can shift dramatically. Hence, modeling and empirical validation take on an increased level of urgency during the module development cycle. This paper highlights key wireless packaging trends in electrical performance improvement, size reduction, time-to-market acceleration, and cost reduction.

ELECTRICAL PERFORMANCE IMPROVEMENT

Electrical performance improvements are being achieved through 1) higher Q inductors and capacitors, 2) tighter specifications on filters and duplexers, 3) integration of EMI shielding, and 4) lower inductance flip chip interconnects.

Shown in Figures 1 to 3 are Q factor performance data for inductors and capacitors at 1GHz frequency. Higher performance specifications at the module level drive component selection movement from Standard Q to High Q or Mega High Q categories. The challenge for suppliers is to manufacture the higher performance components near cost parity with standard components. This is especially difficult for smaller form factor components, so module designers are continuously working the cost-performance tradeoff.

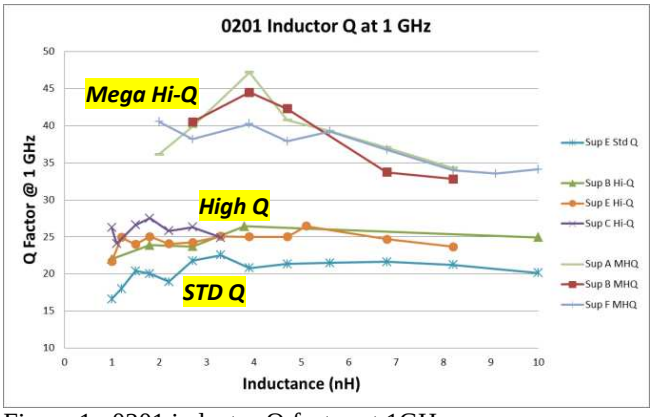

Figure 1. 0201 inductor Q factor at 1GHz.

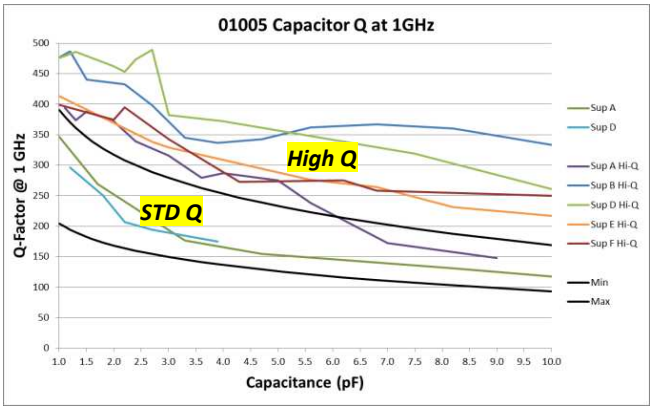

Figure 2. 01005 capacitor Q factor at 1GHz.

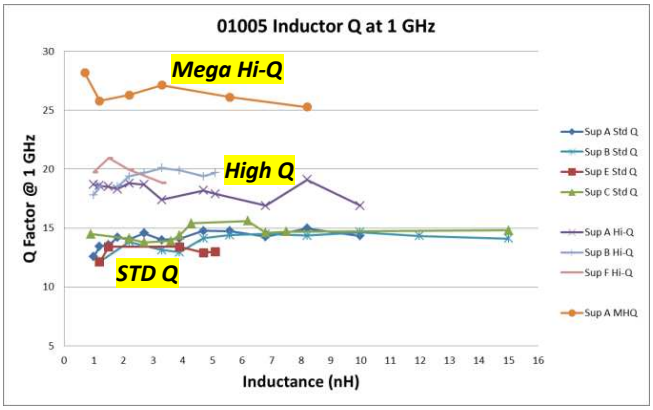

Figure 3. 01005 inductor Q factor at 1 GHz.

SAW, BAW, and FBAR filters and duplexers have become the most critical passive components in many RF modules due to their relatively large size and high proportion of the total BOM cost. Band proliferation at the module level and product level drives tighter specifications on the filters and duplexers. Hence, the general trends are moving from standard SAW to temperature compensated SAW, BAW, and FBAR. BAW and FBAR are the preferred solutions in the highest frequency bands.

Module level EMI shielding is becoming a requirement for many applications. The shielding might be used to suppress either outbound radiation or inbound radiation. In some cases, intra-module shielding is required to reduce interference between adjacent sections of a device. Shown in Figure 4 are measured near field radiation patterns before and after application of module level EMI shielding. A 15 to 30 dB reduction in radiated energy is generally achievable.

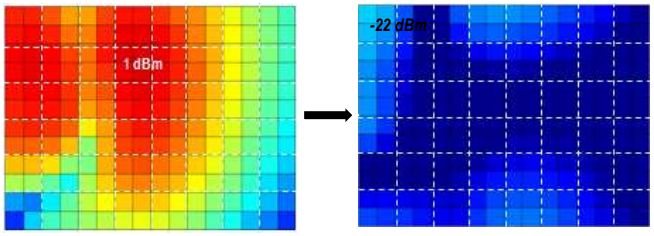

Figure 4. Radiated energy before and after application of module level EMI shielding.

Flip chip interconnects are increasingly being used in RF modules. At high current density and high temperature, diffusion and intermetallic compound reactions can lead to failure as shown in Figure 5 [1]. Smaller UBM diameters are required as bump pitch is reduced. This can result in higher current density, and more rapid electromigration failure. Improvements in performance can be achieved by moving to Ni UBM or copper pillar structures [1].

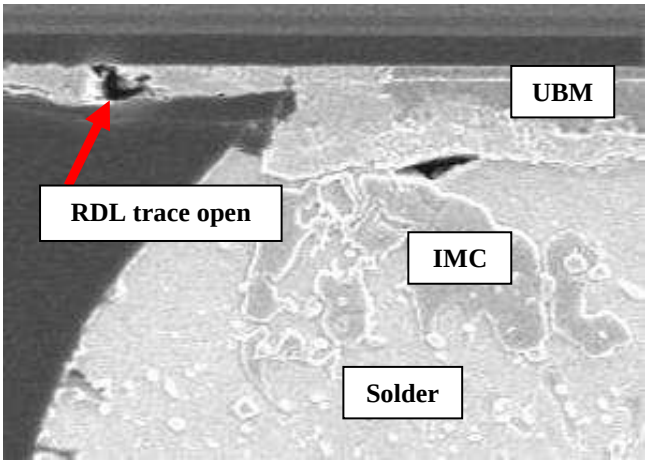

Figure 5. Example of electromigration failure in flip chip solder joint.

SIZE REDUCTION

Size reduction is being achieved through 1) smaller passive components, 2) tighter spacing between components, 3) thinner substrates, 4) stacked die, 5) thinner mold caps, and 6) conversion to WLCSP. All of these size advancements push the assembly process to more aggressive design rules and advanced materials. Embedding components and cavity structures are also being evaluated.

Filter and Duplexer area and thickness trends are shown in Figures 6 and 7. As the filter content continues to increase in RF modules, the pressure to reduce area becomes more severe. Overall product thickness reduction trends likewise drive a parallel trend in filter thickness reduction.

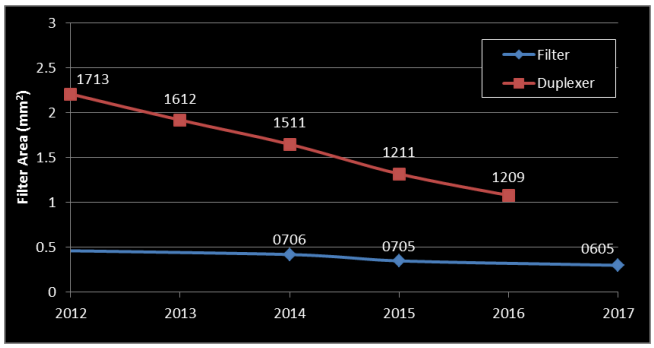

Figure 6. Filter and duplexer area roadmap

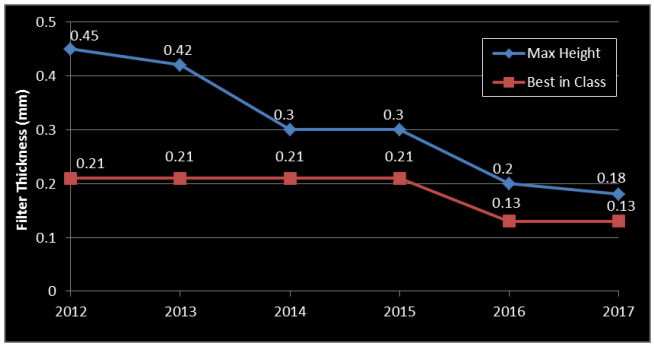

Figure 7. Filter and duplexer thickness roadmap.

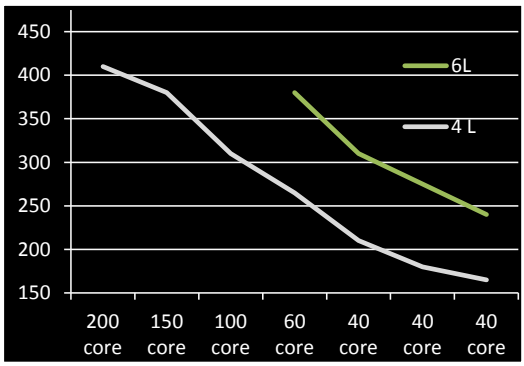

Figure 8. Laminate substrate thickness (um) roadmap.

The majority of RF modules use a 4-layer or 6-layer laminate PCB substrate. Shown in Figure 8 are the laminate substrate thickness trends. Core thicknesses have reduced from 100µm down to 40µm over the past several years. Further substrate reductions are achieved by reducing copper layer and dielectric layer thicknesses. In addition, coreless substrates have become main stream in RF applications, and they typically come in 3-, 5-, and 7-layer stack ups.

Module substrates are processed through the packaging assembly line as part of a larger strip. A primary challenge in reducing substrate thickness is to maintain relatively flat strips. Thermal excursions through the various process steps can warp the substrate and cause equipment jamming issues and yield loss. Methods to counteract substrate warpage include balancing metal content in the various layers, material selection, and the use of strip carriers.

Another method to reduce module area is through die stacking, as shown in Figures 9 and 10. A significant development effort is applied to continuously improving design rules which enable thinner and smaller die stacks. The most important process optimization is required in back grinding, die attach, wire bonding, and molding.

IPDs are now mainstream in several products, with the primary benefit of size reduction over circuits using discrete passive elements. Another advantage in IPDs is that they can be stacked with active die in the same manor shown in Figures 9 and 10. Development in IPDs includes increasing the layer count, increasing the metal and dielectric thicknesses, and adding through vias to enable flip chip-on-flip chip stacking.

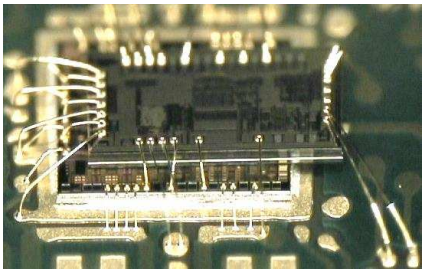

Figure 9. Stacked wire bond dies.

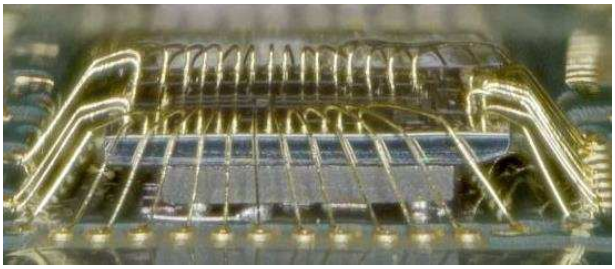

Figure 10. Stacked flip chip + wire bond dies.

COST REDUCTION

Overriding all this development activity is a constant drive for cost reduction. Conversion from gold wire to copper wire is well advanced. Copper wire bonding results in a significant material cost reduction over gold wire bonding. However, the process overhead cost is higher due to reduced throughput and equipment up time. Small bond pad openings on the die are also more challenging for copper wire bond applications.

Simplified process flows and improved equipment throughput are consistent themes throughout the manufacturing line. Other opportunities for cost reduction include saw street reduction, improved substrate panel utilization, and lower cost material sets.

REDUCTION IN TIME-TO-MARKET

Time-to-market reductions are being achieved through 1) quick turn material delivery, assembly, and test, 2) improved component models, and 3) more use of finite element analysis to design packages and solve quality issues.

A thermal simulation example is shown in Figure 11. Once simulation capability is calibrated to measured results, a very efficient design optimization cycle can be achieved.

One of the challenges to reducing time-to-market is the constant requirement to maintain standards for high quality product. Extensive reliability testing tends to extend development timelines. A serial flow of qualifying materials and components => processes => modules => end product has become unmanageable. More activities need to be done in parallel, and shorter duration reliability tests need to be utilized where possible.

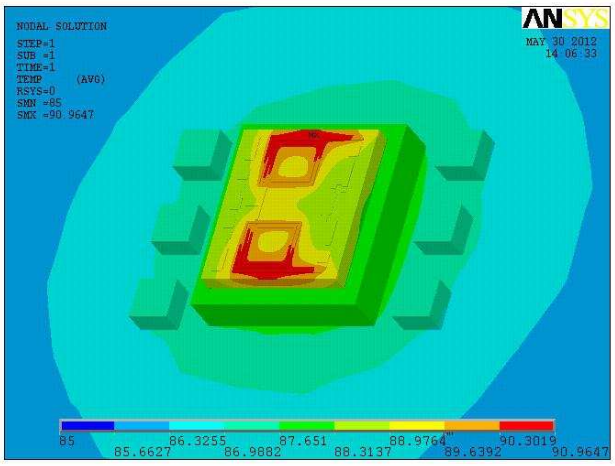

Figure 11. Thermal simulation result for QFN package.

CONCLUSIONS

Packaging trends in the wireless industry were discussed. Today's development is primarily focused on electrical performance improvement, size reduction, cost reduction, and accelerated time-to-market. Critical issues and potential solution areas were highlighted.

ACKNOWLEDGEMENTS

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REFERENCES

[1] R. Darveaux, J-D V Hoang, B. Vijayakumar, "Electromigration Performance of WLCSP Solder Joints," Proc. SMTAI 2014.

ACRONYMS

BAW: Bulk Acoustic Wave
BOM: Bill of Materials
EMI: Electromagnetic Interference
FBAR: Film Bulk Acoustic Resonator
IMC: Intermetallic Compound
IPD: Integrated Passive Device
PCB: Printed Circuit Board
RDL: Redistribution Layer
SAW: Surface Acoustic Wave
UBM: Under Bump Metallurgy