RF Performance Improvement of 0.25µm GaN HEMT Foundry Technology

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Abstract— In this paper, we present RF performance improvement of 0.25µm GaN HEMT technology. The optimization of the 1st SiN passivation pretreatment enhanced the gain by 1.3dB from 1GHz through X-band. The development and implementation of a slot via design enables source via connections to be made to the internal transistor. This development extended the K=1, MAG/MSG curve breakpoint to higher frequencies and into the Ku-band.

Keywords: AlGaN/GaN, X-band, backside via, slot via

INTRODUCTION

Excellent RF device and good reliability performance of AlGaN/GaN HEMTs has been demonstrated by many companies in the world [1~2]. WIN Semiconductors is leveraging our experience in GaAs pHEMTs, HBTs and BiHEMTs and is developing AlGaN/GaN HEMTs to broaden WIN Semiconductors' foundry services portfolio driven by our customer interests and needs. WIN is a pure play foundry with a mission to provide our customers Foundry services with the best yield and cycle time. In 2013, WIN demonstrated our first 0.25µm GaN technology with good performance in the X-band and thereafter a program to develop high volume production capability in terms of yield and cycle time is being executed at WIN Semiconductors in parallel with a program to improve the 0.25µm GaN technology performance in the Ku-band.

Two methods of improving the RF performance in GaN-based devices are presented in terms of an optimized 1st SiN dielectric passivation pretreatment and slot via process. Since the 2DEG of the GaN HEMT channel is formed by spontaneous and piezoelectric polarization, it is important to keep a repeatable and stable dielectric-to-semiconductor surface condition during the process. The production of 0.25µm GaN HEMTs has recently been undertaken by a handful of companies in an effort to provide technology to address not only L-, S-, and C-band applications but also X- and Ku-band. To enable good performance in the Ku-band a backside slot via technology was developed effectively increasing the maximum available gain performance.

I. PROCESS OPTIMIZATION

The pretreatment process prior to 1st SiN passivation plays an important role in the front-side process. During high voltage operation, the interface between the 1st SiN passivation and the AlGaN surface can be changed due to the high electric field imposed on gate-drain surface which can induce reliability issues. In order to achieve low gate leakage current, stable cut-off frequency and high gain performance the surface pretreatment needs to be carefully optimized.

The condition A (with O_2 plasma) and B (without O_2 plasma) pretreatment process prior to 1st SiN passivation is shown in Table 1. The surface states between the 1st SiN passivation and the AlGaN interface were characterized by pulsed I-V measurement as shown in Fig.1. Condition B showed a relatively lower drain current degradation and RF dispersion which indicates there may be less trapping underneath the 1st SiN passivation compared to condition A.

TABLE I
Condition A (with O_2 plasma) and condition B (without O_2 plasma) pretreatment prior to 1st SiN passivation.

Process	Pretreatment
with O2 plasma	A
without O2 Plasma	B

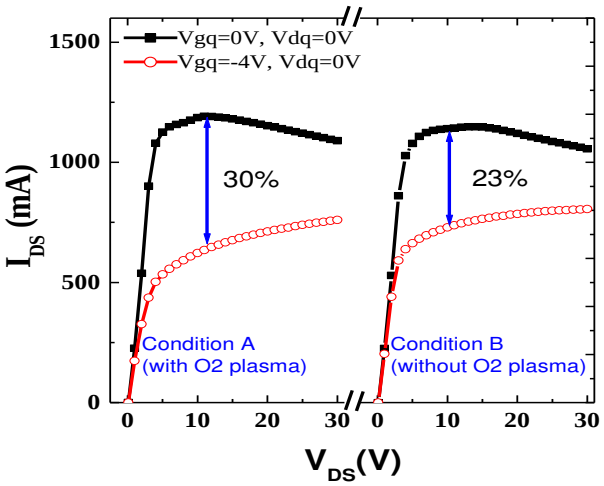

Figure 1.Pulsed I-V characterization of condition A (with O_2 plasma) and condition B (without O_2 plasma) pretreatment prior to 1st SiN passivation measurement where Vgq=0V, Vdq=0V, compared with Vgq=-4V, Vdq=0V, pulse width=750nS, and duty cycle=0.1%.

Fig. 2 shows the short-circuit current gain ($|h_{21}|$) and the maximum stable gain/maximum available gain (MSG/MAG) from on-wafer S-parameters measurements as a function of frequency for the 0.25µm gate-length device with 2x125µm gate periphery. The values of unity current gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) were determined by extrapolation of the $|h_{21}|$ and MSG data. For optimized condition B, at a drain bias of 28V and a drain current of 100mA/mm, the f_T and f_{max} were 24.5GHz and 79GHz, respectively. Comparing the A and B pretreatment conditions, optimized condition B can increase MAG/MSG performance by approximately 1.3dB and f_{max} by approximately 9GHz while keeping the same f_T performance.

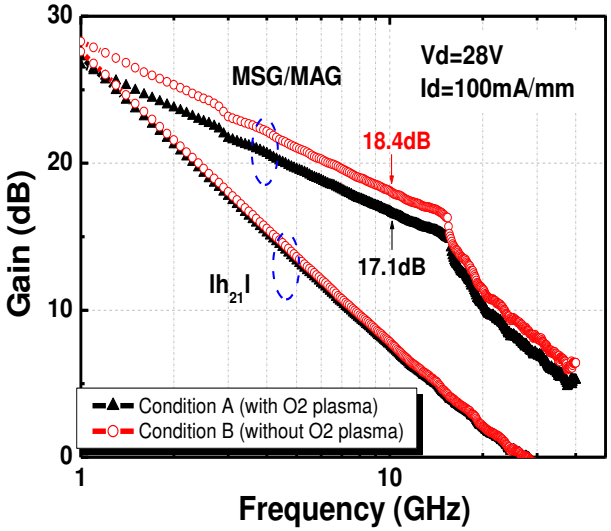

Fig.2. Comparison of small signal of a 2x125µm device performance for the condition A (with O2 plasma) and condition B (without O2 plasma) pretreatment prior to 1st SiN passivation where Vd=28V and Id=100mA/mm.

40 samples were chosen to compare the small-signal performance of condition A (with O_2 plasma) and condition B (without O_2 plasma). The small-signal RF PCM key target parameters measured on a 2x125µm transistor include: f_T, f_{max} and maximum stable gain (MSG) at 10GHz. wherein all RF parameters are measured at an IDS=100mA/mm and VDS=28V. RF PCM measurements are taken at 25 sites per wafer and f_{max}, f_T, MSG and leakage current (IPO) is shown in Fig 3. For the optimized condition B, the MSG is increased by approximately 1.3dB and the f_{max} is increased by approximately 9GHz while keeping the same f_T performance (24.5GHz) and better leakage current uniformity.

The gain in the X- and Ku-bands was improved by successfully developing a 30µm x 60µm oval substrate via technology that enables backside connections directly to the internal source contact (ISV) of the transistors. The reduced source inductance in the ISV structure enables the K=1 breakpoint of the MAG/MSG curves to be extended to higher frequency in comparison to the traditional 85µm diameter outside source circular substrate via (OSV) design. The small-signal gain performance of ISV design is compared with OSV design in Fig. 4 where the device size is 1.25mm.

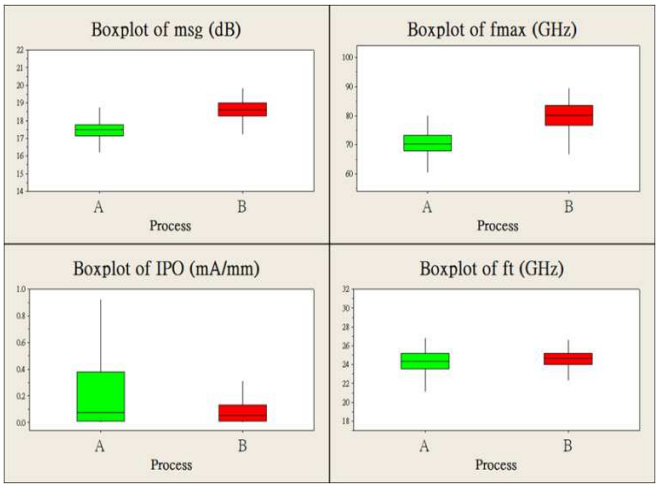

Fig.3. RF PCM chart comparison for condition A (with O_2 plasma) and condition B (without O_2 plasma).

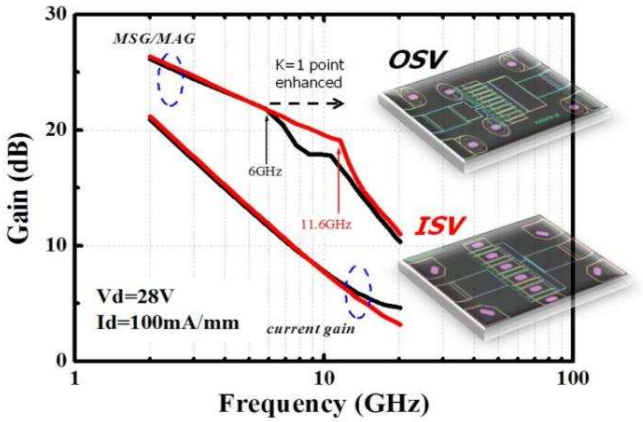

Fig.4. Small-signal gain comparison of the internal source slot via and the outside source circular via.

An SEM cross-sectional picture and an X-ray 3D image of the 30µm x 60µm ISV and the 85µm diameter OSV are shown in Fig 5. Both the OSV and the ISV show a very clean backside via sidewall and bottom surface, a vertical profile and good backside metal adhesion after backside processing.

10GHz load-pull characterization was done for a 10x125µm gate periphery device tuned for maximum power, biased at Vds=28V and Ids=100mA/mm. The Pout, Gain and PAE performance is shown in Figure 6 for the 1st SiN pretreatment condition A (with O_2 plasma) and condition B (without O_2 plasma). The optimized condition B improves gain by approximately 1.3dB in comparison to condition A. The PAE and Pout performance is above 45% and 36dBm for both conditions. The source and load tuning for both conditions was 0.8231∠-179.35 and 0.7394∠142.63, respectively.

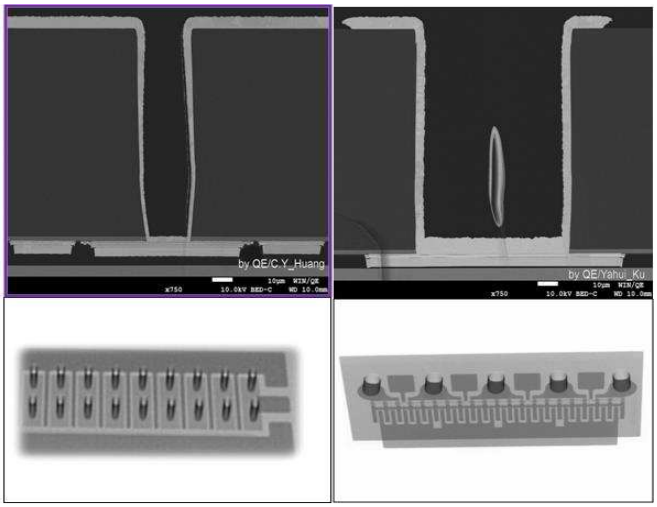

Fig.5. SEM image of the internal source slot via and the outside source circular via

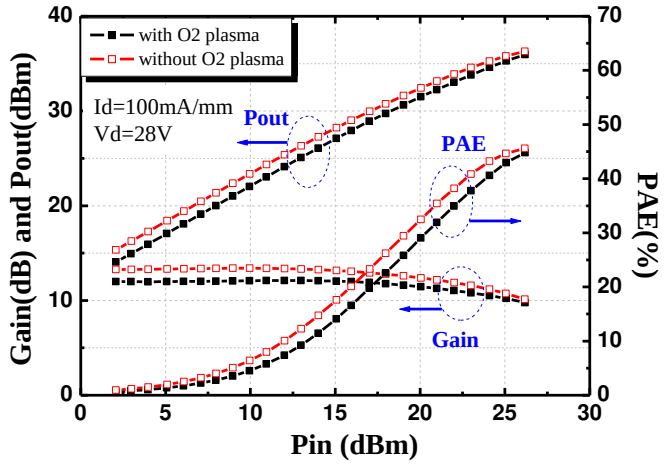

Fig.6. Load-pull comparison of a 10x125µm transistor in continuous-wave operation at 10GHz, with bias points of Vd=28V and Id=100mA/mm, tuned for maximum output power.

II. RELIABILITY

To determine whether the condition B (without O_2 plasma) reliability performance is acceptable a set of 22 devices were chosen and subjected to DC High Temperature Operating Lifetime (HTOL) and High Temperature Reverse Bias (HTRB) test. DC HTOL data is shown in Figure 7 where the devices were stressed at a peak junction temperature of 250°C with Vd=28V. All devices show good, uniform reliability performance.

HTRB reliability tests are an effective methodology to evaluate the comparatively sensitive Schottky contact. The HTRB reliability data is shown in Figure 8 where the devices were stressed at oven temperature 150°C with Vg=-8V, Vd=50V. All devices show good, uniform reliability performance.

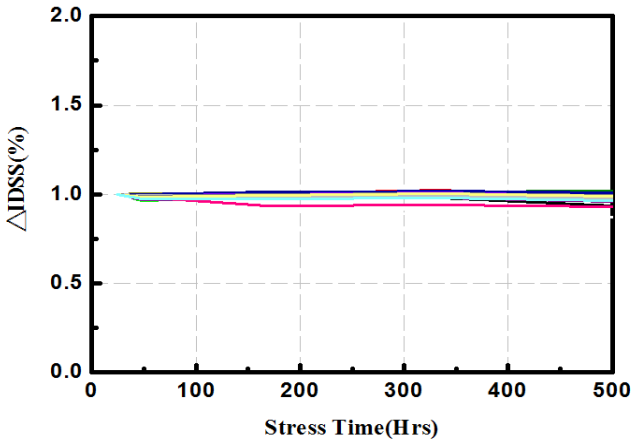

Fig.7. DC HTOL reliability performance change of the optimized pretreatment (condition B) with IDSS normalized to the initial value.

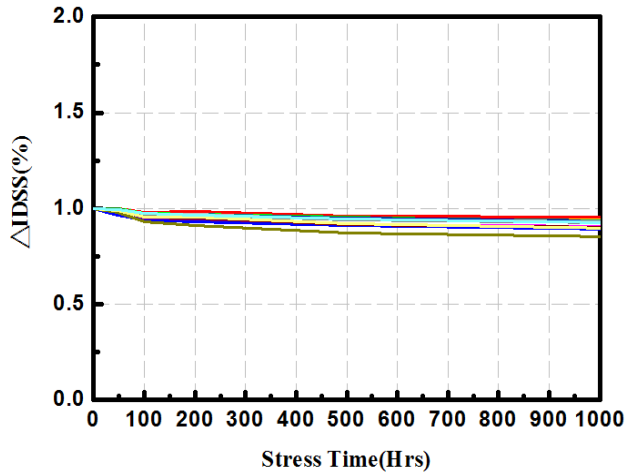

Fig.8. HTRB reliability performance change of the optimized pretreatment (condition B) with IDSS normalized to the initial value. Tests were interrupted in intervals of 50, 100, 200, 500 and 1000 hours.

Mean–time-to-failure (MTTF) is a method of evaluating the device's long-term reliability when operating at a specific junction temperature. In this test, four groups of 40 optimized condition B (without O_2 plasma) transistors are biased at Vd=28V and Id=75mA. Each group is then subjected to different ambient temperature until all parts fail. The ambient temperatures of 150°C, 165°C, 180°C and 195°C, predict a Tj of 313°C, 332°C, 351°C and 369°C respectively. The calculated MTTF is 3.53E6 hours at a junction temperature of 225°C. The activation energy (Ea) is calculated to be 2.1eV as shown in Fig. 9.

In order to qualify the thermal and mechanical stability, the devices were subjected to temperature cycling from -40°C to 125°C with a total of 1000 cycles. Fig. 9 shows the thermal cycle test (TCT) results. No failures were observed for both

the OSV and ISV structures in regards to changes in via resistance. Additionally, the metalized OSV and ISV structures both have excellent adhesion after TCT test as determined from optical and X-ray imaging.

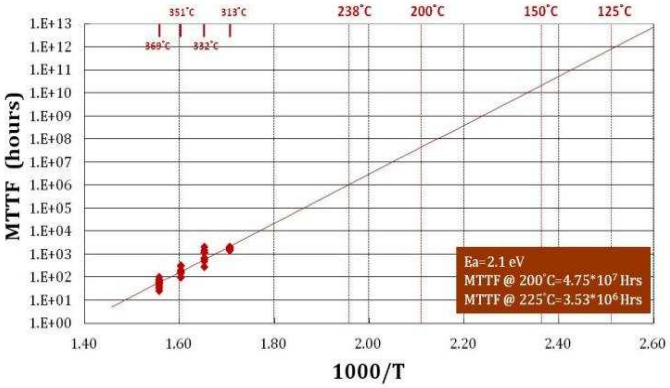

Fig.9. Arrhenius plot of the 0.25µm GaN technology with 20% Idss degradation as the failure criteria.

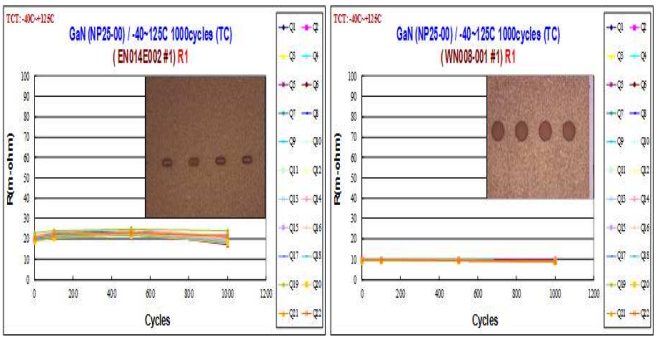

Fig.10. Backside via chain resistance after temperature cycle testing up to 1000cycles comparing a test structure with the 30µm x 60µm slot vias and 85µm diameter circular vias.

III. Conclusions

The RF performance of 0.25µm GaN/SiC HEMT technology has been improved by optimizing the pretreatment prior to 1st SiN passivation to achieve a 1.3dB increase in gain. The gain in Ku-band has been significantly further improved through the development and implementation of 30µm x 60µm slot vias incorporated within the internal source contacts on the transistors.

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References

[1] R. S. Pengelly et al,"A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs", IEEE Trans. On Microwave Theory and Techniques, Vol. 60, No. 6, June, 2012.

[2] M. H. Weng et al, "Pure Play GaN Foundry 0.25µm HEMT Technology for RF Applications", Monterey California, U.S.A., IEEE CSIC Symposium, Oct., 2013.