# Qualification of Backside Via Etch Process in GaN-on-SiC HEMT Devices

Frank Fan, Minkar Chen, Daniel Hou, and David Wang

Global Communication Semiconductors, LLC.
23155 Kashiwa Court, Torrance, California 90505
Phone: 310-530-7274
Email: ffan@gcsincorp.com

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**Abstract**

**In this paper, we describe the method we used to qualify the backside via etch process in GaN-on-SiC HEMT device manufacturing. Via chain resistance measurements were conducted after each thermal cycling test to evaluate changes in via resistance. Failure analysis was performed on failed dies based on the test results. We identified the root cause to be delamination between the plated metal and via sidewall/via bottom. Process improvements were then implemented to clean the sidewall and bottom more effectively. Results on both circular and slot vias are reported in this paper.**



## INTRODUCTION

GaN-based devices offer significant advantages for next generation military and commercial applications due to their high breakdown voltage and high electron mobility. GaN-on-SiC HEMT device performance and manufacturing technology have received considerable R&D efforts in recent years. Developing a stable and reliable backside via etch process is one of the key challenges for achieving high performance and high yield GaN-on-SiC HEMT Monolithic Microwave Integrated Circuits (MMIC) devices.

The backside vias are etched through the 75 um-thick SiC substrate and metallized with electroplated gold. To fabricate the backside vias, the wafer goes through a series of backside processing steps, including wafer bonding, thinning, via patterning, SiC via etch, and metallization. The vias are etched through the SiC substrate in inductively coupled plasma (ICP) reactors to stop at the frontside metal. Then the vias are metallized with electroplated gold.

For etching backside vias in SiC, earlier studies focused on understanding the mechanism of the formation of the pillar defects, optimizing process parameters to minimize or eliminate them [1, 2, 3, 4], and obtaining sufficient etch selectivity between SiC and GaN etch as well as between SiC and the hard mask used during the etch. More recently, efforts have been spent on achieving a higher etch rate, a post etch cleaning process of the vias, and overall manufacturability [5, 6].

In this paper, we present the method we used for the qualification of the backside via etch process and associated results.

## PROCESS QUALIFICATION

### 1) Method of Qualification

A via chain design on the Process Control Monitor (PCM) dies was used to qualify the backside via etch process. Figure 1 shows an eight-via chain test structure.

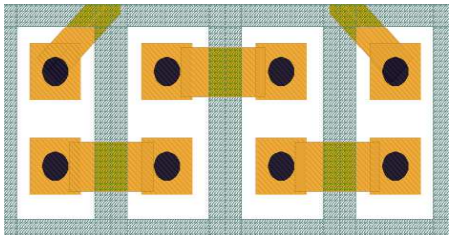


**Figure 1.** A via chain with 8 vias

After completion of the backside process, the electrical resistance of the via chain was measured with Kelvin probes at a number of PCM test sites per wafer. To evaluate the reliability of the through-wafer vias in terms of via resistance change and via integrity, a series of thermal stress

tests were conducted with a via resistance measurement following each stress test. First, a static stabilization bake ("stabake") was performed at 250°C for 24 hours in an oven with nitrogen ambient. Following the stabake, two consecutive temperature cycling stress tests were conducted on each wafer: first, temperature cycling to 300°C for 10 cycles ("TC 300C"), then temperature cycling to 350°C for 10 cycles ("TC 350C"). The temperature cycling was implemented in a conventional quartz-lamp rapid thermal processor with 50°C/s ramp-up rate, in an argon atmosphere.

Figure 2 shows the via resistance change after each thermal stress test relative to the initial value measured after completing the backside process. The change is less than 10%.

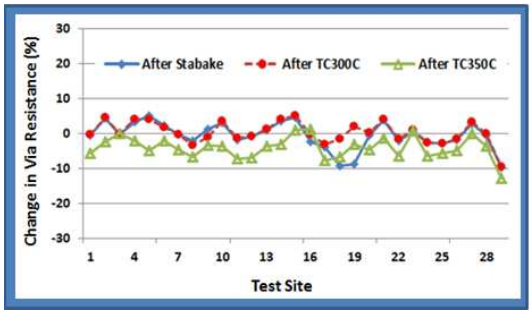
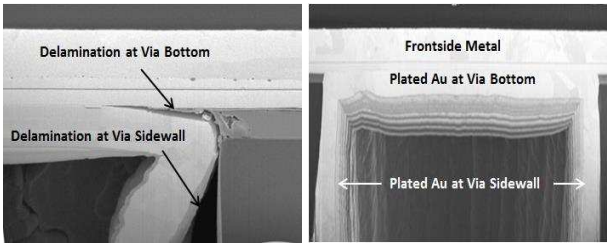



**Figure 2**. Via resistance change after TC tests

### 2) Failure Analysis and Process Improvement

When the via resistance increased by more than 20% after any of the thermal stress tests or became open, failure analysis was conducted to identify the root cause and process improvements were implemented to fix it. For example, at the early stage of process development, we found some failures from the via resistance measurements after thermal cycling tests. FIB cross-section was then performed on the failed via. Delamination was observed between the plated metal and the frontside metal structure at the via bottom, and between the plated metal and the via sidewall, as shown in Figure 3, where Fig. 3(a) is the failed via and Fig. 3(b) is a good via for reference. The delamination was a result of surface contamination at the via bottom and polymer on the via sidewall. The polymer was formed during the etching of SiC by using an etching gas mixture containing carbon and fluorine.

To solve the delamination problem, a process must be developed to remove the sidewall polymer and clean the via




(a) (b)

**Figure 3**. (a) Failed via with delamination; (b) Good via as reference.

bottom more effectively. Extensive experiments were carried out with various chemicals at different temperatures for different durations to reach the optimal solution. Figure 4 shows SEM photos of an etched via before and after our sidewall clean process, where Figs. 4(a) and 4(c) were taken before and Figs. 4(b) and 4(d) were taken after. A thick (as shown in Fig. 4(a)) and rough (as shown in Fig. 4(c)) layer of polymer was seen on the via sidewall after via etch in the ICP chamber. The sidewall became clean and smooth after cleaning, as shown in Figs. 4(b) and 4(d). The results clearly demonstrated that the sidewall polymer was removed successfully. Better adhesion was achieved between the sidewall and plated metal to survive the stress tests at high temperatures described previously. No such failures have occurred since the process improvements had been implemented.

### 3) Via Resistance

In the process qualification, we measured the total resistance of the via chains. The average resistance per via was obtained by dividing the total resistance of the via chain by the number of the vias in the design. We found that the resistance per via varied from 8 to 14 mΩ depending on different mask designs used to qualify the via etch process. This variation is due to the inclusion of the resistance of the metal patterns on both the frontside and backside in the total resistance of the via chain. Such resistance is a function of metal thickness, metal line width, and length between the vias. For a first order analysis, we calculated the theoretical resistance of each segment in the via chain, using nominal values for metal thickness on the front and the back, the metal thickness on the via sidewall, the via size, the substrate thickness, and the metal line width and length in the via chain. Table 1 shows the results for a given via chain design of 8 vias.

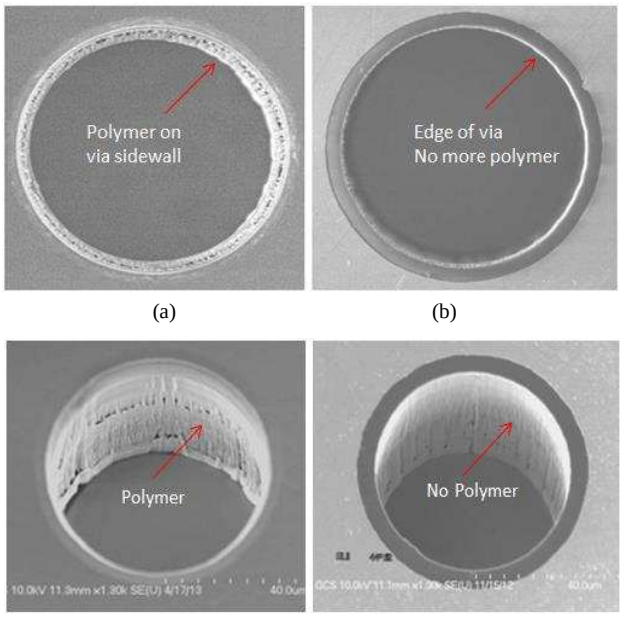



**Figure 4.** (a) and (c): Before sidewall clean;
(b) and (d): After sidewall clean.

**TABLE 1.**
THEORETICAL RESISTANCE OF A VIA CHAIN
WITH 8 VIAS (mΩ)

| | Resistance of Via Chain | Avg per Via |
|---|---|---|
| Frontside | 42.6 | 5.3 |
| Backside | 9.7 | 1.21 |
| Via | 37.3 | 4.66 |
| Total | 89.6 | 11.2 |

From the table, the total theoretical resistance of this particular via chain design is 89.6 mΩ, or 11.2 mΩ if averaged per via. The total theoretical resistance of the vias (excluding the frontside and backside patterns) is 37.3 mΩ. The theoretical resistance for a single via is thus 4.66 mΩ (37.3 divided by 8). The total measured resistance averaged per via in this case was 12.1 mΩ (total measured resistance divided by number of vias). Thus the measured resistance for a single via was 5.59 mΩ (12.1-5.3-1.21). This is only a first order analysis based on assumed values of certain parameters. It provides a guideline for theoretical and actual via resistance and explains why the measured via chain resistance varies with the via chain designs.

**4) Slot Via Qualification**

In more advanced designs, slot vias are desired so that the backside ground vias can be placed under every source pad to reduce source inductance, which would improve RF performance of large GaN HEMT transistors, especially for high frequency operations. Using the same approach, a slot via etch process has also been qualified. The via etch process developed for circular vias only needed to be slightly modified for slot vias, while no change was made to the sidewall cleaning process.

Examples of slot vias are shown in Figure 5, where Figure 5(a) shows an optical photo of the vias after etch and Figure 5(b) shows a SEM photo of a finished slot via.

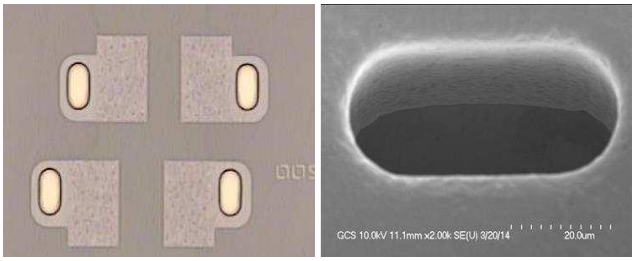



**Figure 5.** (a) Optical photo after via etch; (b) After Metallization

Figure 6 shows test results on via resistance changes of 5 chips selected for stress tests and failure analyses, from which we can see that the change in via resistance after stabilization bake and thermal cycling tests is all within 5%.

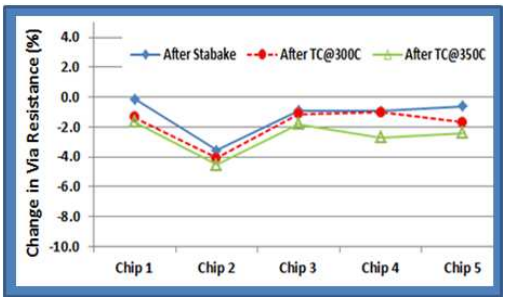



**Figure 6.** Test Results for Slot Via

Further analysis, including FIB cross-sections, demonstrated excellent integrity of the backside vias with no delamination at the interface.

## CONCLUSIONS

A backside via etch process for both circular and slot vias through the SiC substrate has been successfully developed and qualified for the fabrication of GaN-on-SiC HEMT MMIC devices. A series of process improvements have been implemented to etch through the SiC substrate and clean the via sidewall/via bottom effectively. The via resistance was measured after each stress test, including stabilization bake at 250°C, and thermal cycling tests at 300°C and 350°C. Change in via resistance is shown to be <10%. The results demonstrate successful qualification of an improved SiC backside via etch process.

## ACKNOWLEDGEMENTS

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