Thermal characterization of AlGaN/GaN HEMTs on Si and *n*-SiC substrates

R. Zhytnytska[1], J. Böcker[2], H. Just[2], O. Hilt[1], E. Bahat-Treidel[1], S. Dieckerhoff[2], J. Würfl[1] and G. Tränkle[1]

[1] Ferdinand-Braun-Institut, Leibniz Institut für Höchstfrequenztechnik, Gustav-Kirchhoff-Str. 4, 12489 Berlin, Germany
e-mail: zhytnytska@fbh-berlin.de
[2] Technische Universität Berlin, Power Electronics Research Group

Keywords: AlGaN/GaN HEMT, thermal characterization, Si substrate, SiC substrat

Abstract

The thermal properties of large periphery 60 mΩ AlGaN/GaN HEMTs fabricated on Si and SiC substrates have been studied by applying pulsed I_{ds} characterization at varying base plate temperatures and by correlating it to ANSYS simulation. At bias points being typical for power switching (linear region of I-V characteristics) the thermal properties of devices on SiC substrates show a small advantage as compared to those on Si substrates. However, if operated in the saturation region (higher value of power dissipation) at longer time pulse, GaN-on-SiC devices show a clear advantage over GaN-on-Si devices.

INTRODUCTION

High voltage powers switching AlGaN/GaN HEMTs are gaining considerable interest for future highly efficient power electronics applications. Due to its lower cost and production line compatibility, the GaN-on-Silicon approach is very attractive for industrial implementation. On the other hand, Si has a three times lower thermal conductivity as compared to SiC, well established substrate material for GaN microwave devices. In order to evaluate potential trade-offs it is important to compare systematically power switching devices on Si to similar devices on SiC substrates.

The channel temperature characterization of AlGaN/GaN devices is important for reliability estimation as well as for the prediction of switching power losses. Many methods of channel temperature (T_{ch}) characterization for AlGaN/GaN HEMTs have been presented in literature. Direct measurement methods such as micro-Raman spectroscopy [1] [2] or combined micro-Raman/IR thermography technic [3] provide a high lateral resolution and can for instance detect the exact position of the transistor´s heat source. On the other hand, these measurement methods are complicated, time consuming and expensive, and the high lateral resolution may not be necessary for many routine investigations.

The electrical characterization of temperature dependent device properties is an indirect method allowing a fast estimation of average channel temperature. Generally, the heat flow in AlGaN/GaN HEMT device packaged on heat sink can be described by Fourier's law:

$$\dot{Q} = \frac{(T_{ch} - T_{A0})}{R_{th}} \qquad (1)$$

In eq. (1) $\dot{Q}$ is heat flow which is equivalent to the dissipated power, R_{th} is thermal resistance, T_{A0} reference ambient temperature and T_{ch} is channel temperature. This equation represents the steady-state situation (dc). Thermal characterization based on dc measurement is an established method for rather small devices (W_g = 150 µm) [4]. This method relies on the assumption that at a fixed gate-source voltage (V_{gs}) the drain current decreases almost linearly with increasing ambient temperature T_A according to eq. (2) if the device is operated in saturation.

$$I_{ds} = I_{ds0} + \alpha_{th} \cdot (T_A - T_{A0}) \qquad (2)$$

I_{ds0} is the drain current at reference ambient temperature (T_{A0}) and α_{th} is an experimentally obtained proportionality constant.

This method is not applicable for very large devices as the dissipated heat at high drain voltage (V_{ds}) and operating the device in saturation would lead to device destruction. However, the on-state bias point for power switching applications is usually placed in the linear region of the output characteristics. In this case the on-state drain voltage is rather low, for example (V_{ds} < 5 V, I_{ds} < 1/3 $I_{ds\,max}$). In [5] it has been analytically found, that pulsed

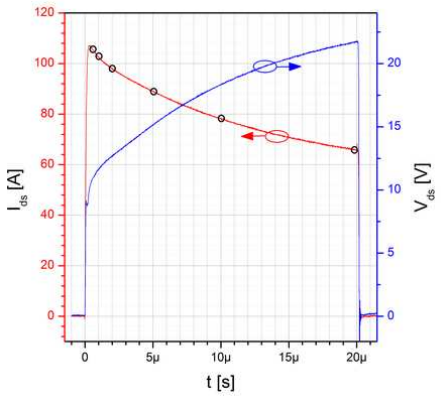

Figure 1: Exsample of pulsed IV characterisation of large periphery devices fabricated on Si substrates, pulse duration 20 µs. Circular marks show exraction points of time regions.

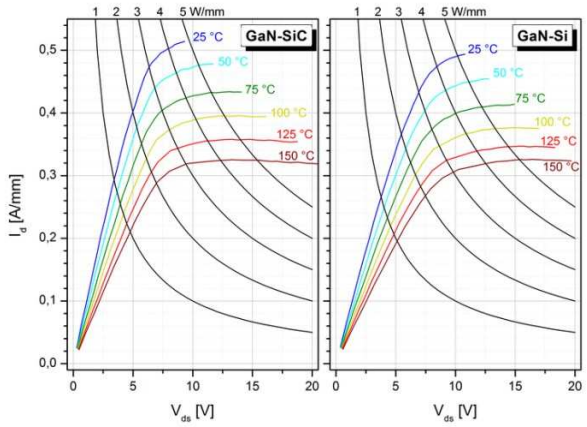

Figure 2: Pulsed (at 0.5 µs) I_{ds}-V_{ds} characteristics measured at V_{gs} = + 4.4 V for GaN-on-SiC and V_{gs} = + 4.6 V for GaN-on-Si at base plate temperatures varying from 25 °C to 150 °C.

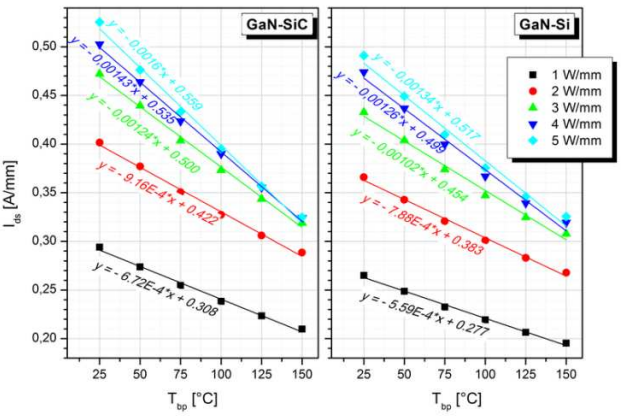

Figure 3: I_{ds}(T) extracted at t = 0.5 µs for varying power conditions on Si and SiC substrates. Approximation by linear equations is presented by lines.

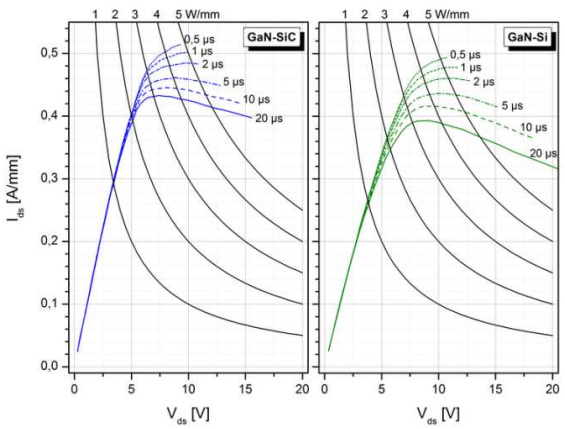

Figure 4: Pulsed I_{ds}-V_{ds} characteristics measured at V_{gs} = + 4.4 V for GaN-on-SiC and V_{gs} = + 4.6 V for GaN-on-Si extracted at time points 0.5…20 µs at base plate temperature of 25 °C.

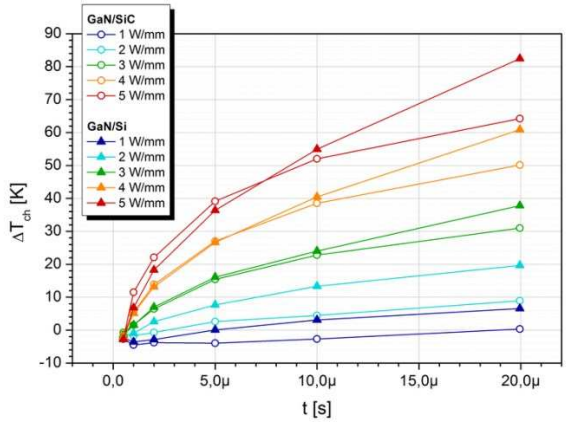

Figure 5: Delta of channel temperature (T_{ch} - T_{bp}) depending on time calculated from figure 4 for power dissipation of 1…5 W/mm for Si and SiC substrates.

electrical characterization can probe the time-depended thermal behavior of AlGaN/GaN devices. If devices are pulsed from a zero drain and zero gate voltage bias point, trapping effects are negligible and any reduction of drain current I_{ds} is directly related to a thermal effects. In our study we present a method of thermally characterizing large AlGaN/GaN HFETs based on pulsed electrical measurements.

DEVICE FABRICATION AND MEASUREMENT SETUP

All devices are processed on MOCVD grown GaN-on-Si wafers supplied from a commercial vendor and GaN-on-SiC wafers from FBH epitaxy. The GaN-on-SiC epitaxial structure consists of ~ 50 nm AlN seeding layer, 2 µm GaN:Fe buffer (~ 2×10^{18} cm^{-3}), 850 nm *uid* GaN channel, 9 nm $Al_{0.24}Ga_{0.76}N$ barrier, 3 nm GaN cap and 100 nm *p*-GaN. GaN-on-Si epitaxial structure consists of 4.5 µm buffer (including channel), 15 nm $Al_{0.25}Ga_{0.75}N$ barrier and 95 nm *p*-GaN.

The large periphery 60 mΩ transistors with 214 mm gate width have been processed using FBH´s *p*-GaN gate technology [6]. All devices have a gate-drain separation of 15 µm. The devices are cut to 4.4 × 2.3 mm^2 chip size. The substrate thickness is 200 µm. Chips are soldered on an Au-coated CuMo heat sink using a $PbSn_5Ag_{2.5}$ solder alloy (~ 20 µm) and connected by Au wire bonding.

A transistor measurement setup capable to handle drain current levels up to 200 A has been developed at TU Berlin. Devices are pulsed from the bias point V_{ds} = 0 V to any bias point in the output I-V characteristics (V_{ds} = 0…20 V) for a constant pulse length of 20 µs. During the 20 µs pulsing the system acts as a high-speed data logger. After pulsing the system bias comes back to V_{ds} = 0 V and resides there for 1 ms before the next pulse is released. The dynamic I_{ds}-V_{ds} characteristics have then been extracted at various time-points within the pulse (at 0.5, 1, 2, 5, 10 and 20 µs after the switching event, see figure 1). To provide a fair comparison between GaN-on-Si and GaN-on-

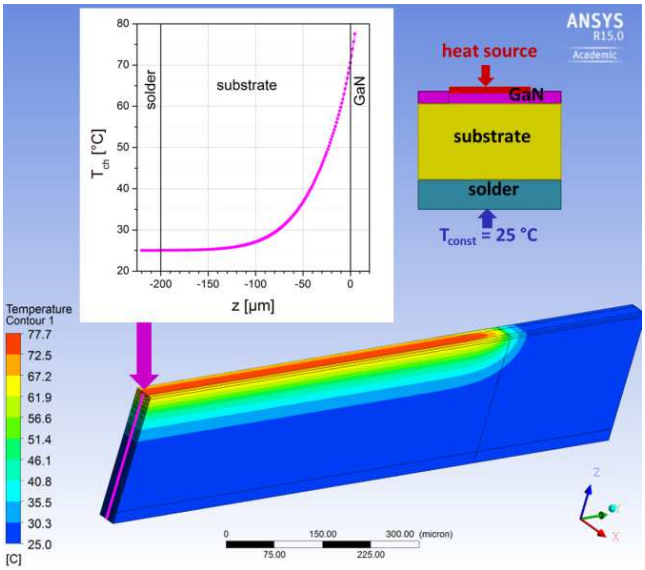

Figure 6: Temperature distribution simulated with ANSYS for power condition of 5 W/mm on Si substrate after pulse length of 20 µs. Inset: T_{ch} along marked z coordinate.

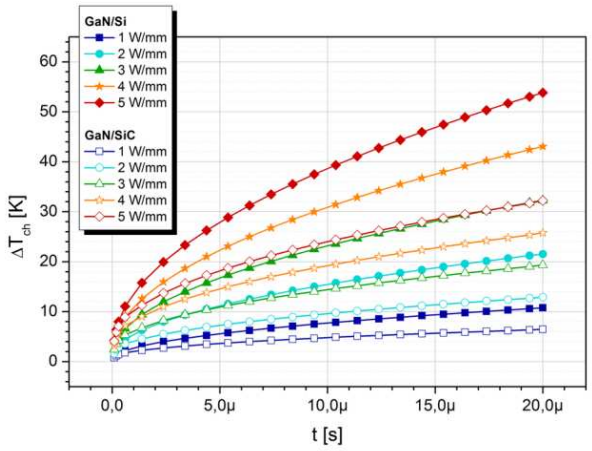

Figure 7: Delta of channel temperature (T_{ch}-T_{bp}) depending on time simulated with ANSYS for power dissipation of 1…5 W/mm for Si and SiC substrates.

SiC devices the devices have been biased such that saturation current at the shortest pulse duration (0.5 µs) is identical for both devices, for details see figure 2. The maximum I_{ds} at 25 °C is ~ 0.52 A/mm for the GaN-on-SiC and ~ 0.5 A/mm for the GaN-on-Si device.

TABLE 1
MATERIAL PARAMETERS USED FOR SIMULATION

Material	Thermal conductivity [W/(m·K)]	Specific heat [J/(g·K)]	Density [g/cm³]
GaN	160	0.49	6.15
Si	149	0.7	2.33
SiC	400	0.69	3.2
PbSn5Ag2.5 solder	26	0.13	11.02

EXPERIMENTAL RESULTS

For calibrating the measurement routine the high current branches of the output characteristics at different base-plate temperatures have been probed by very short pulses of 0.5 µs duration only (figure 2). In this case the temperature increase (self-heating) due to the measurement pulse itself can be neglected (isothermal condition). Figure 2 also contains the hyperbolic curves of constant dissipated power for power densities between 1 and 5 W/mm. For $I_{ds}(T_A)$ calibration the I_{ds} values data at the intersection point with the curves of constant power density have been extracted from Fig. 2. As the self-heating of the transistor is negligible the decrease of I_{ds} with increasing T_{pb} can be approximated by an almost linear dependency on temperature. The linear thermal coefficient (α_{th}) has then been calculated for each power density condition (see figure 3). Our results show, that within chosen T_{bp} conditions, for both regions of output characteristics, the linear region and saturation region, I_{ds} (T_A) could be approximated by linear equations. The thermal gradient of I_{ds} is higher in the saturation region of the I_{ds}-V_{ds} characteristic as compared to linear region.

Figure 4 shows pulsed I_{ds}-V_{ds} characteristics for different pulse duration at T_{bp} = 25 °C for transistors on SiC and Si substrates. The thermally caused decrease of I_{ds} with increasing power dissipation and the pulse length is present for both substrates. On Si substrate this decrease is stronger than on SiC. The channel temperature has been calculated by using the thermal coefficients from figure 3. The calibration error, calculated from error of linear approximation, within ± 5 K is responsible for negative values of ΔT_{ch} (see figure 5).

The channel temperature increases with increasing pulse duration as expected from theory (see figure 5). At P = 1 W/mm and 2 W/mm ΔT_{ch} is slightly higher for the Si substrate. At t = 20 µs the difference is 8 K for 1 W/mm and 11 K for 2 W/mm. These power dissipation points represent the linear ohmic region of the I_{ds}-V_{ds} characteristics.

If the dissipated power is higher than 3 W/mm (representing the saturation region of I_{ds}-V_{ds} characteristics) for larger pulse durations (20 µs) the difference between Si and SiC substrates becomes clearly visible. The ΔT_{ch} at P = 5 W/mm is 82 K on Si substrate and 64 K on SiC substrate. The ΔT_{ch} difference between both substrates is 18 K.

SIMULATION RESULTS

The experimental results have been compared to thermal transient simulation (ANSYS) of idealized GaN-on-Si and GaN-on-SiC structures. The simulation has been done on a simplified 1-finger model representing the thermal characteristics of fingers in the center of the large device (see figure 6). The model used for simulation consists of a cut-out of a one finger cell (1.6 mm finger length) from the center of a large transistor containing 134 fingers. The

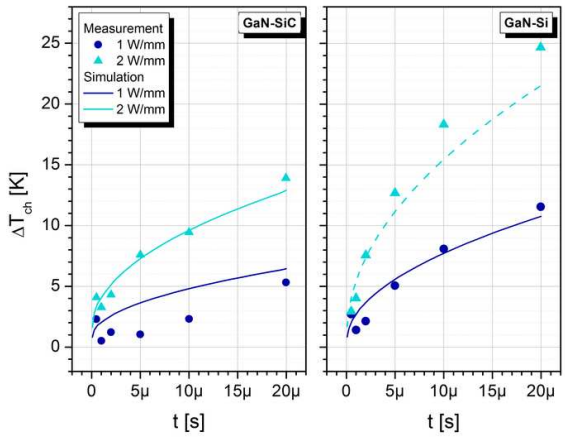

Figure 8: Comparison of measured and simulated ΔT_{ch} for power dissipation of 1 and 2 W/mm, representing the linear region of I-V characteristics, for Si and SiC substrates.

model is reduced to a half finger arrangement when considering axial symmetry. Adiabatic boundary conditions have been applied on the finger sidewalls. The bottom of solder has an isothermal boundary (25 °C). The structure consists of a 3.2 µm (for SiC) and 4.5 µm (for Si) thick GaN layer, a 200 µm thick substrate and a 20 µm thick solder layer. The heat source has been defined as an area power flow between source and drain contact (width 17.2 µm) on top of the GaN layer. Table 1 summarizes the material parameters used for simulation. Figure 6 shows the simulated temperature distribution for power condition of 5 W/mm on Si substrate after pulse length of 20 µs. Within the 150 µm of substrate thickness the temperature drops to the ambient temperature of 25 °C (inset).

Figure 7 compares the simulated increase of ΔT_{ch} with the pulse duration for P = 1…5 W/mm on Si and SiC substrates. At P higher than 3 W/mm the simulated ΔT_{ch} is lower than measured on both substrates. At 20 µs and 5 W/mm ΔT_{ch} is 54 K on Si substrate and 32 K on SiC substrate. The simulated ΔT_{ch} difference between both substrates is 22 K. At P = 1 and 2 W/mm the simulation results are in coincidence with the measurement results (see figure 8).

DISCUSSION

The measurement results show that two regions of thermal dependency are to be distinguished: the linear ohmic region of I_{ds}-V_{ds} characteristics with power dissipation below 2 W/mm and saturation region with power dissipation above 3 W/mm. The channel temperature is higher on Si substrate as compared to SiC substrate especially if the measurements have been taken after longer pulse durations and if the device is biased in the saturation region. In the linear region a good agreement between experiment and simulation has been found (see figure 8). If short pulses are applied in the saturation region of the I_{ds}-V_{ds} characteristics the channel temperature on both substrates is identical. This can be explained as follows: The spatial distribution of heat generation inside the GaN-layers, along the source-drain direction changes with increasing V_{ds} [7]. If the device is biased in the linear region the heat is uniformly distributed along the source-drain channel. Such distribution was considered for the simulations. Therefore the measurement results are matching well in at this bias condition. At higher V_{ds} the heat source is narrowing to the gate region. Since this situation has not been considered by the simulation, the measured temperature is higher than the simulated temperature.

CONCLUSIONS

In our study we have shown the thermal characterization of large AlGaN/GaN HEMTs for power applications. We have shown that our measurement method is sufficient for thermal characterization of large power switching devices. Thermal simulation based on a simplified model gives a good prediction for bias points being representative for power switching applications (in the linear region of the output IV characteristics). For typical power switching applications no significant disadvantages of thermal properties of devices on Si substrates have been found.

ACKNOWLEDGEMENTS

Support from EU FP7 project HiPoSwitch (Grant no. 287602) is gratefully acknowledged.

The authors would like to thank F. Brunner for epitaxy and L. Schellhase for device packaging.

REFERENCES

[1] M. Kuball, J. M. Hayes, M. J. Uren, T. Martin, J. C. H. Birbeck, R. S. Balmer, and B. T. Hughes, *IEEE Electron Device Letters,* vol. 23, no. 1, January 2002.

[2] M. Kuball, G. J. Riedel, J. W. Pomeroy, A. Sarua, M. J. Uren, T. Martin, K. P. Hilton, J. O. Maclean, and D. J. Wallis, *IEEE Electron Device Letters*, vol. 28, no. 2, February 2007.

[3] A. Sarua, H. Ji, M. Kuball, M. J. Uren, T. Martin, K. P. Hilton, and R. S. Balmer, *IEEE Transactions on Electron Devices*, vol. 53, no. 10, October 2006.

[4] R. Menozzi, B.R. Nener and L. Faraone, IEEE Transactions on Device and Materials Reliability, vol. 8, no. 2, pp. 255-264, June 2008

[5] A. Wang, M. J. Tadjer, and F. Calle, Semiconductor Science and Technology, vol. 28 (2013) 055010

[6] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel and J. Würfl, *Proc. ISPSD 2010*, Hiroshima, pp. 347-350.

[7] T. Sadi and R. W. Kelsall, *IEEE Transactions on Electron Devices*, vol. 53, pp. 2892–2900 , 2006.