Improved Thermal Stabilities in Normally-off GaN MIS-HEMTs

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Abstract

Normally-off MIS-HEMTs with good thermal stability in threshold voltage (V_{TH}) is demonstrated in this work. The MIS-HEMTs featuring a partially recessed fluorine implanted (Al)GaN barrier were realized by a fluorine-plasma implantation/etch technique. A well-controlled dry etching for AlGaN barrier recess and a fluorine ion implantation into barrier are carried out with CF_4 plasma at a relatively high RF driving power. The partially recessed barrier leads to improved thermal stability, while the fluorine implantation is essential to achieve normally-off channel without completely removing the barrier and losing the high mobility heterojunction channel. When the operating temperature increases from 25 °C to 200 °C, the device exhibits a small negative shift of V_{TH} (~0.5 V). The partially recessed MIS-HEMTs, with AlN/SiN_x passivation, can also deliver stable dynamic performance with negligible current collapse when switching at high temperatures.

INTRODUCTION

GaN based power transistors, with the merit of operating at elevated junction/ambient temperatures and high switching frequencies, are suitable for high-performance compact power converters [1]. To meet the requirement of power switches with small gate leakage current and large gate swing, the MIS gate is preferred over schottky gate. As high-voltage power switching devices typically operate at elevated junction temperature (T_J), thermal stabilities of the GaN power MIS-HEMTs are of particular importance. For the MIS-gate GaN transistors, their high temperature stability can be hindered by the challenges of V_{TH} instability originating from the thermal electron emission of trap states at the dielectric/III-N interface [2, 3]. To address this issue, a thinned barrier layer is proposed to bring the deep interface traps below the Fermi level at pinch-off so that they become inactive [3].

In this work, normally-off MIS-HEMTs with a partially recessed (Al)GaN barrier were realized by implementing a fluorine-plasma implantation/etch technique. The partially recessed barrier leads to improved thermal stability, while

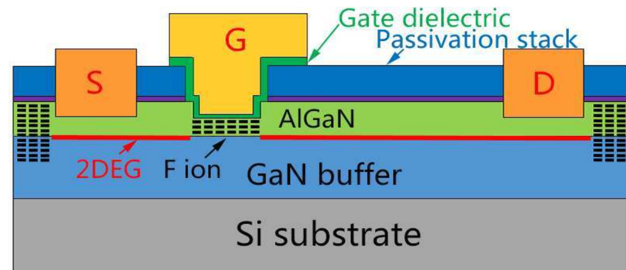

Fig. 1: Cross-sectional schematic of a fabricated normally-off MIS-HEMT.

the fluorine implantation can convert the device from D-mode to E-mode without completely removing the barrier and sacrificing the high mobility heterojunction channel [4]. Both the barrier recess and fluorine ion implantation were conducted with CF_4 plasma at relatively high RF driving power. Excellent thermal stability in V_{TH} was demonstrated at increasing operating temperatures, and is mainly attributed to the partially recessed barrier layer that brings the critical dielectric/AlGaN interface closer to the 2DEG channel. The MIS-HEMTs show small current collapse under switching tests conducted at temperature ranging from 25 °C to 200 °C.

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DEVICE FABRICATION

The MIS-HEMTs are fabricated on a GaN-on-silicon sample that consists of a 22-nm (Al)GaN barrier and a 4-μm GaN buffer/transition layer. Fig. 1 depicts the schematic cross-section of the normally-off MIS-HEMT. The fabrication process started with source/drain ohmic contacts formation, followed by an AlN/SiN_x passivation [4] and planar isolation achieved by multi-energy F-ion implantation. After removing the passivation stack in the gate window by ICP-RIE dry etching, the fluorine ion implantation and gate recess were carried out by applying CF_4 plasma to the gate region. By properly adjusting the power level of the RF source driving the fluorine plasma, we are able to obtain two desirable results: 1) a well-controlled slow dry etching for gate recess; and 2) effective shallow implantation of fluorine ions into the AlGaN barrier. Fluorine plasma implantation at a higher RF power level of 200 W resulted in a well-controlled

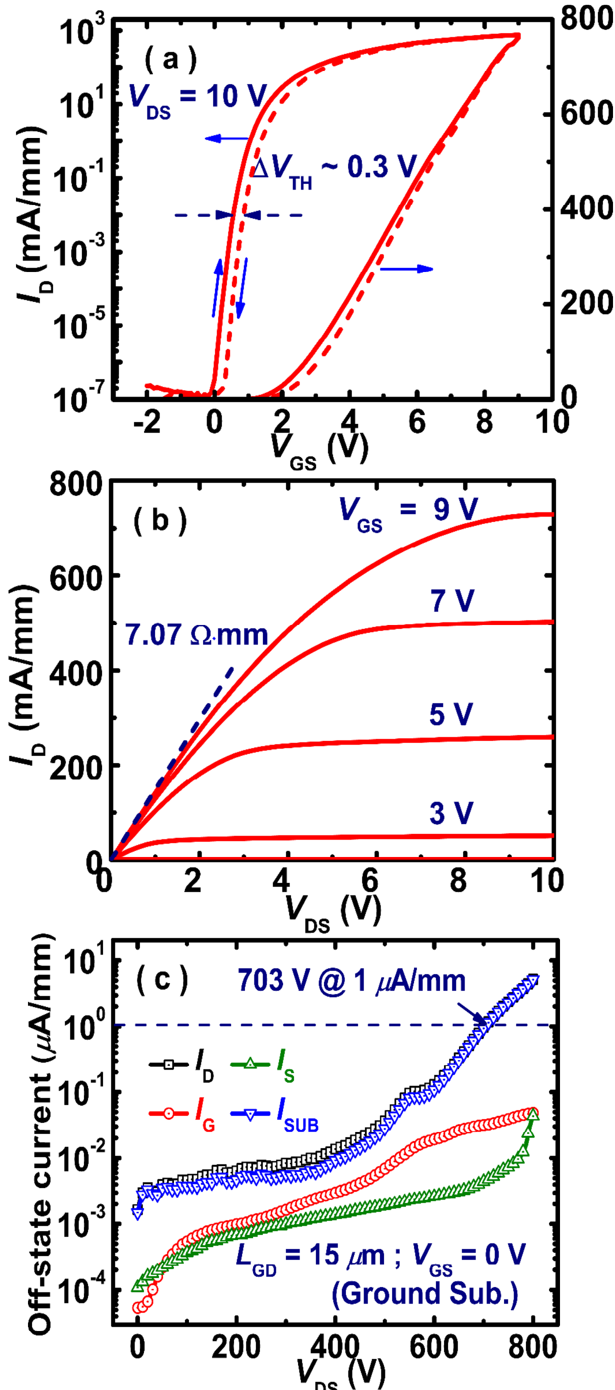

Fig. 2: (a) Transfer and (b) output characteristics of a MIS-HEMT with L_G = 1.5 μm and L_{GD} = 10 μm. (c) OFF-state I-V characteristics of a MIS-HEMT with a gate-source voltage of 0 V and a grounded substrate.

slow etching process with an etching rate of 2-nm/min. Meanwhile, a lower RF power of 150 W only induced insignificant etching of the barrier layer [5]. After 6 minutes of F-plasma implantation/etch, a recess depth of ~12 nm and an atomic-smooth etched surface were obtained. After removing another 2-nm AlGaN by a digital

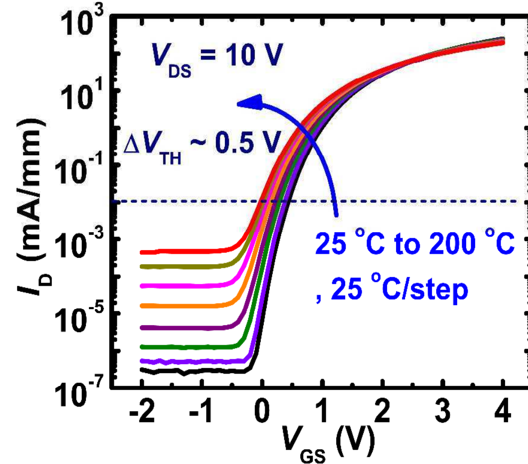

Fig. 3: Temperature (T)-dependent transfer characteristics of a MIS-HEMT with L_G = 1 μm and L_{GD} = 2 μm at T increasing from 25 °C to 200 °C.

etching [6], 20-nm Al_2O_3 was deposited by ALD with an *in situ* nitridation process [7].

RESULTS AND DISCUSSION

Figure 2 shows the room-temperature dc characteristics of a normally-off MIS-HEMT with a gate length L_G = 1.5 μm and a gate-to-drain spacing L_{GD} = 10 μm. The device exhibits a threshold voltage (V_{TH}) of +0.6 V at a drain current of 10 μA/mm, or ~+2.1 V by the linear extrapolation of the drain current at the point of peak transconductance. The device delivers a maximum drive current of 730 mA/mm at a forward gate bias of 9 V, and an on-resistance of 7.07 Ω·mm. A subthreshold swing (*SS*) of ~105 mV/dec and a small hysteresis (~0.3 V) between the up- and down- V_{GS}-sweep (with a relatively fast sweeping rate of 0.7 V/s) suggest a high quality dielectric/F-implanted-(Al)GaN interface of the device. Three-terminal OFF-state breakdown measurement of a MIS-HEMT with L_{GD} = 15 μm yields a breakdown voltage of 703 V at a drain leakage of 1 μA/mm with the substrate grounded. The drain leakage current in the OFF-state is dominated by the vertical drain-to-substrate current while the source and gate current (I_S and I_G) remain below 0.1 μA/mm even at a drain bias of 800 V.

Figure 3 depicts the temperature (T)-dependent transfer characteristics of a MIS-HEMT. When temperature increases from 25 °C to 200 °C, an increase of 3 orders of magnitude is observed in the OFF-state drain leakage due to increased buffer leakage, while the on-state drain current decreases due to lower carrier mobility at higher temperatures. By using a current criterion of 10-μA/mm I_{DS}, V_{TH} shifted by 0.5 V negatively. According to a recent report [8], the thermally stable V_{TH} of MIS-HEMTs with recessed gate is mainly attributed to the thin barrier thickness. The recessed barrier buries the deep interface

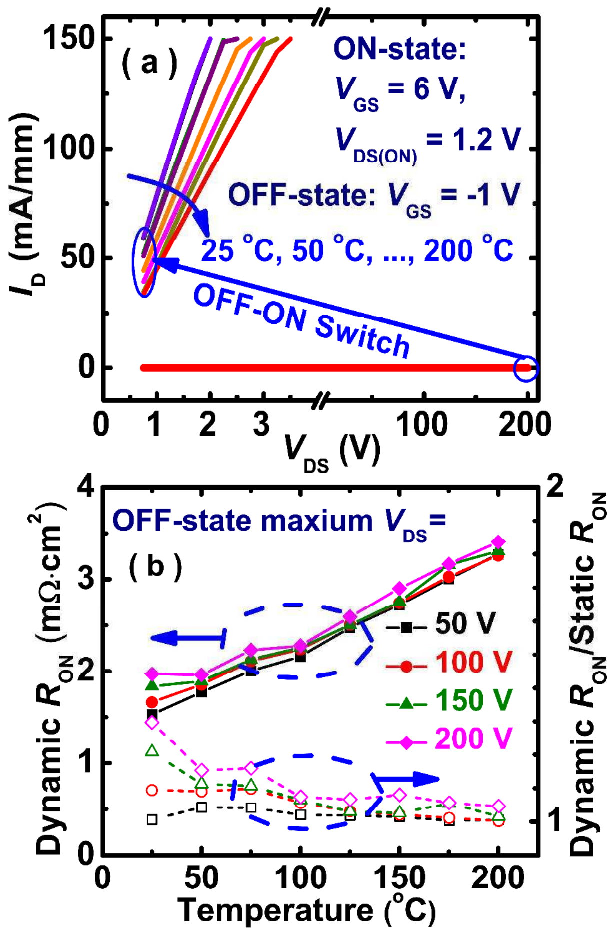

Fig. 4: (a) ON-wafer transient switching I_D-V_{DS} characteristics of a MIS-MEMT with L_{GD} = 10 μm at T ranging from 25 °C to 200 °C. The ON-state features V_{GS} and V_{DS} bias of 6 V and 1.2 V, respectively. The switching time is ~0.1 s. (b) Ratio of dynamic R_{ON} and dc static R_{ON} obtained by the T-dependent low-speed transient switching test with various OFF-state V_{DS} stress (50 V to 200 V).

traps below the Fermi level at pinch-off so that they become inactive and they are not able to emit electrons at high temperatures.

The high-drain-bias transient switching tests were performed with the temperature ranging from 25 °C to 200 °C, and the temperature dependence of the dynamic on-resistance (R_{ON}) is plotted in Fig. 4. The MIS-HEMT is capable of blocking 200 V at an operation temperature of 200 °C with vertical drain-to-substrate current dominating the drain leakage. In the OFF-state, the maximum drain stress V_{DS} at high temperature was kept below 200 V due to the limitation of our on-wafer test system. In the ON-state, the dynamic R_{ON} is evaluated at 6-V V_{GS} and 1.2-V V_{DS} bias. At elevated temperatures, despite an increasing value of the R_{ON} due to the reduced channel mobility, the degradation of dynamic R_{ON} under a V_{DS}'stress up to 200 V is reduced. At room temperature, the dynamic R_{ON} degradation for 200 V stress is 29.6%, which reduces to

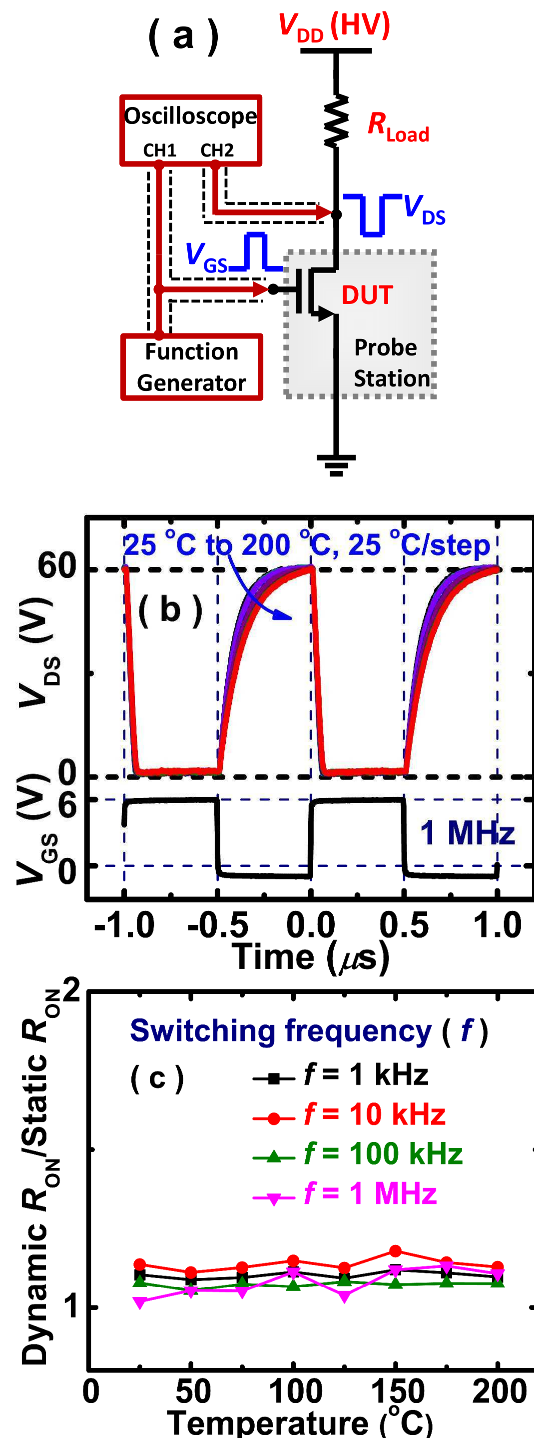

Fig. 5: (a) Schematic diagram of the testing circuit of on-wafer hard switching characterization. (b) Switching waveforms of a MIS-HEMT operated at 1 MHz with 50% duty cycle. V_{GS} is switched from −1 V to +6 V and the maximum V_{DS} is 60 V. (c) Ratio of dynamic R_{ON} and dc static R_{ON} obtained by high-frequency (1 kHz to 1 MHz) hard switching characterization at temperature increasing from 25 °C to 200 °C.

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4.6% when operating temperature increase to 200 ^{o}C. These results suggest that some relatively shallow traps are involved in degrading the dynamic R_{ON}, and emissions from these traps are accelerated at higher temperatures.

Continuous hard switching tests of the MIS-HEMT at temperature ranging from 25°C to 200°C were conducted using the circuit configuration shown in Fig. 5(a), with a V_{DD} of 60 V. Typical switching waveforms of the MIS-HEMT operated at 1 MHz with a 50% duty cycle are illustrated in Fig. 5 (b). By measuring the on-state drain voltage drop $V_{DS,ON}$ in the switching waveforms, the dynamic R_{ON} can be determined by,

$$R_{\mathrm{ON_Dynamic}} = V_{\mathrm{DS,ON}} \,/\, \left(\frac{V_{\mathrm{DD}} - V_{\mathrm{DS,ON}}}{R_{\mathrm{Load}}}\right)$$

The dynamic R_{ON} degradation under 60-V switching with various switching frequency (e.g from 1 kHz to 1MHz) are plotted against the operation temperature in Fig. 5 (b). During the hard switching test under high-frequency and high-temperature conditions, the increase of dynamic R_{ON} is less than 18% and shows negligible temperature dependence. The stable dynamic performance of the MIS-HEMT is consistent with our previous results of GaN HEMT with the same AlN/SiN_x passivation scheme [9].

CONCLUSIONS

Thermally stable threshold voltage (V_{TH}) up to 200 ^{o}C has been obtained in normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs with partially recessed fluorine-implanted barrier. The partially recessed barrier leads to improved thermal stability, while the fluorine ion implantation can bring normally-off operation without completely removing the barrier and losing the high mobility heterojunction channel. By using AlN/SiN_x passivation technique, the device can also deliver low current collapse within a wide temperature range from 25 ^{o}C to 200 ^{o}C. In particular, the dynamic on-resistance is shown not to be more severely degraded at higher temperatures. The normally-off MIS-HEMTs with improved thermal stability in DC and dynamic performance are suitable for power switching applications.

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ACRONYMS

MIS: Metal-Insulator-Semiconductor
HEMTs: High Electron Mobility Transistors
RF: Radio Frequency
D-mode: Depletion-mode
E-mode: Enhancement-mode
2DEG: Two-Dimensional Electron Gas
ICP-RIE: Inductively Coupled Plasma-Reactive Ion Etching
ALD: Atomic Layer Deposition