CS MANTECH™ 2021

# Digest of Papers

## 2021 International Conference on Compound Semiconductor Manufacturing Technology

May, 24th 2021

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# 2021

# International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH)

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May 24th, 2021

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# CHAIR'S MESSAGE

As your Chairman, I am excited to welcome you to the 35th annual International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH), our first virtual event.

From its inception in 1986, the CS MANTECH conference has been the only conference dedicated to featuring manufacturing objectives alongside state-of-the-art compound materials challenges and industry-leading device performance demonstrations, all within a single virtual venue. I am very proud of our Technical Program team and Executive Committee for compiling this virtual conference, which captures all that CS MANTECH has to offer. We welcome participants from around the globe engaged in research, academia, and production. Our virtual event promotes a free exchange of ideas, processing methods, research, and Best Known Methods to advance the knowledge of utilizing Compound Semiconductors by presenting peer-reviewed papers, our workshop, and vendor talks.

I also would like to thank all of the volunteers on the Technical Program Committee and the Executive Committee, along with their supporting organizations. CS MANTECH would not be possible without a tremendous amount of work from many individuals who have volunteered their time to ensure its success.

**Thorsten Saeger**
**Qorvo**
**Conference Chair**
**2021 CS MANTECH**

The CS Mantech organization has lost a beloved and valued member with the recent passing of our long-time Executive Assistant Margaret Doyle. She was a loving wife to her husband Richard, doting mother of 8 and grandmother of 4, avid gardener, and dear friend to all of us who were lucky enough to know her. She was called "Peggy" by her family but at Mantech she was always and only Margaret. For two decades of the conference, she was a smiling face greeting attendees at the registration desk, the "lady with the camera" visually documenting our event, helping Nobel prize winners, CEO's, and foreign student attendees with the same unfailing warmth and good cheer. She worked particularly closely with our exhibitors, who enjoyed her friendly personality and benefited from her constant helpful attitude.

Margaret had only recently retired from her Mantech work but had planned to attend our next face-to-face conference with Rich as honored guests to say goodbye to her many friends and well-wishers. We are all deeply saddened by her passing, by not having the opportunity to see her lovely smile one more time, to get one more chance to tell her how much we appreciated her long service, and to wish her well in retirement. We extend our deepest sympathies and condolences to her loving family. She will live on in the hearts and minds of those who cherish her memory. Rest in Peace, dear Margaret.

# 2021 CONFERENCE SPONSORS

(Updated 5/18/2021)

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The He Bong Kim Award is named after the founding chairman of the conference, whose vision and desire for excellence is continued through the recognition of the best papers from the previous year's conference. Congratulations to these award winning teams for their excellent presentation and technical contribution to our field!

**2019 AWARD WINNER**

**Current Status of SiC Materials and Devices for use in Power Applications**
John Palmour
*Wolfspeed, A Cree Company*

**2019 AWARD HONORABLE MENTION**

**First ESA missions to use gallium nitride (GaN) – a disruptive technology for space based payloads**
Andrew Barnes
*European Space Agency*

**2019 BEST STUDENT PAPER**

**Extreme Temperature Operation of Ultra-Wide Bandgap AlGaN High Electron Mobility Transistors**
P. H. Carey IV[1], F. Ren[1], A. G. Baca[2], B. A. Klein[2], A. A. Allerman[2], A. M. Armstrong[2], E. A. Douglas[2,] R. J. Kaplar[2], S. J. Pearton[1]
*[1]University of Florida, [2]Sandia National Laboratories*

**2018 AWARD WINNER**

**Looking for reliability and high performance in RF and power conversion applications? Use GaN.**
Umesh Mishra
*University of California Santa Barbara & Transphorm Inc.*

**2018 AWARD HONORABLE MENTION**

**Automotive Industry Trends and Their Impact on the Future Vehicle**
Kamal Khouri
*NXP Semiconductors*

**2018 BEST STUDENT PAPER**

**Controlling Impurity-Induced Disordering Via Mask Strain for High-Performance Vertical-Cavity Surface-Emitting Lasers**
Patrick Su, Thomas O'Brien, Jr., Fu-Chen Hsiao, and John. M. Dallesasse
*University of Illinois at Urbana-Champaign*

**2017 AWARD WINNER**

**The 5G Effect on RF Filter Technologies**
Steve Mahon
*Feldman Engineering*

**2017 AWARD HONORABLE MENTION**

**Effect of Manufacture on the Microstructure of GaN-on-Diamond**
Dong Liu[1,2], Daniel Francis[3], Firooz Faili[3], James W. Pomeroy[2], Daniel J. Twitchen[3], and Martin Kuball[2]
*[1]University of Oxford, [2]Center for Device Thermography and Reliability, University of Bristol, [3]Element Six Technologies*

**2017 BEST STUDENT PAPER**

**Cubic Phase GaN Integrated on CMOS-Compatible Silicon (100)**
Richard Liu and Can Bayram
*University of Illinois at Urbana-Champaign*

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| **2016 AWARD WINNER** | **Epitaxial Lift-off and Transfer of III-N Materials and Devices from SiC**<br>David Meyer[1], Brian Downey[1], Travis Anderson[1], Scott Katzer[1], Neeraj Nepal[1], Virginia Wheeler[1], David Storm[1], and Matthew Hardy[2]<br>*[1]Naval Research Laboratory, Electronics Science and Technology Division, [2]NAS NRC Postdoctoral Fellow, residing at the Naval Research Laboratory* |
| **2016 AWARD HONORABLE MENTION** | **Millimeter-wave GaN HEMTs with Cavity-gate Structure Using MSQ-based Inter-layer Dielectric**<br>Shiro Ozaki[1,2], Kozo Makiyama[1,2], Toshihiro Ohki[1,2], Yoichi Kamada[2], Masaru Sato[1,2], Yoshitaka Niida[1,2], Naoya Okamoto[1,2], and Kazukiyo Joshin[1,2]<br>*[1]Fujitsu Limited, [2]Fujitsu Laboratories Ltd.* |
| **2016 BEST STUDENT PAPER** | **Simulation of Fabrication- and Operation-Induced Mechanical Stress in AlGaN/GaN Transistors**<br>Sameer Joglekar[1], Chuanxin Lian[2], Rajesh Baskaran[2], Yan Zhang[2], Tomás Palacios[1], and Allen Hanson[2]<br>*[1]Massachusetts Institute of Technology, [2]MACOM Technology Solutions Inc.* |
| **2016 BEST STUDENT HONORABLE MENTION** | **Nonalloyed Refractory Metals for Self-Aligned InP HBT Emitter Contacts with InAs/InGaAs Emitter Cap**<br>Ardy Winoto, Junyi Qiu, and Milton Feng<br>*Department of Electrical and Computer Engineering, University of Illinois* |
| **2015 AWARD WINNER** | **High Power Plastic Packaging with GaN**<br>Quinn D. Martin, *MACOM Technology Solutions, Inc.* |
| **2015 BEST STUDENT PAPERS** | **A CMOS-compatible Fabrication Process for Scaled Self-Aligned InGaAs MOSFETs**<br>Jianqiang Lin, Dimitri A. Antoniadis, and Jesús A. del Alamo, *MIT* |
| | **Measuring the Thermal Conductivity of the GaN Buffer Layer in AlGaN/GaN HEMTs: Effect of Carbon and Iron Doping**<br>M. Power[1], J. W. Pomeroy[1], Y. Otoki[2], T. Tanaka[2], J. Wada[2], M. Kuzuhara[3], W. Jantz[4], A. Souzis[5], and M. Kuball[1], *[1]University of Bristol, [2]Hitachi Metals, [3]University of Fukui, [4]SemiMap Scientific Instruments, [5]II-VI Wide Bandgap Group* |
| **2014 AWARD WINNER** | **GaAs Wafer Breakage Reduction**<br>Shiban Tiku, Bruce Darley, Manjeet Singh, Ernesto Ambrozio and Patrick Santos, *Skyworks Solutions Inc.* |
| **2014 AWARD HONORABLE MENTION** | **GaN Reliability – Where we are and where we need to go?**<br>G.D. Via, *Air Force Research Laboratory* |
| **2014 BEST STUDENT PAPER** | **Stability and Temperature Dependence of Dynamic $R_{ON}$ in AlN-Passivated AlGaN/GaN HEMT on Si Substrate**<br>Zhikai Tang[1], Sen Huang[2], and Kevin J. Chen[1], *[1]Hong Kong University of Science and Technology, [2]Institute of Microelectronics, Chinese Academy of Science* |

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| **2014 BEST STUDENT HONORABLE MENTION** | **Surface Recombination and Performance Issues of Scaling Submicron Emitter on Type-II GaAsSb**<br>Huiming Xu, Eric Iverson, and Milton Feng, *University of Illinois at Urbana-Champaign* |
| **2013 AWARD WINNER** | **Characterization and Control of Insulated Gate Interfaces on GaN-Based Heterostructures**<br>Tamotsu Hashizume[1,2] and Masamichi Akazawa[2], *[1]Research Center for Integrated Quantum Electronics, Hokkaido University, Japan, [2]JST-CREST, Japan.* |
| **2013 AWARD HONORABLE MENTION** | **Yield Learning of a GaAs-Based High-Throw Count Switch for Handset Applications**<br>Tertius Rivers, Corey Nevers, Chi-Hing Choi, and Hui Liu, *TriQuint Semiconductor, Hillsboro, Oregon, USA.* |
| **2013 BEST STUDENT PAPER** | **600V High-Performance AlGaN/GaN HEMTs with AlN/SiNx Passivation**<br>Zhikai Tang, Sen Huang, Qimeng Jiang, Shenghou Liu, Cheng Liu, and Kevin J. Chen, *Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong* |
| **2013 BEST STUDENT HONORABLE MENTION** | **Improvement in Enhanced Spontaneous Emission of Resonant Cavity Light Emitting Transistors via Inductively Coupled Plasma Etching Top Distributed Bragg Reflector**<br>Mong-Kai Wu, Michael Liu, and Milton Feng*, Department of Electrical and Computer Engineering University of Illinois, Micro and Nanotechnology Laboratory, Urbana, IL, USA.* |
| **2012 AWARD WINNER** | **Improving Front Side Process Uniformity by Back-Side Metallization**<br>Kezia Cheng*, Skyworks Solutions, Inc.* |
| **2012 BEST STUDENT PAPER** | **Impact of Step Edges on Trapping Behavior in N-polar GaN HEMTs**<br>Nicole Killat[1], Michael J. Uren[1], Seshadri Kolluri[2], Stacia Keller[2], Umesh K. Mishra[2], and Martin Kuball[1], *[1]University of Bristol, [2]University of California, Santa Barbara* |
| **2012 BEST STUDENT HONORABLE MENTION** | **Non-Linearity Characterization of Submicron Type-I InP/InGaAs/InP and Type-I/II AlInP/GaAsSb/InP DHBTs**<br>Huiming Xu, Eric Iverson, K.Y. (Donald) Cheng, Mark Stuenkel, and Milton Feng, *University of Illinois at Urbana-Champaign* |
| **2011 AWARD WINNER** | **Investigation and Reduction of Leakage Current Associated with Dielectric Gate Encapsulation in AlGaN/GaN HFETs**<br>S. A. Chevtchenko, P. Kurpas, N. Chaturvedi, R. Lossy, and J. Würfl, *Ferdinand-Braun-Institut* |
| **2011 BEST STUDENT PAPER** | **Type-II DHBTs Microwave Characterization and Metallization Issues**<br>Kuang-Yu (Donald) Cheng and Milton Feng, *University of Illinois at Urbana-Champaign* |

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| **2011 BEST STUDENT HONORABLE MENTION** | **Impact Ionization in AlGaN/GaN HEMTs with InGaN Back-barrier**<br>Nicole Killat[1], Milan Ťapajna[1], Mustapha Faqir[1], Tomas Palacios[2], and Martin Kuball[1], *[1]University of Bristol, [2]MIT* |
| **2010 AWARD WINNER** | **Benchmarking of Thermal Boundary Resistance of GaN-SiC Interfaces for AlGaN/GaN HEMTs: US, European and Japanese Suppliers**<br>Martin Kuball, Nicole Killat, Athikom Manoi, and James W. Pomeroy, *University of Bristol* |
| **2010 AWARD HONORABLE MENTION** | **Ultra-Thin Barrier Layers for mm Wave Frequencies in III-N HEMT Technologies**<br>J. K. Gillespie[1], A. Crespo[1], K. Chabak[1] M. Kossler[1], V. Trimble[1], M. Trejo[1], G. D. Via[1], B. Winningham[1], B. Poling[2] and D. Walker, Jr.[2], *[1]Air Force Research Lab, [2]Wyle Labs.* |
| **2010 BEST STUDENT PAPERS** | **Enhancement-mode Pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs with InAlP Native Oxide Gate Dielectric**<br>Xiu Xing and Patrick J. Fay, *University of Notre Dame* |
| | **High Performance InAlN/GaN HEMTs on SiC Substrates**<br>Han Wang[1], Jinwook W. Chung[1], Xiang Gao[2], Shiping Guo[2], and Tomas Palacios[1], *[1]Massachusetts Institute of Technology, [2]IQE RF* |
| | **Ultra-Low Ohmic Contacts to N-Polar GaN HEMTs by In(Ga)-Based Source-Drain Regrowth by Plasma MBE**<br>S. Dasgupta, Nidhi, D. F. Brown, T. E. Mates, S. Keller, J. S. Speck, and U. K. Mishra, *University of California, Santa Barbara* |
| **2009 AWARD WINNER** | **Opportunities for Development of a Mature Concentrating Photovoltaic Power Industry**<br>Sarah Kurtz, *National Renewable Energy Laboratory* |
| **2009 BEST STUDENT PAPERS** | **Lifetime Estimation of Intrinsic Silicon Nitride MIM Capacitors in a GaN MMIC Process**<br>Sefa Demirtas[1], Jesus A. del Alamo[1], Donald A. Gajewski[2], and Allen Hanson[2]<br>*[1]Massachusetts Institute of Technology, [2]Nitronex Corporation* |
| **2009 BEST STUDENT PAPERS (cont)** | **Field Dependent Self-Heating Effects in High-Power AlGaN/GaN HEMT** M. Hosch[1], J. W. Pomeroy[2], A. Sarua[2], M. Kuball[2], H. Jung[3], and H. Schumacher[1], *[1]Ulm University, Institute of Electron Devices and Circuits, [2]H.H. Wills Physics Laboratory, University of Bristol, [3]United Monolithic Semiconductors* |
| **2008 AWARD WINNER** | **Measuring Lift-off Quality and Reliability with Special Test Structures** William Roesch and Dorothy June M. Hamada, *TriQuint Semiconductor* |

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| **2008 BEST STUDENT PAPERS** | **Nano-scale Type II InP/GaAsSb DHBTs to Reach THz Cutoff Frequencies**<br>William Snodgrass and Milton Feng, *University of Illinois* |
| | **Pre-passivation Plasma Surface Treatment Effects on Critical Device Electrical Parameters of AlGaN/GaN HEMTs**<br>David J. Meyer, Joseph R. Flemish, and Joan M. Redwing, *Pennsylvania State University* |
| **2007 AWARD WINNER** | **The Role of Substrate Dislocations in Causing Infant Failures in High Complexity InGaP/GaAs HBT ICs**<br>T. S. Low[1], K. W. Alt[1], R. E. Yeats[1], C. P. Hutchinson[1], D. K. Kuhn[1], M. Iwamoto[1], M. E. Adamski[1], R. L. Shimon[1], T. E. Shirley[1], M. Bonse[1], F. G. Kellert[1], D. C. D'Avanzo[1], A. Wibowo[2], S. Hassler[2], N. Pan[2], G. Hillier[2], H. Badawi[3], M. Young[3], and W. Liu[3], *[1]Agilent Technologies, [2]Microlink Devices, [3]AXT, Inc.* |
| **2007 BEST STUDENT PAPERS** | **Development of Simple Electrolytes for the Electrodeposition and Electrophoretic Deposition of Pb-free, Sn-based Alloy Solder Films**<br>Chunfen Han, Qi Liu, and Douglas Ivey, *University of Alberta* |
| | **AlGaN/GaN High Electron Mobility Transistors and Diodes Fabricated on Large Area Silicon on Poly-SiC (SoPSiC) Substrates for Lower Cost and Higher Yield**<br>T. J. Anderson, F. Ren, L. Voss, M. Hlad, B. Gila, S. J. Pearton, J. Kim, and J. Lin, *University of Florida,* and P. Bove, H. Lahreche, J. Thuret, and R. Langer, *Picogiga, International* |
| **2006 AWARD WINNER** | **Recent Progress of Highly Reliable GaN-HEMT for Mass Production** Toshihide Kikkawa, Kenji Imanishi, Masahito Kanamura, and Kazukiyo Joshin, *Fujitsu Laboratories, Ltd.* |
| **2006 BEST STUDENT PAPER** | **Improvements in the Process for Electrodeposition of Au-Sn Alloys**<br>Nasim Morawej, Douglas G. Ivey, and Siamak Akhlaghi, *University of Alberta* |
| **2005 AWARD WINNER** | **Outstanding Issues in Compound Semiconductor Reliability**<br>Bill Roesch, *TriQuint Semiconductor* |
| **2005 BEST STUDENT PAPER** | **Investigation of Metal Contact Stacks for Submicron GaN HEMT**<br>Y. Knafo, I. Toledo, I. Hallakoun, J. Kaplan, G. Bunin, T. Baksht, B. Hadad, and Y. Shapira, *Tel-Aviv University and Gal-El (MMIC)* |
| **2004 AWARD WINNER** | **Trends in RF and Wireless Packaging**<br>Karlheinz Bock, Juergen Wolf, Herbert Reichl, *Fraunhofer Institute for Reliability and Microintegration* |
| **2004 BEST STUDENT PAPER** | **Junction Temperature and Thermal Resistance of Ultrafast Submicron InP/InGaAs SHBTs**<br>Walid Hafez, Richard Eden, Forest Dixon, and Milton Feng, *University of Illinois* |
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# MESSAGE FROM THE TPC CHAIR

A year ago the CS MANTECH executive committee made the difficult but necessary decision to cancel the 2020 Conference. Given the information we had at that time, we were hopeful that our live event scheduled for May 24-27, 2021 in Orlando, FL would offer the MANTECH community a chance to gather again to share our experiences – technical and otherwise – from the Pandemic of 2020.

Clearly that goal was too optimistic …

Over the past year, we have all become quite familiar with remote work and remote meetings. Rather than cancel another CS MANTECH Conference, our decision this year was to dive head-first into the new frontier of virtual conferences. We were not paving new ground in the broader technical community; however, this was a new challenge for most of the all-volunteer CS MANTECH executive committee. It's been interesting to learn how much of the conference could be kept, and which elements just wouldn't work. In the end, I believe we have put together a conference that is engaging, serves our core mission of providing a forum for members of the compound semiconductor community to exchange and discuss new ideas, and is appropriate for the virtual format forced upon us.

While the format of this year's conference is definitely different, we have included as many familiar elements from our in-person events as possible. We start the week on Monday, May 24th with a full day of Workshop presentations focused on Gallium Nitride, covering topics such as epi material development, device modeling, device design and processing, electrical measurements, and packaging. Our workshop presenters are experts in their respective fields, drawn from both academia and industry. We are pleased to be "co-located" again this year with the JEDEC-sponsored Reliability of Compound Semiconductors (ROCS) Workshop. ROCS will run in parallel with the MANTECH Workshop on Monday. The CS MANTECH and ROCS Workshops will both be presented live, accessible to registered attendees through our conference platform.

This year's CS MANTECH Conference features 46 presentations organized into nine sessions spread over three days. Each day includes a single-track morning session, followed by a generous break before starting parallel sessions in the afternoon. Tuesday begins with two invited plenary speakers: Dr. Mark Rosker from DARPA will present "Next Revolution in Semiconductor Materials," followed by Professor Jeehwan Kim from MIT who will discuss "Challenges and Opportunities in Remote Epitaxy for Releasable Epilayers on Graphene." Wednesday and Thursday also start with invited plenary speakers: Dr. Phillip Neudeck from NASA Glenn Research Center will describe "Progress Towards Prolonged IC Deployment into Previously Inaccessible Hostile Environments Via Development of SiC JFET-R ICs" to kick-off the day on Wednesday, and Thursday opens with Dr. Naoteru Shigekawa presenting "Low-Temperature Direct Wafer Bonding Innovating CS Device Technologies." These invited plenary speakers will present their work live; all other conference presentations will be pre-recorded. The afternoon sessions each include six presentations, and cover topics such as epi manufacturing and test, wafer processing, process control, device technologies including GaAs, GaN, SiC, photonic devices, and filters. A live question and answer Zoom Webinar will be held at the end of each day featuring the authors from the afternoon sessions, and moderated by the session chairs.

Even though we are not able to hold the vibrant Vendors Exhibition that is a hallmark of CS MANTECH, we have included an opportunity for our exhibitors to submit "Vendor Presentations," similar to the Vendor Forum talks offered during our in-person conferences. These presentations are interspersed

among the technical sessions, and are available from a separate "Vendor Showcase" on the conference platform as well. I hope you'll take the time to see what's new in the CS MANTECH vendor community.

Another feature of our on-line event is the Sponsor Hall. Sponsors have historically been essential partners in supporting the annual CS MANTECH Conference, and this year is no different. Consider taking a virtual stroll through the Sponsor Hall to see what these companies have to offer, and maybe leave a "thank you" message for their support!

Last, but definitely not least, MANTECH Conferences are known as a place where we can reconnect with colleagues in the greater compound semiconductor industry. We have set-up chat rooms in the networking area where you can meet old friends and new acquaintances to discuss a presentation, ask about a technical challenge you're working on, or just catch-up on life.

If there's anything the past year has taught me it's to be cautious in predicting when we can return to "normal" – whatever that may look like. Still, I'm optimistic that in 2022 many of us, if not all of us, will be able to meet again in person. The 2022 CS MANTECH Conference is scheduled to be held in Monterey, CA from May 9-12.

Thank you for choosing to participate in the first (and hopefully last) fully virtual CS MANTECH Conference – I look forward to seeing you on-line!

**Peter Ersland**
**Technical Program Chair**
**2021 CS MANTECH**

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# SESSION 1:
# PLENARY 1

# Next Revolution in Compound Semiconductor Materials

Mark J. Rosker[1], William D. Palmer[1], Tsu-Hsi Chang[2], Joseph J. Maurer[3], Justin Hodiak[3]

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**Keywords: gallium arsenide (GaAs), gallium nitride (GaN), diamond, gallium oxide (β-$Ga_2O_3$), boron nitride (BN)**

**Abstract**

**The performance of compound semiconductor devices has reached practical limitations that requires new innovations beyond simple material and fabrication scaling. The next revolution will enable affordable, high-performance compound semiconductor technology. This will be achieved by theoretical simulations of emerging material systems, by engineering new material limits, and by leveraging silicon-like fabrication technology.**

## INTRODUCTION

Semiconductor technologies have evolved over the past seventy years with innovative approaches that have improved performance, size, weight, power, and cost for different applications. Such approaches have involved the engineering of electrons, holes, photons, and phonons across a wide variety of device architectures and operating environments. Silicon logic technology triumphed over GaAs logic technology in the 1990s, but GaAs HBT technology continues to dominate high-performance, power-efficient RF power amplifiers in today's cellular phones. This technology evolution has been fundamentally driven by intrinsic materials properties.

The most obvious technology example is bandgap engineering. The moderate 1.12 eV energy gap for silicon at 300 K supports high dopant concentrations, which has enabled various device types and electronic contacts. Compound semiconductors (CSs) have frequently been attractive alternatives because they are characterized by a larger energy gap (e.g., GaN, at 3.4 eV) or a smaller one (e.g., InAs, at 0.36 eV). In either case, the bandgap leads to desired materials characteristics, but also imposes additional challenges to appropriately engineer donors, acceptors, and surface states for good charge confinement and low contact resistance. In addition, many CS materials have direct energy bandgaps (compared to silicon's indirect energy bandgap), offering profound advantages with respect to high efficiency solid-state lasers and detectors.

In the first wave of the CS revolution (Figure 1), the U.S. government drove technology development to monolithically integrate CS devices on homogeneous substrates to enable solid state CS electronics [1]. Examples included GaAs-based MMICs for active electronically scanned arrays in the 1980s and InGaN-based light-emitting-diode (LED) to enable blue/green lasers in the 1990s. These innovations revolutionized defense systems and significantly impacted the commercial telecommunications and lighting industries.

The 2nd revolution in CS devices, also funded by the US government, was to move past homogenous to heterogenous device integration. Recognizing the semi-insulating electrical characteristics and superior thermal conductivity (e.g. compared to sapphire), SiC electronics investment began in the late 1970s by the Office of Naval Research (ONR). ONR quickly advanced SiC material synthesis and quality. Subsequent ONR investment in the 1990s demonstrated GaN-on-SiC electronics technology based on high performance GaN RF transistors on this SiC substrate. Beginning around 2000 and continuing over the next two decades, DARPA supported substrate quality advances as well as high power device development. This brought AlGaN/GaN HEMT-on-SiC technology to system adaptation in power electronics and RF electronics for both military systems and the commercial base station market. Similarly, DARPA's Antimonide Based Compound Semiconductors (ABCS) program developed µm-scale buffer layers to heterogeneously integrate dissimilar high performance AlSb/InAs channel (6.1 Å lattice family) on InP (5.8 Å) or GaAs (5.6 Å) substrates for low power, high frequency electronics circuits. Wide and narrow bandgap developments firmly established the feasibility of a heterogenous device in which the active material is grown on top of a substrate with similar lattice constant.

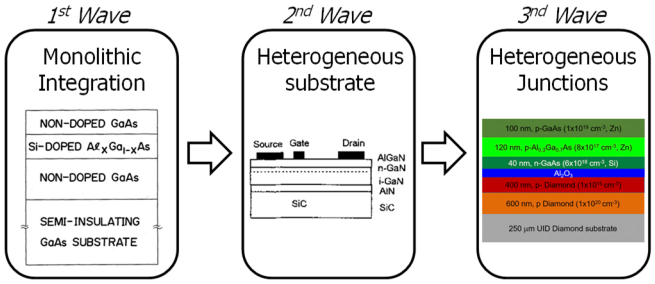


Figure 1: The three waves of the CS revolution

We suggest that the 3rd revolution in CS materials will involve heterogeneous junctions within devices at nanometer scale. The 3rd wave integration will realize abrupt junctions between high performance materials with dissimilar lattice constants within a device. Even more than the previous one, such a revolution would face daunting challenges of complexity, accessibility, and affordability, but would offer new materials characteristics with intrinsic and profound

advantages. Although we will focus here on applications to electronics, many other areas that make use of CS materials (e.g., optical, quantum, magnetic devices) could similarly benefit from this revolution.

## THE STATE OF THE ART

Because of its superior material characteristics, CS technology outperforms silicon technology in many applications, including radio-frequency (RF) electronics, high-power electronics (HPE), and optoelectronics. Table 1 highlights examples of fundamental material advantages enjoyed by CSs compared to silicon. Advantages with respect to energy band gap, carrier mobility, material breakdown field, or thermal conductivity provided the motivation of the 1st wave of CS technology revolution. In that wave, device performance was fundamental driven by material properties.

Table 1: Comparison of material properties for multiple compound semiconductors and Si CMOS.

| Parameter | Motivation | Unit | Si | GaAs | ABCS | InP | GaN |
|---|---|---|---|---|---|---|---|
| Electron Mobility | Carrier velocity | $10^3$ cm$^2$/V·s | 1.4 | 8.5 | 40 | 12 | <1 |
| $V_{peak}$ | Transit time | $10^7$ cm/s | 1 | 2 | 8 | 2.5 | 2.5 |
| $E_{BK}$ | Voltage swing | $10^5$ V/cm | 5.7 | 6.4 | 0.4 | 4 | 40 |
| $E_g$ | Charge density | eV | 1.12 | 1.42 | 0.35 | 0.74 | 3.4 |
| κ | Heat removal | W/cm·K | 1.3 | 0.5 | 0.27 | 0.05 | 2.9 |
| Maturity | Circuit complexity | | Excellent | Good | Limited | Ok | Limited |

The 2nd wave involved the leverage of heterogenous substrates to further enhance the device performance. The transistors' parasitic components (e.g., intrinsic resistances and capacitances) also became much more important factors affecting device's performance. Similar to the famous Dennard scaling rule of silicon CMOS, CS devices had also been scaled to achieve high speed, power, and power efficiency. Figure 2 shows the trend of transistor speeds ($f_T$ and $f_{max}$) for several SoA devices.

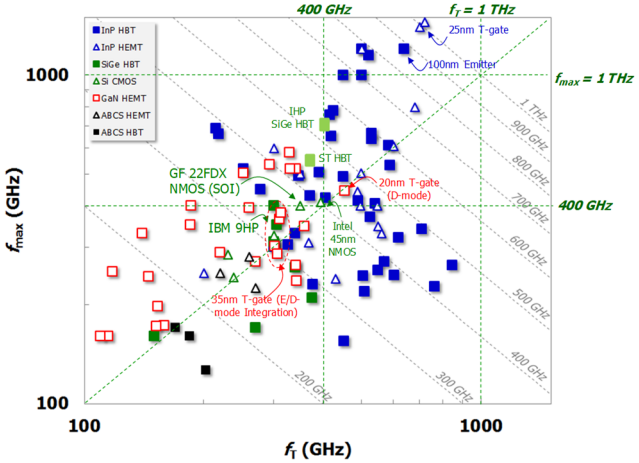


Figure 2: State-of the-art transistor speed for multiple compound semiconductors and Si CMOS.

Despite progress in CS material and device parasitic scaling, CS electronics have faced integration challenges that have limited their implementation in near-term needs, such as commercial 5G or beyond-5G systems or military wideband millimeter wave RF applications. For example, GaN-based MMICs can generate more RF output power than InP and silicon technologies around 100 GHz (as shown in Figure 3a) due to GaN's higher breakdown voltage supported by its larger energy band gap. However, the power efficiency of GaN MMICs is still relatively low compared to InP technology (Figure 3b) above millimeter wave because the GaN device access, contact, and channel resistances are intrinsically inferior to those of InP devices. To enable next-generation device performance, new integration approaches will be needed to further exploit intrinsic material advantages within a device – the 3rd wave revolution.

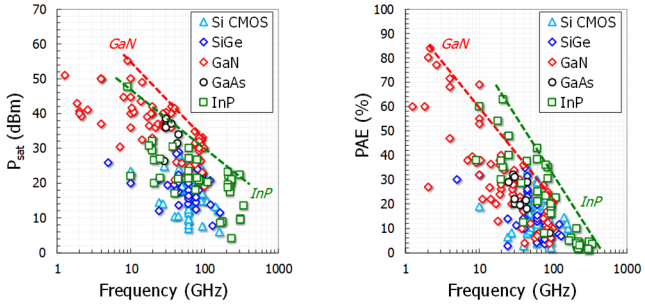


Figure 3: RF MMIC output power and Power Added Efficiency (PAE) for multiple compound semiconductors and Si CMOS.

## CHALLENGES FOR THIRD-WAVE HETEROGENOUS JUNCTIONS

We propose the next wave of revolution will start with materials innovation with the combination of advanced fabrication techniques (similar to 1st and 2nd waves) with the emphasis on integrating dissimilar materials at junctions or interfaces within a device. Further, we suggest an end-to-end (from material selection, parasitics engineering, to device performance) theoretical research framework to identify and accelerate the innovations.

Table 2 lists some emerging ultra-wide bandgap (UWBG) semiconductor materials with great promise [1], which are likely to enable future electronics with device speed, power, and efficiency advantages. However, several daunting technical challenges will need to be overcome before these unique material properties can be fully exploited.

### *Understanding Materials Physics*

Any emerging material systems, including UWBGs, are relatively new and incompletely studied. As a result, many hypotheses of material properties have not been fully assessed or proven by theoretical or experimental examination. Understanding fundamental limitations of a material system by theoretical simulation, prediction, and benchmarking is essential to decide whether further investment of device fabrication is warranted. For example, the thermal conductivity of β-$Ga_2O_3$ deserves additional fundamental

research. The Boron Nitride (BN) material system also deserves more investigations into engineering its crystal structures, e.g. from c-BN (3D) to h-BN (2D), for different thermal and electrical properties. Future research should also focus on understanding the feasibility of low-temperature synthesis with high BN material quality.

Table 2: Properties of emerging UWBG materials

| Parameter | Motivation | Unit | AlN | β-$Ga_2O_3$ | Diamond | c-BN |
|---|---|---|---|---|---|---|
| Electron Mobility | Carrier velocity | $10^3$ cm²/V·s | 0.43 | 0.15 | 4.5 | 0.83 |
| $V_{peak}$ | Transit time | $10^7$ cm/s | 1.3 | 1.1 | 1.9 | TBD |
| $E_{BK}$ | Voltage swing | $10^5$ V/cm | 154 | 103 | 175 | 150 |
| $E_g$ | Charge density | eV | 6.0 | 4.9 | 5.5 | 6.4 |
| κ | Heat removal | W/cm·K | 3.19 | 0.27 | 22.90 | 9.40 |

*Approaching Materials Property Limits*

Once the materials physics is understood, choosing appropriate material combinations for device design becomes possible. For instance, β-$Ga_2O_3$ has a large energy bandgap, which is attractive for power devices, but its thermal conductivity is currently low and theoretically it is only an n-type material. Due to these fundamental material properties, future innovations are needed to overcome these challenges and thus simultaneously realize a power device with an embedded thermal management strategy and low contact resistances to exploit the true potential of its large bandgap. In contrast, diamond has exceptional electrical and thermal characteristics, but the research community continues to struggle to identify doping techniques for electrical contacts as well as appropriate gate dielectric materials for stable operation. Such doping challenges are also common for other emerging UWBG material systems. Although preliminary device demonstrations are encouraging, to date the device performance is unfortunately limited by the electrical contact or channel access resistances.

*Increasing Material Availability*

After decades of research, both diamond and AlN have been identified as device materials that can potentially outperform GaN. However, the availability of these materials as native substrates at large size and high quality are necessary for research or production. Historically, the limiting factors determining the practicality of a semiconductor technology are the defect density and the size of the substrate. Si, GaAs, and SiC substrate technologies previously encountered similar scaling challenges. Without investment in material synthesis, purification, and large diameter wafer development, the innovation of new CS technology will be hampered.

## APPROACHES FOR THE NEXT REVOLUTION

Fast discovery of new materials, advanced fabrication tool sets, and affordable computing resources have become more available today compared to decades ago. This argues for a strategy to quickly identify the technology opportunities, accelerate the innovation, and ensure the affordability of the 3rd wave of the CS technology revolution.

(1) Exploitation of Material Limits for Applications:

New materials have been continuously proposed in the literature with unique or appealing material characteristics. However, most of the proposed materials do not have competitive properties compared to existing technical solutions. The fundamental research community should focus on the measurement of material characteristics and material synthesis techniques to identify these fundamental limits. With clear application goals in mind, the researchers should then selectively focus on those promising material candidates. For example, BN still needs more fundamental research for its low-temperature synthesis and crystal structure engineering while AlN, diamond or β-$Ga_2O_3$ may be ready for large substrate growth or high performance device demonstrations in the nearer-term.

In addition, the semiconductor industry typically focuses on applications operating around room temperature or meeting military temperature specifications (e.g. between -55 to 125 °C). In reality, such temperature ranges may not be the best operational temperatures from the material property perspective. Using β-$Ga_2O_3$ as an example, the highest electron mobility happens around 90 K. While emerging applications, such as quantum computing at cryogenic temperatures or high temperature electronics in harsh environments, new innovations can potentially engineer the best materials at those extreme temperatures.

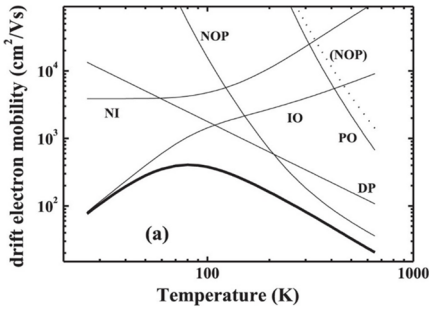


Figure 4: Simulated drift mobility of β-$Ga_2O_3$ versus temperature. (Figure courtesy of A. Parisini and R. Fornari, University of Parma, and IOP Publishing [2].)

(2) "Engineering" New Material Limits

The next step is to integrate the desired material properties *within* a device or to create a new device structure that can break the traditional device design tradeoffs. For example, an ideal RF switch must handle a large signal power range with low ON resistance and good isolation. Previously, InP HEMT technology has been used for low-loss RF switches. However, the power handling capability of these devices is poor. In fact, there is no ideal CS material to fulfill the needed specifications of emerging systems that require extremely high carrier mobility, large breakdown voltage, high charge density, and exquisite electric static gate control. However, by

leveraging the mature epitaxial growth techniques of CS, and the lower mobility GaN channel, a CS material can be stacked to form a 3D multi-channel structure with side gates to achieve extremely low ON resistance while supporting high power swing [3].

Within-device heterogeneous integration can further expand the device design space. Since only p-type diamond material is currently available and there is no mature gate dielectric options for diamond-based field effect transistors, the current usage of a diamond film is typically for its high thermal conductivity. But researchers have recently demonstrated heterogeneously integrated p-AlGaAs/n-GaAs/p-diamond epitaxial structures made by thin film transfer to form an HBT with a thin diamond collector that supports high breakdown voltages not possible with standard AlGaAs/GaAs HBTs [4].

(3) Adoption of Advanced Fabrication Processes

CS technology is generally considered to be more expensive than silicon in fabrication cost due to smaller wafer size and more expensive substrates. However, the fabrication tools of CS devices are typically relatively out of date compared to advanced silicon technology. As a result, CS devices have not been able to enjoy the advantages of advanced lithography, CMP (chemical mechanical polishing), or planarized multi-level copper interconnect process modules. The consequence of using legacy fabrication processes is that such legacy processes are not scalable for high-yield, high-performance, and low-cost production. To boost manufacturability and reduce costs, the CS industry should consider adopting silicon-like fabrication processes. Recently, reliable GaN-on-Si HEMTs fabricated in a silicon foundry was reported with competitive device performance [5], but further work and investment is required to achieve silicon-like fabrication of CS electronics.

(4) Theoretical Simulation for Technology Affordability

As the complexity of proposed innovations continues to increase, it will become economically infeasible to explore all the possibilities through expensive design of experiments and fabrication runs. However, through continued advancement in high performance computing, it becomes more affordable to first perform intensive theoretical computations, from the atomic to the circuit level, to better understand the ideal and non-ideal characteristics of channel materials, dielectrics, contacts, DC device characteristics, and RF circuit performance. The expected next-generation fully integrated TCAD (Technology Computer-Aided Design) capabilities will significantly reduce the exploration cycle and design space of experiments. Ideally, such new modeling tools will be able to predict a MMIC's transient performance, including a large signal model to capture current collapse behavior across a large range of operating frequencies, at different temperatures, or with various signal waveforms.

## CONCLUSIONS

The next revolution of CS is urgently needed to support emerging applications and new industries. A comprehensive development strategy (Figure 5) is proposed to leverage advanced computing to theoretically identify new material candidates and model transient circuit performance. To ensure future technology affordability, adoption of silicon-like fabrication modules and scaling to larger wafer sizes will be critical for the success of the next-generation of compound semiconductors.

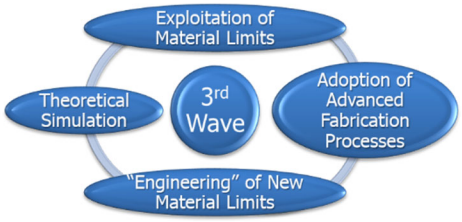


Figure 5: The 3rd Compound Semiconductor Revolution

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] Tsao, J. Y. et al., "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," in *Adv. Electron. Mater*. 2018, 4, 1600501.

[2] A. Parisini, R. Fornari, "Analysis of the scattering mechanisms controlling electron mobility in β-$Ga_2O_3$ crystals," Semiconductor Science and Technology 2016, 31, 035023.

[3] R. S. Howell et al., "Advances in the Super-Lattice Castellated Field Effect Transistor (SLCFET) for wideband low loss RF switching applications," 2016 IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA, 2016, pp. 1-3.

[4] Sang June Cho *et al.*, "Fabrication of AlGaAs/GaAs/diamond heterojunctions for diamond-collector HBTs," AIP Advances 10, 125226 (2020)

[5] S. Chowdhury et al., "650 V Highly Reliable GaN HEMTs on Si Substrates over multiple generations: Expanding usage of a mature 150 mm Si Foundry," *2019 30th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, Saratoga Springs, NY, USA, 2019, pp. 1-5.

# Challenges and Opportunities in Remote Epitaxy for Releasable Epilayers on Graphene

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**Keywords: Graphene, remote epitaxial films**

**Abstract**

**In today's talk, I will introduce a remote epitaxy technique that can produce single-crystalline membranes on graphene readily exfoliatable to form freestanding single-crystalline membranes. My group at MIT recently discovered that "any types" of single-crystalline compound materials, such as III-V, III-N, and complex oxides, can be epitaxially grown on graphene-coated substrates. The graphene is sufficiently thin such that crystalline orientation of substrates can be guided by the substrate beneath graphene. The slippery graphene surface allows the epitaxial films to be released from the substrate while the substrate can be reused. At the same time, remote epitaxial films grown on graphene can substantially reduce the density of dislocations. I will discuss how this advanced technology revolutionizes compound semiconductor technologies.**

REFERENCES

[1] Y. Kim, et al, and J. Kim, "Remote epitaxy through graphene enables two-dimensional material based layer transfer" Nature, Vol. 544, 340 (2017)
[2] W. Kong, et al, and J. Kim, "Polarity govern atomic interaction through two-dimensional materials", Nature Materials, Vol. 17, 999 (2018)
[3] S. Bae et al, and J. Kim, "Graphene-assisted spontaneous relaxation towards dislocation-free heteroepitaxy", Nature Nanotechnology (2020)
[4] S. Bae, et al, and J. Kim, "Integration of bulk materials with two-dimensional materials for physical coupling and applications", Nature Materials (2019)
[5] H. Kum, et al., and J. Kim, "Heterogeneous integration of singlecrystalline complex-oxide membranes, Nature, Vol 578, 75-81 (2020)

# SESSION 2:
# EPI MANUFACTURING AND TEST

# GaN-on-diamond design for manufacturing

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**Keywords: GaN, GaN-on-diamond, Direct Diamond Formation, HEMT, Thermal Boundary Resistance**

**Abstract: Various processes of making GaN-on-diamond have been demonstrated. Few, if any, are manufacturable at wafer scale or in volume. In this paper we discuss a few aspects that make the GaN-on-diamond by direct diamond formation manufacturable and report on the consistency of results over more than 100 wafers.**

## INTRODUCTION

Gallium nitride (GaN) high electron mobility transistor (HEMT) devices have been driving the radio frequency (RF) and power industry for years[1]. This is because of the high break down voltages achievable in this material system. However, in high power applications, HEMT devices are still thermally limited. The natural solution is to pair GaN with diamond. because diamond has the highest thermal conductivity of any bulk material.

We have made and demonstrated GaN-on-diamond material that allows devices to operate at 50W/mm [2]. In this paper we will discuss how to manufacture the structure with high yields despite the inherent material defects, manufacturing inconsistencies and diamond variability. We then show the repeatability of the results within wafers and across wafer batches.

There are a few different methods for making GaN-on-diamond: growth of GaN on single crystal diamond; bonding of fully formed GaN to fully formed diamond; and direct diamond formation (DDF) where diamond is grown onto flipped GaN. In this paper, we focus on the DDF approach, which we believe is currently the most promising for mass manufacturing.

## GAN-ON-DIAMOND BY DIRECT DIAMOND FORMATION

The process for making GaN-on-diamond was first demonstrated in 2006.[3] This process, which we continue to use, consists of taking fully formed GaN grown on <111> silicon, bonding it to a carrier silicon wafer and removing the <111> silicon substrate and transition layers, then growing in their place a diamond wafer. The process is completed by removing the carrier wafer.

Our goal is to make this process as reliably manufacturable as possible. A few points of difficulty in achieving this goal include: achieving a uniform carrier bond between the GaN grown on silicon wafer to a carrier wafer; achieving a uniformly low thermal resistance interface between the GaN and the diamond; limiting electrically active traps between the GaN and the diamond; and avoiding changes to the sheet resistance of the 2DEG after removal of the carrier wafer. A description of how each difficulty is overcome is discussed below.

Practical problems not be addressed here include the GaN strain control, diamond wafer uniformity and bow. These are too closely linked to the specific equipment to address in detail.

## CARRIER BONDING

The first hurdle to reliable manufacturing is selecting the appropriate carrier bonding method. Carrier bonding typically depends either on a low temperature organic bond or on diffusion bonding. However, since the carrier bond of the GaN wafer needs to survive diamond growth temperatures which approach 800ºC; all organic bonds are not viable. Diffusion bonds typically rely on smooth surfaces with roughness of less than 0.1nm, and are therefore not desirable. To satisfy both the exposure to high temperatures and avoid the need for extreme cleanliness, we chose to develop a glass

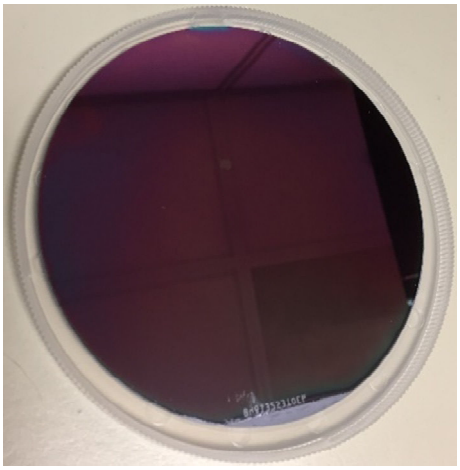

Fig. 1. Shows a 4” flipped GaN wafer onto a carrier silicon wafer. The bond is complete and the wafer laser ID can be seen near the epi flat.

bond. In this process, a custom spin on glass forms a layer of glass approximately 5um thick and has a melting point above 850ºC. This thick bond line allows the bonded wafer to survive the growth temperatures as well as being insensitive to roughness or particles up to about 5 µm in size. Figure 1 shows a wafer where the GaN epi has been flipped and the growth substrate removed.

Using this method, the bonded GaN and carrier wafer pair is flat. The bow of this bonded pair is typically lower than the spec of the epi wafer because the expansion coefficient between the growth substrate matches exactly the expansion of the carrier wafer. This flatness allows the growth substrate to be removed by a combination of grinding and etching. Grinding is important because it is faster and because wet etching is difficult since both the GaN growth and the carrier substrates both are silicon.

## THERMAL INTERFACE

Another hurdle to reliable manufacturing is achieving a uniform repeatable and low thermal resistance thermal interface. Achieving this depends on removal of the transition layers and using the appropriate adhesion layer.

The first component of a uniform thermal interface is to remove the AlGaN transition layers. Once the epi is flipped and the substrate removed, the transition layers are exposed. The transition layers are part of the GaN grown on silicon structure they are an AlGaN mixture they are thick and highly defective because of the defects and the ternary composition they have a thermal conductivity of 10W/mK which makes them the largest thermal barrier in GaN epi [4]. These allow the GaN to be grown on silicon but have no function in the final device operation. Now that the epi has been flipped, the transition layers are exposed, they can be removed which significantly reduces the thermal interface resistance between the GaN and the diamond. We use a wet etch process selective to AlGaN over GaN.

The second component of a uniform low resistivity thermal interface is the adhesion layer. Ideally there would be no adhesion layer, unfortunately, GaN exposed to diamond growth conditions is etched along defect lines and leaves an electrically-active high thermal resistance interface. We use a SiN layer as an adhesion layer. This SiN layer is critical for the electrical and thermal properties of the final GaN-on-diamond substrate. The SiN both passivates the exposed GaN N-face and protects it from the diamond growth which includes atomic hydrogen. Unfortunately, the SiN has a thermal conductivity of approximately 3W/mK while the GaN has thermal conductivity of 160W/mK and the diamond 1600W/mK, the SiN has thermal conductivity of 3W/mK. It must thus be minimized to reduce the interfacial thermal boundary resistance. The competing manufacturing priority is that the interface needs to be thick enough that the thermal properties are consistent across the wafer and that the electrical properties are maintained. To balance these competing requirements, we chose a thickness around 300 Å. We measure the interfacial thermal boundary resistance by a technique pioneered by the University of Bristol[5]. Figure 2 shows the measurement of the TBR (thermal boundary resistance) over the center three inches of a 4-inch wafer. TBR is measured in $m^2K/GW$. The theoretical minimum TBR is 7 $m^2K/GW$ the best demonstrated is around 10 $m^2K/GW$. A typical GaN on silicon wafer has a TBR above 100 here the bulk of this wafer has TBR around 23 $m^2K/GW$.

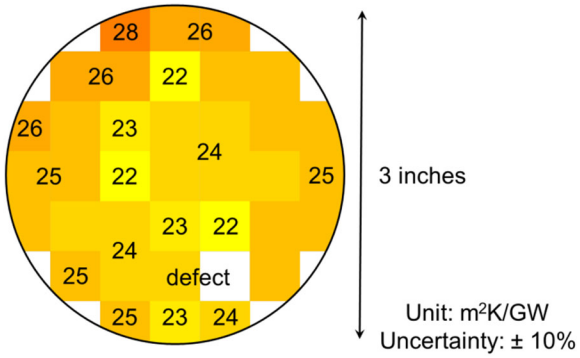


Fig. 2. Shows thermal boundary resistance measurements from a GaN-on-diamond wafer.

## LIMITING ELECTRICALLY ACTIVE TRAPS

Once the adhesion layer is deposited, the diamond is grown. It is important to verify that the interface between the GaN

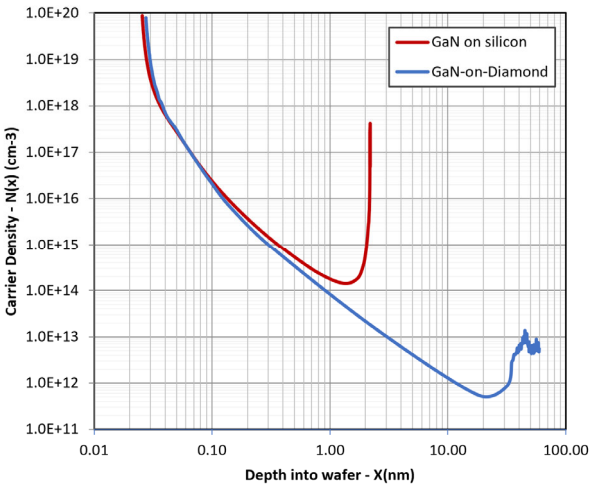


Fig. 3. Carrier density vs depth of GaN on silicon (red) and diamond(blue). From CV measurements with a 760um Hg probe.

and the diamond is not electrically active. Defects or traps at the interface between GaN and diamond would form a secondary channel which would affect the high speed or high voltage performance of devices. For GaN-on-diamond to be useful, it is not only important that the interface be thermally conductive, it is also important that it be electrically neutral.

To evaluate the electrical characteristics of our interface, we take a CV measurement of the substrate. By varying the voltage of the CV measurement, we can extract the charge density as a function of depth into the semiconductor. For comparison, we plot the charge density vs depth characteristics of the original GaN grown on silicon epi and compare to the same epi after transfer to diamond. This comparison is shown in figure 3.

The GaN on a silicon substrate in the CV measurements cannot deplete the carriers past the transition layers which are highly defective. However, measuring the same GaN after it was transferred to diamond and transition layers have been removed, the measurement can deplete the carriers deep into the diamond itself, showing no electrical traps at the GaN to diamond interface.

## SURFACE DAMAGE AND 2DEG SHEET RESISTANCE

The finally we wish to show the consistent electrical characteristics over a number wafers. The metric we chose is the sheet resistance. The sheet resistance is a good indicator of the electrical performance of the wafer and can be mapped on the GaN before and after the epi transfer to diamond. Our goal is to reproduce the electrical performance of the GaN on silicon in the GaN-on-diamond. In figure 4, we map about 100 4" wafers and plot the average wafer sheet resistance of the GaN before and after the transfer to diamond. Showing that the GaN sheet resistance has not significantly change during the epi transfer process is a good indicator that the GaN can be reliably transferred to diamond without affecting its electrical properties.

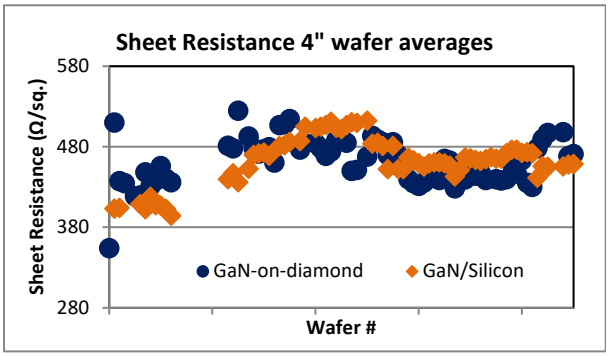


Fig. 4. Sheet resistance average on 100 wafers taken from the average of 100 measurements per wafer. Experimental wafers excluded.

## CONCLUSIONS

From the data shown we have demonstrated the DDF process with characteristics consistent with volume manufacturing. In particular, the DDF process is robust to variations in the process and initial materials while maintaining the required thermal and electrical characteristics. We show good thermal and electrical characteristics across wafers and through batches of wafers, to date we have produced over 1000 wafers using this process and have the capability of producing 100's of wafers per year.

## ACKNOWLEDGEMENTS

The author and the entire Akash GaN-on-diamond team would like to acknowledge Dr. Avi Bar-Cohen, who passed away in 2020 and was instrumental in funding the early work on this material. He will be missed.

## ACRONYMS

2DEG: 2-Dimensional Electron Gas
DDF: Diamond Direct Formation
HEMT: High Electron Mobility Transistor
CV: Capacitance Voltage

## REFERENCES

[1] http://www.semiconductor-today.com/features/PDF/semiconductor-today-june-july-2017-RF-power.pdf
[2] M. Tadjer, T. Anderson, M. Ancona, P. Raad, P. Komarov, T. Bai, J. Gallagher, A. Koehler, M. Goorsky, D. Francis, K. Hobart , F. Kub, "GaN-On-Diamond HEMT Technology With TAVG = 176°C at PDC,max = 56 W/mm Measured by Transient Thermoreflectance Imaging," in IEEE Electron Device Letters, vol. 40, no. 6, pp. 881-884, June 2019, doi: 10.1109/LED.2019.2909289.
[3] D. Francis, F. Ejeckam, J. Wasserbauer, D. Babic "Semiconductor devices having gallium nitride epilayers on diamond substrates" US Patent US67141105P April 13, 2005
[4] J. Cho et al., "Thermal characterization of GaN-on-diamond substrates for HEMT applications," 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, San Diego, CA, 2012, pp. 435-439, doi: 10.1109/ITHERM.2012.6231463.
[5] H. Sun, R.B. Simon, J.W. Pomeroy, D. Francis, F. Faili, D.J. Twitchen, and M. Kuball, "Reducing GaN-on-diamond interfacial thermal resistance for high power transistor applications", Appl. Phys. Lett. 106, 111906-1 – 5 (2015).

# Hybrid $NH_3/N_2$ Molecular Beam Epitaxy with Artificial-Intelligence-Assisted Reflection High-Energy Electron Diffraction Analysis

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**Keywords: molecular beam epitaxy (MBE), artificial intelligence (AI), reflection high-energy electron diffraction (RHEED), gallium nitride (GaN), Domm™**

**Abstract**

**Among various III-N epi growth methods, the hybrid molecular beam epitaxy (MBE) method can achieve good productivity for III-N epiwafers because it can produce an interface with excellent properties and afford a high growth rate. Furthermore, reflection high-energy electron diffraction (RHEED) analysis can be used for real-time measurements during MBE growth to obtain crystal structure information with atomic-level resolution. The crystal structure information is directly correlated to the epilayer quality and can thus be used to predict this quality. Automated RHEED analysis will be required to monitor the quality of a gallium nitride (GaN) high-electron-mobility transistor (HEMT) structure created by stacking tens of thousands of atomic layers. Toward this end, this study introduces an automated RHEED data prediction and analysis technique that employs a deep-learning-based artificial intelligence system. The results obtained by applying a machine-learning model to RHEED data for predicting the GaN HEMT quality are presented.**

## Introduction

Molecular beam epitaxy (MBE) grown III-N has been used in high performance high electron mobility transistors (HEMTs) for radio frequency (RF) applications.[1–4] With recent developments in regrown $n^+$ ohmic contacts, higher Al content (including binary) structures have been used in HEMTs and ultraviolet light-emitting diodes (UVLEDs);[4–6] this has resulted in increased interest in the use of MBE in such material systems. III-N MBE epi growth with $N_2$ plasma has been proven to be excellent for producing high-quality epi materials with abrupt interface control. However, $N_2$ plasma affords a limited growth rate compared with other techniques. To overcome this limitation for gallium nitride (GaN) MBE, IVWorks has developed a hybrid III-N MBE growth process that uses both $N_2$ plasma and ammonia sources. In this process, the $N_2$ plasma is applied for critical layers and the ammonia source affords a higher growth rate for thicker bulk layers.

Normally, reflection high-energy electron diffraction (RHEED) cannot be used for monitoring the entire MBE growth process of As, P, or Sb owing to the RHEED screen coating. Because As, P, or Sb exists as a solid at room temperature, it can be condensed and coated on RHEED screen that are cooler than ambient. Fortunately, in the III-N material system, N exists as a gas at room temperature, so there is no screen coating. In particular, RHEED can be applied to monitor and capture the entire GaN MBE growth process history for analysis and process control. In this light, the present study uses a novel artificial intelligence (AI)-assisted technique for analyzing RHEED patterns during MBE growth.

## Overview of Domm™ AI Epitaxy System

Domm™ is a patented AI technology that applies deep-learning algorithms for the detection and classification of RHEED patterns in an entire epi growth process. Specifically, a machine-learning model is used to analyze the collected

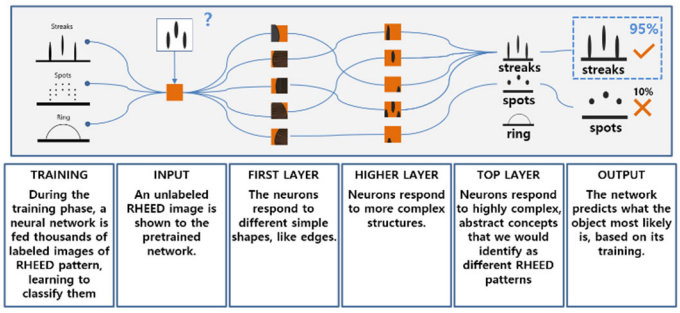


Fig. 1. RHEED pattern recognition by deep-learning based AI Epitaxy System, Domm™

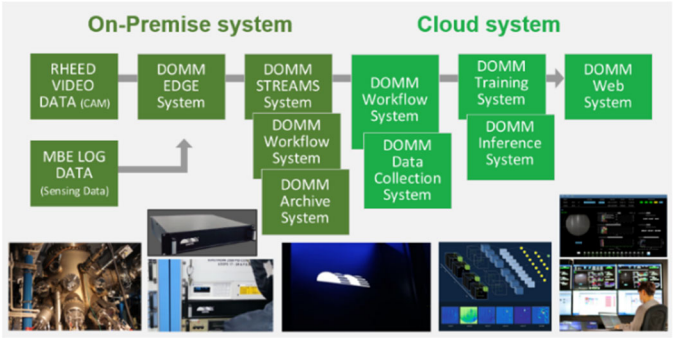


Fig. 2. Architecture of AI Epitaxy System, Domm™

data, such as the diffraction patterns throughout the entire structure, pattern transitions according to the growth mode and growth conditions, and equipment status. The correlations among the RHEED patterns, growth conditions, and final epiwafer quality are fed back to train Domm™ to create prediction models. This enables Domm™ to predict the quality of the growth process in real time before it is completed. Such information can be used to recommend recipe corrections to engineers when the predicted process quality is less than desired or to eventually correct a recipe autonomously to maximize productivity.

### Prediction of Silicon Substrate Deoxidation

In a heteroepitaxial system such as GaN on Si or SiC, the surface condition of the substrate and the deoxidation process are important steps in determining the epiwafer quality. For GaN grown on Si by MBE, the thermal deoxidation temperature of Si(111) is 700°C, and the RHEED pattern is known to change from 1×1 to 7×7.

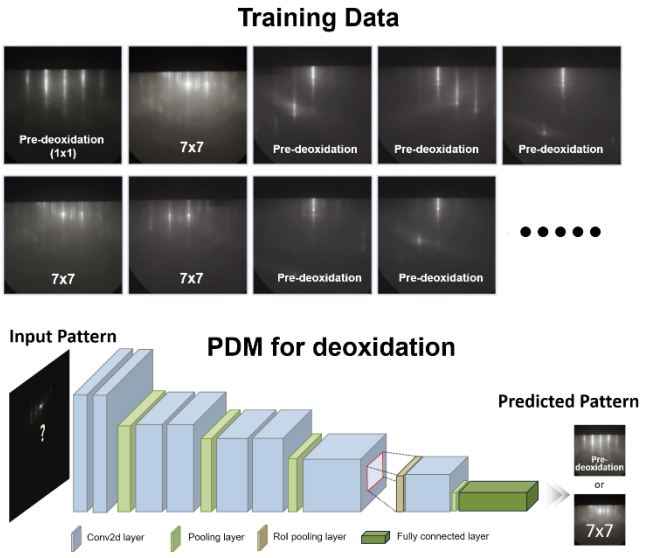


Fig. 3. Neural network architecture of PDM for deoxidation

Fig. 3 shows the training data and neural network architecture of a deep-learning-based pattern detection model (PDM) that was trained with various RHEED patterns of the Si(111) deoxidation process. The trained PDM could then detect RHEED patterns measured in real time during the deoxidation process and classify them by quantifying their probability-based similarity.

Fig. 4 shows the probability of achieving a 7×7 RHEED pattern during the deoxidation process using the PDM in Domm™. For a normal deoxidation process, the PDM predicts pre-deoxidation with almost 100% probability for all input RHEED images at a substrate temperature below 520°C. At higher substrate temperatures, the probability of predicting a 7×7 RHEED pattern increases rapidly; in particular, above 680°C, all input RHEED images are predicted as 7×7. By

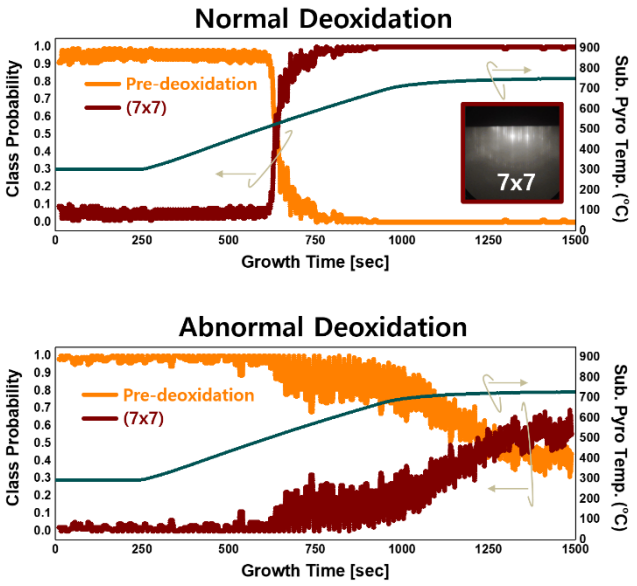


Fig. 4. Probability of achieving 7×7 RHEED pattern in two different runs

contrast, for an abnormal deoxidation process, the probability of predicting a 7×7 RHEED pattern decreases significantly with changes in the substrate temperature, indicating the occurrence of an abnormality.

### Prediction of AlGaN/GaN HEMT Growth

Fig. 5 shows the training data and neural network architecture of the PDM trained with RHEED patterns measured during the MBE growth of a GaN HEMT. In the MBE growth of III-N materials, the V/III ratio affects the

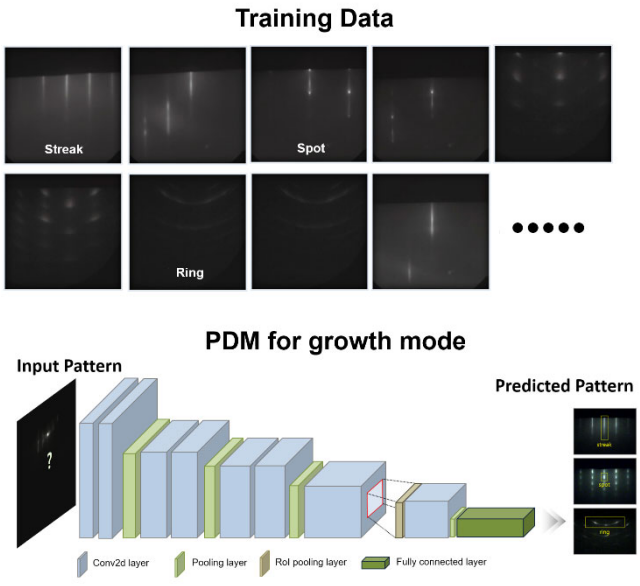


Fig. 5. Neural network architecture of PDM for growth mode

growth mode, and changes in the growth mode can be monitored through the RHEED patterns. When the RHEED pattern is a streak and a spot, the growth mode is 2D and 3D single crystalline, respectively.

Fig. 6a and 6b show the results of using the PDM to monitor the changes in the RHEED patterns when the $NH_3$ flow rate for the i-AlGaN buffer layer during the growth of a GaN HEMT was 760 and 460 sccm, respectively. The RHEED pattern was predicted using a PDM (Fig. 5) trained by inputting real-time RHEED patterns of the growth mode for the complete growth process of a 2.5 µm GaN HEMT structure. For the $NH_3$ flow rate of 760 sccm (Fig. 6a), the input RHEED patterns for the i-AlGaN buffer layer (3-4 region) were predicted as streaks with almost 100% probability. An atomic force microscopy (AFM) morphological analysis of the grown GaN HEMT epiwafer confirmed the step flow growth mode. By contrast, for the $NH_3$ flow rate of 460 sccm (Fig. 6b), the growth was less than ideal. The RHEED patterns look good during the first half of the growth process; this agrees with the prediction of streak patterns using Domm™. However, before time stamp 3', Domm™ sensed subtle changes and predicted a deteriorated surface. The result was indeed a spot RHEED pattern, and AFM revealed a high roughness.

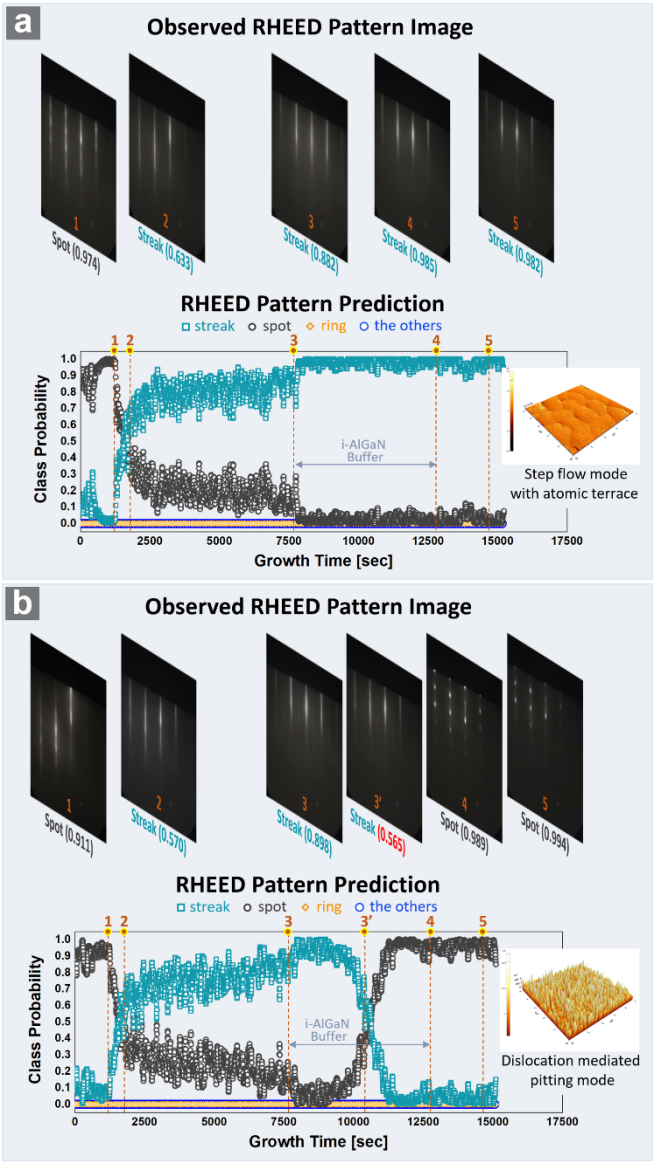


Fig. 6. Evolution of RHEED patterns during HEMT growth with $NH_3$ flow rates of (a) 760 sccm and (b) 460 sccm in i-AlGaN buffer

This demonstration clearly shows that the AI-assisted RHEED technique can be used to monitor and predict an epilayer surface before an engineer could detect its deterioration. The engineer can then adjust the growth condition or abort the growth process to minimize the loss of time and resources.

## Prediction of Crystal Quality

RHEED can be used for real-time measurement and analysis of an MBE-grown epilayer surface to provide its crystal structure information with atomic-level resolution. Because the crystal structure information directly influences the epilayer quality, the quality can be predicted by analyzing the real-time RHEED data. Fig. 7 shows the training data and neural network architecture of the crystalline-quality prediction model (CPM) for predicting the X-ray diffraction (XRD) full width at half maximum (FWHM) (102), which

| | |
|---|---|
| **Training Data Set** | • RHEED intensity<br>• Class probability of PDM for deoxidation<br>• Class probability of PDM for growth mode<br>• Growth condition and sensing data<br>• XRD FWHM (102) |

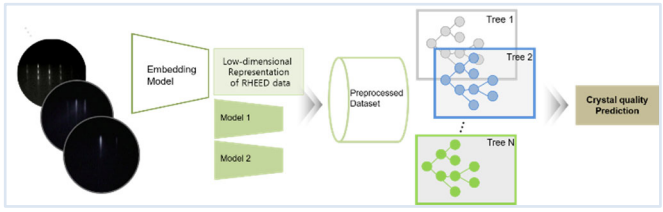


Fig. 7. Neural network architecture and training data of CPM

indicates the crystallinity of the GaN HEMT structure.

The CPM was trained using the RHEED intensity, PDM data, growth conditions, and MBE sensing data that were automatically collected using Domm™ during the growth of GaN HEMTs. It was also trained using the XRD FWHM (102) collected through measurements after the completion of the growth process. Fig. 8 shows a 2D vector space representation of the CPM prediction results for approximately 20,000 cases. Low and high (high and low quality) XRD FWHM (102) values, which indicate crystallinity, are indicated in gray and

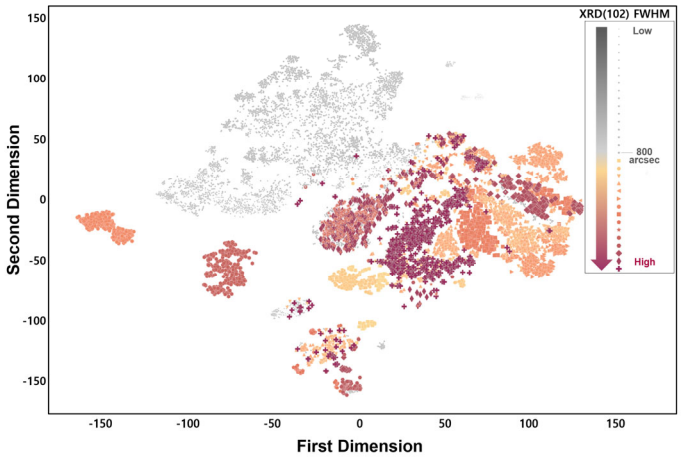


Fig. 8. Prediction result of CPM trained using dataset shown in Fig. 7

red, respectively. The gray values, indicating high quality with an FWHM of 800 arcsec or lower, were seen to be mostly grouped. This suggests that the CPM trained using the dataset shown in Fig. 7 provides excellent FWHM prediction results. Specifically, the CPM provided a high accuracy of 81.7%, precision of 74.1%, recall of 99.3%, F1 score of 84.8%, and area under curve (AUC) of 81.1%.

## Summary and Advanced Capabilities of Domm™

The Domm™ deep-learning-based AI system was used to autonomously analyze and predict the quality of MBE-grown GaN HEMTs using RHEED data. Specifically, a deep-learning-based PDM was used to analyze the deoxidation process and AlGaN buffer layer growth mode of the Si(111) substrate during GaN HEMT epi growth. Further, a CPM trained using the RHEED intensity, PDM results, MBE sensing data, and XRD FWHM (102), which indicates the crystal quality of the GaN HEMT epiwafer, verified the excellent quality of the prediction result. We are developing a sheet resistance prediction model that is trained using lattice space information obtained from RHEED patterns. We will apply this technique to key layers during GaAs MBE growth. The use of RHEED analysis for As/P/Sb MBE growth may be somewhat limited owing to concerns about the screen coating, and only critical layers are monitored.

IVWorks will continue developing Domm™ to realize fully autonomous MBE growth control. Once the AI-assisted technique detects deviations in the RHEED patterns, it will adjust the recipe in real time to ensure that desirable results are obtained. Currently, Domm™ can be applied to GaN/SiC and GaN/Si HEMTs, and RHEED video and material results are being collected to train Domm™ to predict multiple epiwafer parameters. We expect that the fully developed Domm™ will be able to reduce the cost and improve the yield of GaN MBE growth through its monitoring/predicting capabilities.

## References

[1] A. K. Oki, M. Wojtowicz, B. Heying, et al., *GaN Technology for Millimeter Wave Power Amplifiers*, ECS Transactions (The Electrochemical Society), 50(3), 2012.

[2] P. Altuntas, et al., *Power Performance at 40 GHz of AlGaN/GaN High-Electron Mobility Transistors Grown by Molecular Beam Epitaxy on Si(111) Substrate*, IEEE Electron Device Letters, 36(4), April 2015.

[3] J. LaRoche, W. Hoke, et al., *Performance and Reliability of GaN MISHEMTs and MMICs Fabricated From GaN Grown on High Resistance <111> Si Substrates By Molecular Beam Epitaxy*, 2013 CS MANTECH Conference, May 2013.

[4] A. Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, D. F. Brown, et al., *GaN Technology for E, W and G-Band Applications*, IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2015.

[5] Y. Cao, V. Kumar, S. Chen, Y. Cui, S. Yoon, E. Beam, et al., *Qorvo's Emerging GaN Technologies for mmWave Applications*, 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020.

[6] Y. Liao, C. Thomidis, C. Kao, T. D. Moustakas, *AlGaN Based Deep Ultraviolet Light Emitting Diodes with High Internal Quantum Efficiency Grown by Molecular Beam Epitaxy*, Applied Physics Letters, 98(8), 081110, 2011.

## Acronyms

MBE: Molecular Beam Epitaxy
RHEED: Reflection High-Energy Electron Diffraction
GaN: Gallium Nitride
HEMT: High Electron Mobility Transistor
AFM: Atomic Force Microscopy
AI: Artificial Intelligence
PDM: Pattern Detection Model
CPM: Crystalline-Quality Prediction Model

# Commercial N-polar GaN on SiC HEMT Epitaxial Wafers Manufactured by MOCVD for 5G mm-Wave Applications

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**Keywords: N-polar gallium nitride, silicon carbide, HEMT, MOCVD, 5G, millimeter wave**

**Abstract**

**We report the MOCVD manufacturing of N-polar GaN on 100 mm SiC HEMT epitaxial wafers suitable for ultra-high performance 5G mm-wave applications. The wafers exhibit very high 2DEG electron mobility and excellent material characteristics. Pulsed I-V test on processed HEMTs at 25 and 150 ºC showed very little dispersion and charge trapping.**

## INTRODUCTION

N-polar GaN high electron mobility transistors (HEMT) have emerged as a prime candidate for fifth generation (5G) radio frequency (RF) and millimeter-wave (mm-wave) applications. The reversed internal polarization field in N-polar GaN enables several advantageous device designs over the incumbent Ga-polar GaN [1-3]. Based on a "deep recess" structure, researchers at the University of California at Santa Barbara (UCSB) have demonstrated that a N-polar HEMT can deliver a constant 8 W/mm power density at 10, 30, and 94 GHz with record efficiencies [1], and the 94 GHz data is better than the state-of-the-art Ga-polar devices by more than a factor of 2 [2].

We have previously reported the manufacturing of such a N-polar HEMT on a 100 mm sapphire substrate by metalorganic chemical vapor deposition (MOCVD) [4]. Since mid-2020, N-polar GaN on 100 mm SiC has also entered development and is currently being sampled to several customers in the US.

## MATERIALS GROWTH AND CHARACTERIZATION

The production tool is a commercial MOCVD reactor that can handle 100 – 200 mm substrates. The reactor performance and epi characteristics are monitored by various statistical process control (SPC) charts. Real-time growth monitoring includes the wafer temperature, wafer curvature, and growth rate. Post growth material characterizations include wafer bow, epitaxial film thickness, atomic force microscopy (AFM), X-ray diffraction (XRD), Candela surface scan, impurity and dopant concentrations, sheet resistance ($R_{sh}$), two-dimensional electron gas (2DEG) charge and electron mobility, etc.

Figure 1 (a) and (b) present the schematics of a deep recess HEMT and a conventional planar HEMT, respectively. The thick unintentionally doped (UID) GaN cap within the deep recess HEMT serves to reduce DC-to-RF dispersion and enhance the sheet charge and mobility in the access region [1,2]. Figure 2 (a) shows a typical $R_{sh}$ contour map measured on a deep recess HEMT using a Lehighton eddy current tool, and the mean $R_{sh}$ is 234.3 Ω/sq with a nonuniformity of 2.2%. The typical 2DEG electron mobility measured on a deep recess HEMT using a contactless Lehighton microwave Hall is ~1850 $cm^2/V{\cdot}s$, and the TLM mobility measured along the

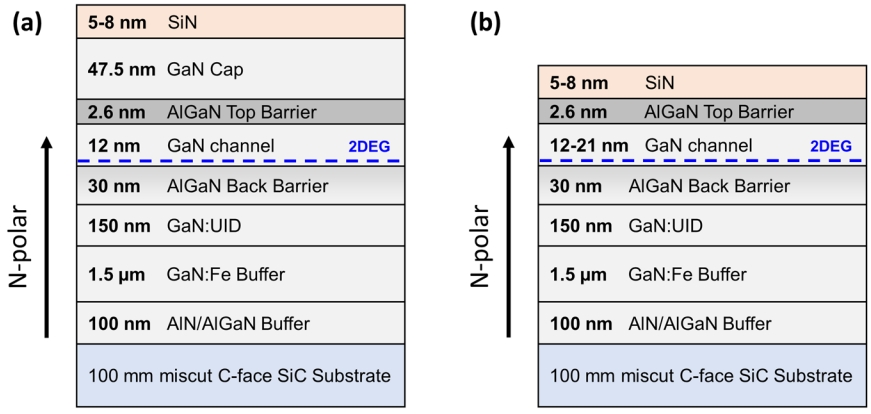


Fig. 1. Schematics of N-polar HEMTs on SiC: (a) a deep recess HEMT with a thick GaN cap on top of a 12nm GaN channel, and (b) a conventional planar HEMT with a 12 – 21 nm GaN channel.

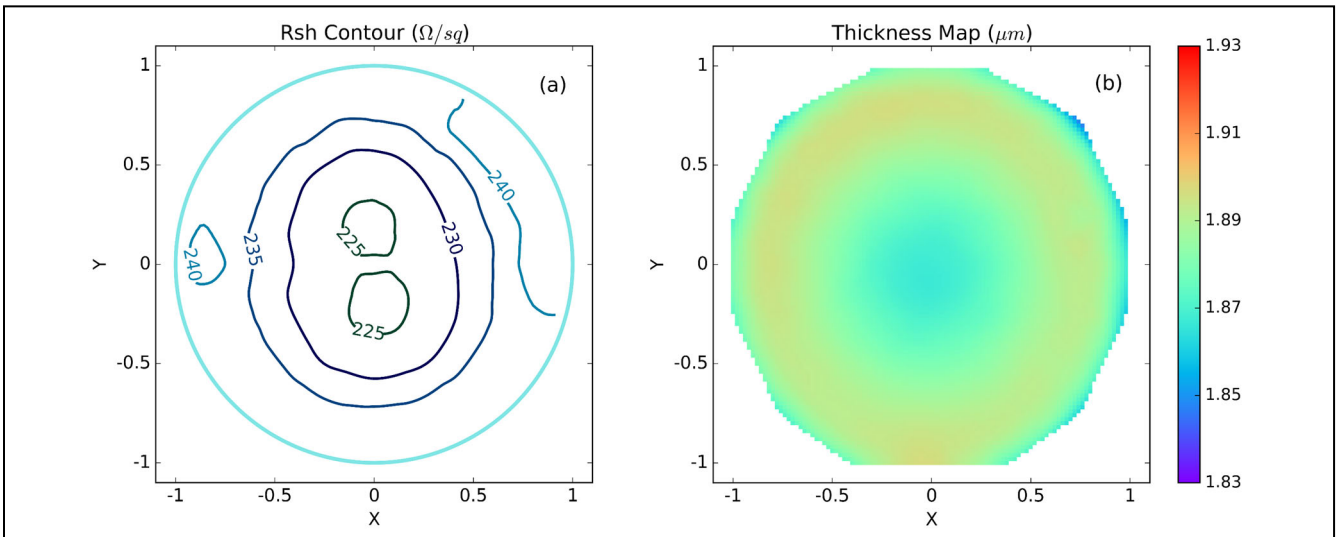


Fig. 2. (a) Typical Lehighton $R_{sh}$ contour map (mean: 234.3 Ω/sq, nonuniformity: 2.2%), and (b) typical thickness map (mean: 1.88 µm, nonuniformity: 0.5%) of a deep recess N-polar GaN HEMT on 100 mm SiC.

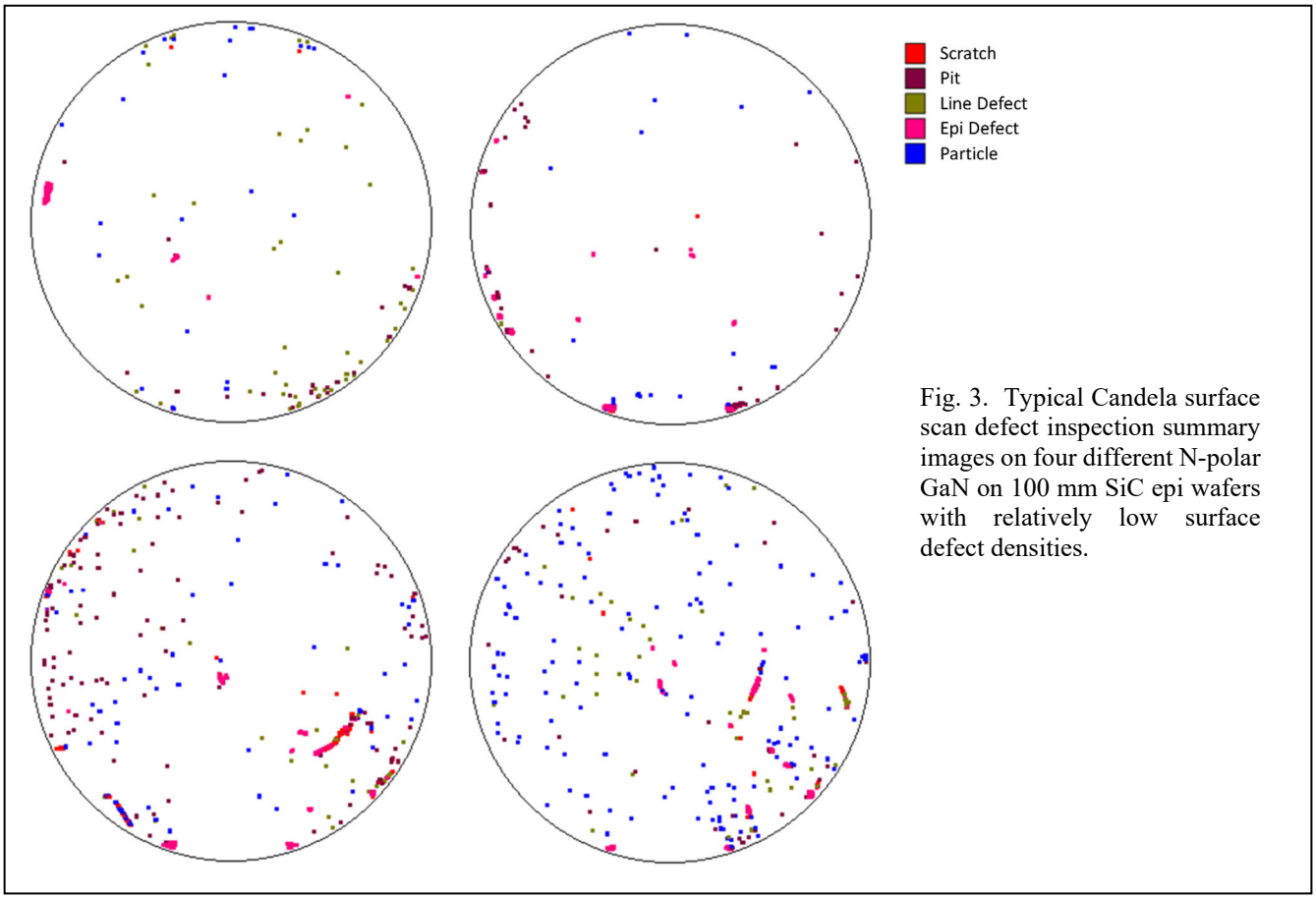


Fig. 3. Typical Candela surface scan defect inspection summary images on four different N-polar GaN on 100 mm SiC epi wafers with relatively low surface defect densities.

surface steps resulting from the SiC miscut is 10-20% higher than the Hall mobility [3]. Figure 2 (b) shows a typical thickness map of N-polar GaN on 100 mm SiC measured by spectroscopic reflectometry. The mean thickness is 1.88 µm with a nonuniformity of 0.5%.

All N-polar GaN on 100 mm SiC epi wafers and the SiC bare substrates pre-epi were scanned using a Candela 8520 system. Figure 3 presents typical defect inspection summary images on four different epi wafers with relatively low surface defect densities. Common defects including scratches, pits, line defects, epi defects, and particles are classified and plotted on the defect wafer maps. Scratches and epi defects have relatively large defect areas and distinct patterns that can be readily identified. Pits and particles can be distinguished based on the defect area ratio between the normal and oblique scatter channels, as well as their different signatures in the topography channel. Line defects are unique to the N-polar GaN epi, which only runs parallel to the surface steps. Further defect classifications are possible by using more sophisticated binning rules [5]. The quality of the C-face miscut SiC substrate is often crucial in achieving good N-polar GaN epi, and we are currently working with the SiC substrate vendors to better understand the correlation.

## DEVICE FABRICATION AND CHARACTERIZATION

To assess the performance of the N-polar GaN on SiC epitaxial materials, we have fabricated and tested planar MIS-HEMT devices based on the structure presented in Fig. 1 (b). The fabrication process started with the deposition of source and drain ohmic contacts, which consisted of a n+ GaN regrown by MOCVD and a non-alloyed Ti/Al metal stack. A first 120-nm SiN passivation was deposited by PECVD. The gate-trench was realized by selectively etching the passivation and stopping on the *in-situ* SiN gate dielectric. A Ti/Al metal stack was deposited as the gate contact. The nominal gate length ($L_G$), source-to-gate distance ($L_{SG}$), and gate-to-drain distance ($L_{GD}$) are 0.8, 1.0, and 2.0 µm, respectively. The devices were isolated using mesa isolation. Each transistor comprises of 2x75 µm gate fingers. The finger width is oriented perpendicular to the substrate miscut steps, so that the 2DEG current flows with highest mobility in the direction parallel to the miscut steps. The final device is passivated with 1 µm PECVD SiN to suppress surface charge trapping effect commonly associated with GaN devices, so that the trapping evaluation is on the epi material rather than that induced by the fabrication process.

To evaluate the dynamic behavior and lack of charge trapping effects, we measured pulsed I-V output characteristics on planar MIS-HEMTs structures at chuck temperatures of 25 and 150 °C. The measurements were acquired using a commercial system with separate pulse heads to simultaneously pulse the gate and drain. The pulsed current was measured by averaging a 200-ns window within a 650-ns bias pulse-width with a 1-ms delay between pulses.

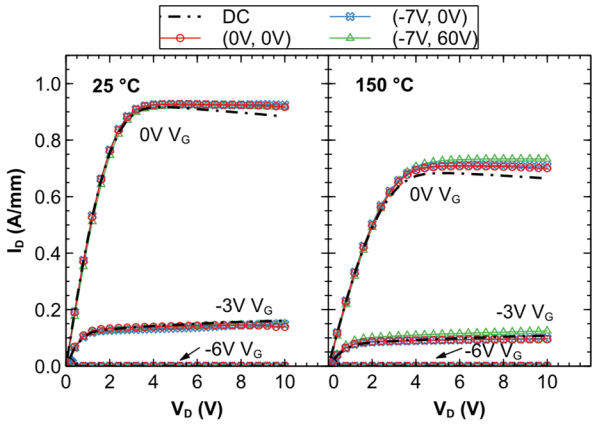


Fig. 4. DC and pulsed IV measurements acquired at probe chuck temperatures of 25 °C (left) and 150 °C (right). The pulsed measurements are taking at 25 °C there is effectively no deviation in the current characteristics with 60 V $V_{DQ}$ and the gate pinched off at -7 V $V_{GQ}$. Similarly, at 150 °C the pulsed currents are all within 4% of each other indicating no significant charge trapping effects are observed.

Initially, the pulsed I-V curves were acquired with a gate and drain quiescent bias point ($V_{GQ}$; $V_{DQ}$) of (0 V; 0 V) to examine the device behavior under no stress and no charge trapping. Subsequently, pulsed I-V curves were acquired at multiple off-state quiescent bias points to assess the dynamic behavior under stress conditions similar to those found in real applications. The quiescent gate voltage ($V_{GQ}$) was held with the channel pinched off at -7 V and the quiescent drain-bias ($V_{DQ}$) was increased from 0 V to 60 V. The results from a representative device are shown in Fig. 4. At 25 °C The saturation drain-current measured at the knee voltage is > 0.9 A/mm and is effectively unchanged when the drain quiescent bias is increased to 60 V. Similarly, at 150 °C, while the increased temperature reduces the knee current and increases the knee voltage due to the heating of the channel, the dynamic behavior is nearly unchanged, with the knee current at (-7 V; 60 V) within 4% of the current from the 150 °C (0 V; 0 V) quiescent bias point. These results indicate that no major charge trapping effects are present in the device structure, therefore indicating the good quality of the N-polar GaN epitaxial material developed at Transphorm.

## CONCLUSIONS

We report the MOCVD manufacturing of N-polar GaN on 100 mm SiC HEMT epitaxial wafers suitable for ultra-high performance 5G mm-wave applications. The wafers exhibit very high 2DEG electron mobility, excellent $R_{sh}$ and thickness uniformities, and very low Candela defect densities. Pulsed I-V test on processed HEMTs at 25 and 150 °C showed very little dispersion and charge trapping, indicating good epitaxial material quality.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] B. Romanczyk *et al*., IEEE Trans. Electron Devices **65**, 45, 2018.
[2] B. Romanczyk *et al*., IEEE Electron Device Lett. **41**, 1633, 2020.
[3] S. Keller *et al*., Semicond. Sci. Technol. **29**, 113001, 2014.
[4] X. Liu *et al*., 2020 CS MANTECH Digest, pp. 29 - 32, May 2020.
[5] V. Gupta *et al*., 2020 CS MANTECH Digest, pp. 37 - 40, May 2020.

## ACRONYMS

GaN: Gallium nitride
SiC: Silicon carbide
HEMT: High electron mobility transistor
MIS: Metal-insulator-semiconductor
5G: Fifth generation
RF: Radio frequency
mm-wave: Millimeter-wave
MOCVD: Metalorganic chemical vapor deposition
SPC: Statistical process control
2DEG: Two-dimensional electron gas
$R_{sh}$: Sheet resistance
UID: Unintentionally doped

# The Phenomenon of Charge Activated Visibility of Electrical Defects In 4H-SiC; Application for Comprehensive Non-Contact Electrical and UV-PL Imaging and Recognition of Critical Defects

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**Keywords: SiC, Triangular defects, Carrot defects, non-contact CV, corona, UV-PL**

**Abstract**

**In this work we investigate activation of the electrical visibility of defects in surface voltage images that in epitaxial 4H-SiC occurs as a result of surface charging to depletion. With increasing charge the defects become visible as sites with reduced depletion voltages. It shall be emphasized that this phenomenon does not involve any defect creation. It reveals defects in a non-invasive and completely reversible way. The invisible defect state is recovered when charge is removed from the surface. Correlation with UV-photoluminescence images prove that the electrical visibility is observed for critical yield killer triangular, downfall and carrot defects. However, the individual defects show differences in the electrical contrast and in the depletion depth corresponding to the onset of visibility. Based on the present, comprehensive study it shall be recognized that a considerable fraction of UV-PL defects in "killer categories" are not electrically active even for deep depletion.**

## INTRODUCTION

Silicon carbide development and device manufacturing require wafer screening for epitaxial layer defects. Currently this is performed with UV-photoluminescence combined with optical topographic images [1]. These techniques categorize different defects; with triangular, downfall and carrot defects considered as the most important cause of electrical failures and yield losses. However, such screening does not provide on its own any information on electrical defect activity.

A practical cost-effective answer to the need for electrical defect screening can be provided by charge based non-contact C-V metrology (CnCV) for wide bandgap semiconductors [2] and the "QUAD" method, (Quality, Uniformity, and Defect) incorporated in CnCV tools. In our previous work, we have shown whole wafer surface voltage mapping of electrical defects [3]. The present work is a continuation that focuses on the charge activation of the electrical visibility of defects. This "field-effect" type phenomenon is combined with UV-PL for quantification of defects in the most critical categories.

## EXPERIMENTAL RESULTS AND DISCUSSION

In this work QUAD measurements and UV-PL imaging were performed on the same n-type epitaxial 4H-SiC wafers. QUAD was measured with the CnCV tool, while near UV-PL images were captured using Lasertec SICA 88 tool at X-Fab.

In charge assisted QUAD, whole wafer negative corona charge deposition was used for biasing to depletion. As discussed in ref. [2], corona charging of SiC surface is non-invasive, fully reversible, and the deposited charge can be conveniently removed by wafer illumination.

Results discussed in this study are for a 150mm diameter wafer. The UV-PL defect map in Fig. 1 reveals defect counts of 107 triangular, 25 downfall, and 191 carrot defects. The sequence of QUAD surface voltage maps in Fig. 2 demonstrates the charge activated electrical visibility of defects. With increasing magnitude of deposited charge, $\Delta Q_C$, the defects are becoming visible as sites with reduced surface depletion voltage. The count of these electrical defects increases from 11 defects at low charge, $\Delta Q_C = -4e11cm^{-2}$, to 155 defects at higher charge, $\Delta Q_C = -1.6e12cm^{-2}$. Overlaying UV-PL and QUAD images, we have identified which of these electrical defects correspond to triangular, downfall, and carrot categories that are considered the most critical yield killers. The results are summarized in Table 1 and Table 2. The largest electrical activity of about 60% is demonstrated for triangular defects. However, in all three categories a considerable fraction of UV-PL defects are not electrically active.

The QUAD results in Fig. 3 show complete recovery of the initial non-visible defect state after removal of the surface charge by illumination. This proves that the presented phenomenon does not involve any defect creation.

The quantitative results on charge induced defect visualization are presented in Fig. 4.

In our practical application of the charge activation phenomenon, 2mm Kelvin probe mapping reveals defects with much smaller dimensions. The explanation involves two enabling factors: 1. charge biasing to depletion activates leakage and neutralizes charge within the defect area; 2. neutralized area around the defect site enlarges due to surface migration of charge. As a result, mapping after delay can reveal small electrical defects.

## REFERENCES

[1] H. Das et al., Materials Science Forum, 924 (2018) 261-264.
[2] M. Wilson, Compound Semiconductor, 25-6 (2019), pp. 20-26.
[3] M. Wilson et al., in CS Mantech Conference Digest 2020.

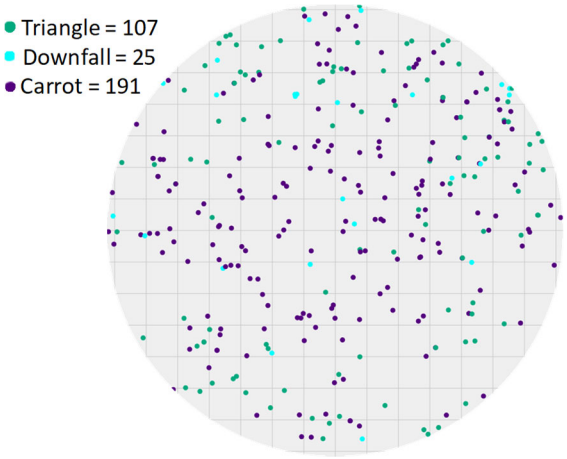


Fig. 1. UV-PL defect map on 4H-SiC wafer showing triangle, downfall and carrot defects.

Table 1. Summary table of QUAD detected defects added at each charge level identified as carrot, triangle or downfall by overlapping position on the UVPL map.

| Defect Type | Initial | Qc= -4e11 | Qc= -8e11 | Qc= -1.2e12 | Qc= -1.6e12 | QUAD Total |
|---|---|---|---|---|---|---|
| Carrot | 2 | 3 | 19 | 4 | 4 | 32 |
| Triangle | 1 | 5 | 48 | 11 | 1 | 66 |
| Downfall | 0 | 2 | 2 | 0 | 0 | 4 |
| Other/Not detected | 0 | 1 | 19 | 11 | 22 | 53 |
| Total | 3 | 11 | 88 | 26 | 27 | 155 |

Table 2. Summary table of UV-PL and QUAD detected defects including defect ratios.

| Defect Type | QUAD Defect Count | UVPL Defect counts | Ratio |
|---|---|---|---|
| Carrot | 32 | 191 | 0.168 |
| Triangle | 66 | 107 | 0.617 |
| Downfall | 4 | 25 | 0.160 |
| Other/Not detected in UVPL | 53 | | |
| Total | 155 | 323 | 0.480 |

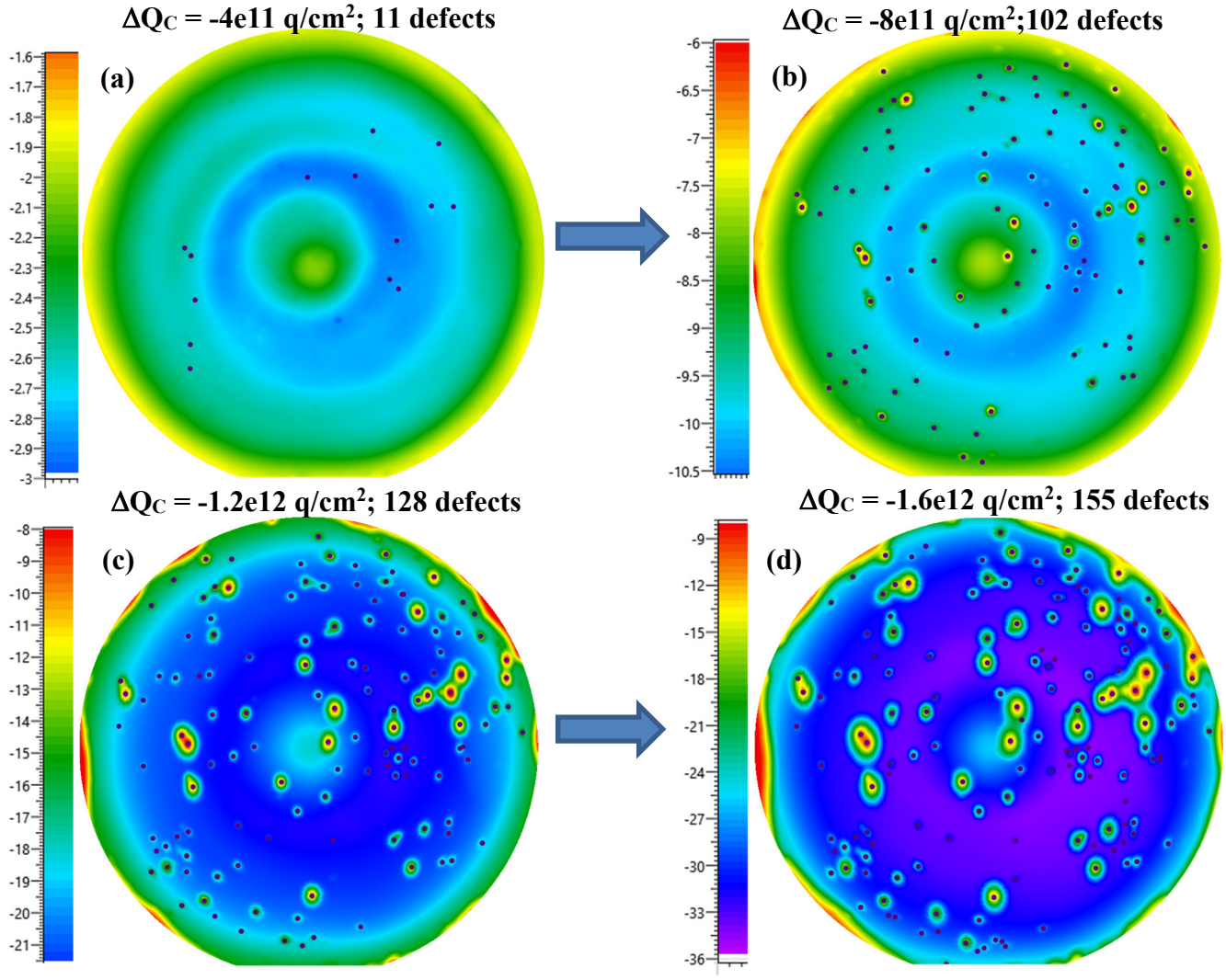


Fig. 2. QUAD surface voltage maps demonstrating charge activated defect visibility enhancement. With increasing deposited corona charge, the defects become more visible in sites with reduced depletion voltage. The defect count increases as more charge is applied: 11 defects at $\Delta Q_C$ = -4e11 q/cm$^2$ (a), 102 defects at $\Delta Q_C$ = -8e11 q/cm$^2$ (b), 128 defects at $\Delta Q_C$ = -1.2e12 q/cm$^2$ (c) and 155 defects at $\Delta Q_C$ = -1.6e12 q/cm$^2$ (d). The latter represents the high charge saturation defect count.

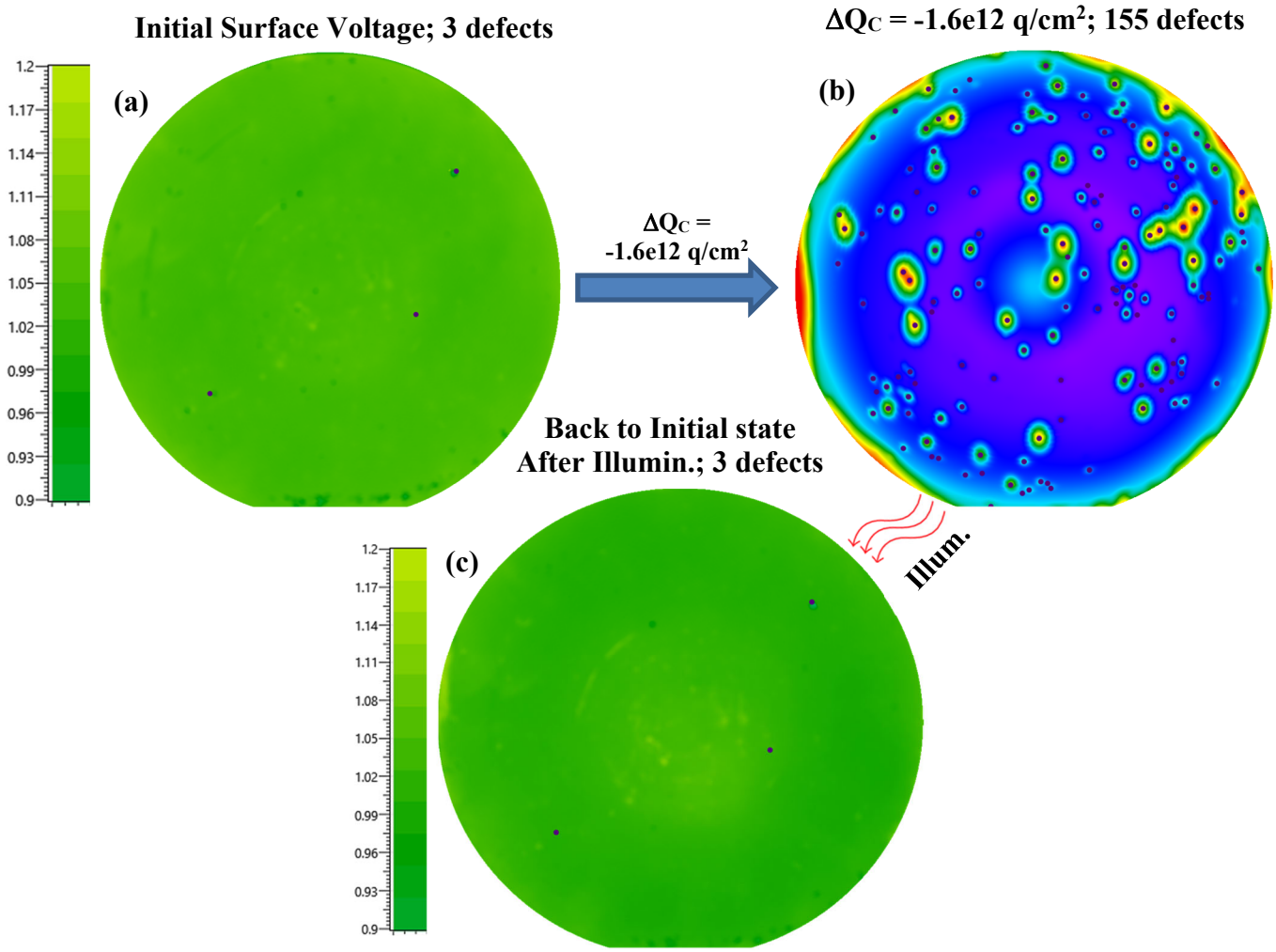


Fig. 3. After charging from the initial surface voltage state (a) to the defect revealing higher charge map (b), recovery back to the initial non-visible defect state is achieved using illumination. This indicates that this effect is not related to defect creation.

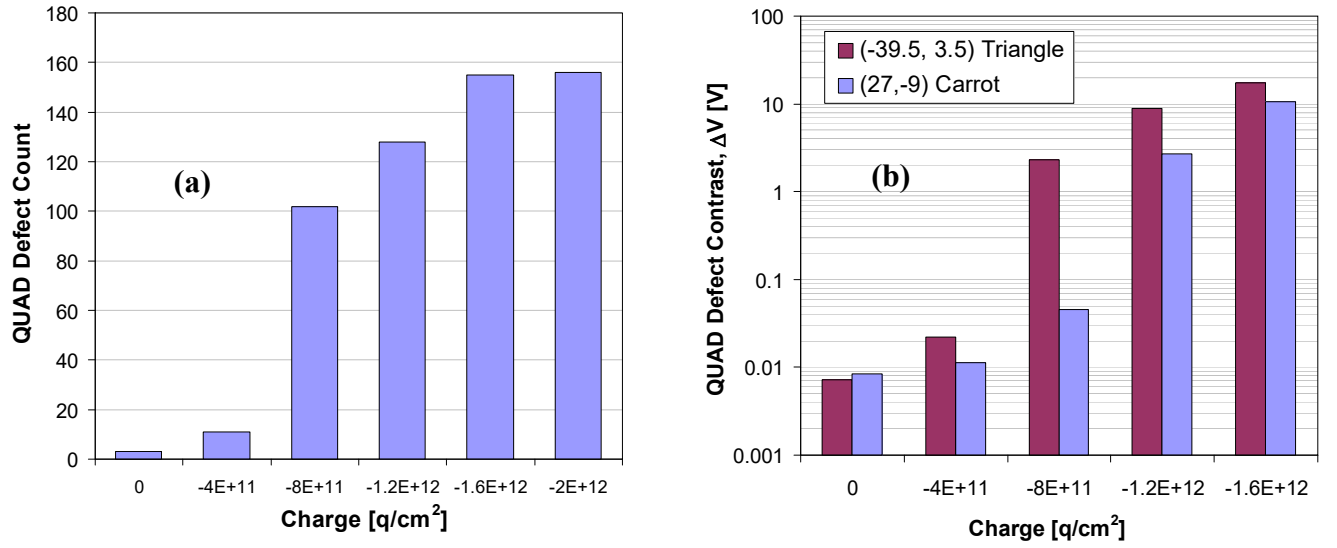


Fig. 4. With increasing corona charge bias, the defect visibility is improved as evidenced by the increase in the QUAD defect counts (a) and enhancement of QUAD defect contrast (b). The contrast is the difference between depletion voltage at defect center and region outside the influence of the defect.

# A Deep Learning-based Multi-model Method for Etching Defect Image Classification

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**KEYWORDS: CNN (Convolutional Neural Network), Deep-learning, Etching defect, Multi-model**

**Abstract**

**Many types of defects can occur during the etching process. Some defects are obvious, while others are not. In addition, the characteristics of some defect types are similar to each other. Traditionally, the classification of defect types fully relies on a well-trained engineer. To overcome the disadvantage of manual classification, we introduced a multi-model method to achieve a high-speed classification computer system.**

**We propose a multi-model classification method, which combines two models to enhance the classification property. The model consists of two InceptionV3 models. To improve the accuracy of partial classification, the second-stage is determined by some critical data from the first-stage model. Finally, we have significant accuracy improvement on metal defect data through the two-stage model.**

## INTRODUCTION

Etching quality has always been one of the most important items in quality control in the semiconductor industry. The quality of the product affects not only the price of the product, but also the purchase intention of customers. Traditionally, the quality monitoring method in the etching process uses an automatic inspection machine to detect defects, and then the engineer manually classifies the defective photos. However, inconsistent judgment standards of different engineers usually lead to inconsistent results of defect classification. In addition, the speed of personnel judgment is slow. For example, when a factory is working at full capacity, it must use a lot of human resources for defect detection, which will cost the company a lot of money, but it has not yet obtained fast and accurate judgments.

According to the special classification requirements of the factory in defect analysis, some of the defect classification results will have special judgment rules. For example, Defect type A has a higher priority than other any defect type. Therefore, "A" classification result should always be classified, when defect A and Defect B or other defect appear in the etching image at the same time. There is a high correlation by such special rules. Consequently, the accuracy of some classes can be difficult to improve when only one model is used.

Therefore, we propose a compound model to improve the accuracy which may be influenced by special classification rules. In the process, all the etching images are classified by the first-stage model, and some of the classification classes are chosen by criteria. We used these classes to classify the images in the second-stage model again. After the second model classification, we took the classification result of the second-stage model as the final answer. If the image was classified into the residual classes from first-stage model, we do not change the classification result. Our compound model structure can greatly improve the accuracy of specific classification requirements to comply with special classification rules. As demonstrated in Figure 1, the proposed architecture is constructed by two independent CNN (Convolutional Neural Network) models architectures.

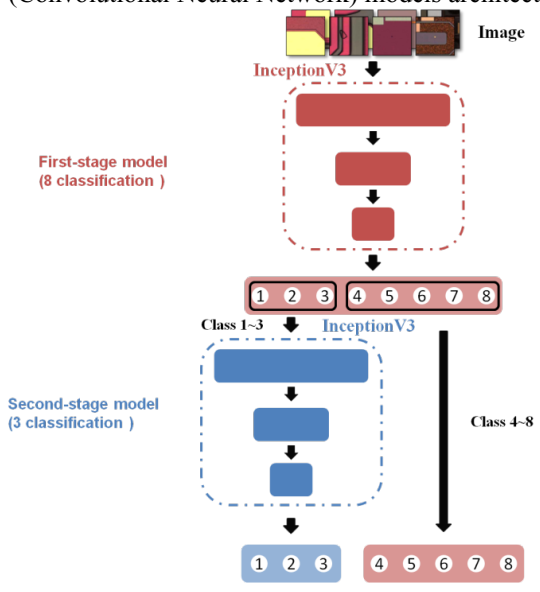


**Fig. 1.** Flowchart of the proposed deep-learning based multi-model method.

## BACKGROUND

### Image classification

Figure 2 shows 8 classes. Class 1 is Normal image w/o any Etching defect issue, and class 2 to 8 is different defect types. Class 2 is Metal scum, which is defined as any foreign matter remaining on the metal layer, such as photoresist, stains or water marks. Class 3 is Passivation scum, which defines that there are foreign matter residues on the protective layer, such as photoresist, stains or water lines. Foreign matter often remains on the protective layer and the metal layer. When it occurs at the same time, we think it should be classified in class 2. So class 2 is a special class, which has a higher priority than other defect types. The schematic diagram of such defect characteristics is shown in Figure 3 and Figure 4.

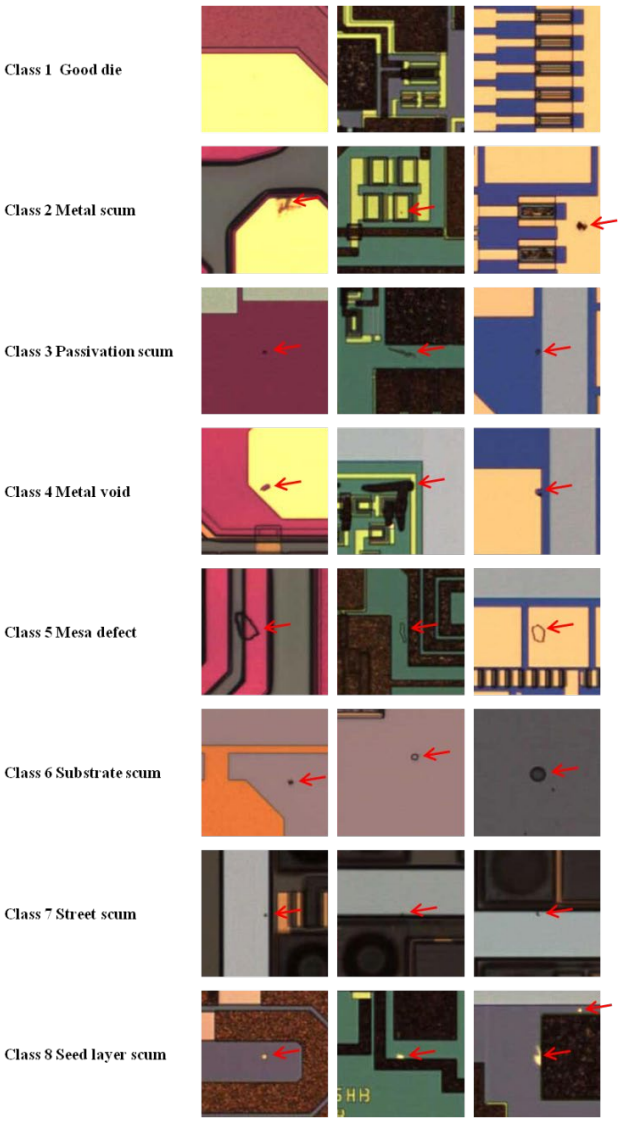


**Fig. 2.** Examples of etching defect patterns. (Defects are pointed by red arrow)

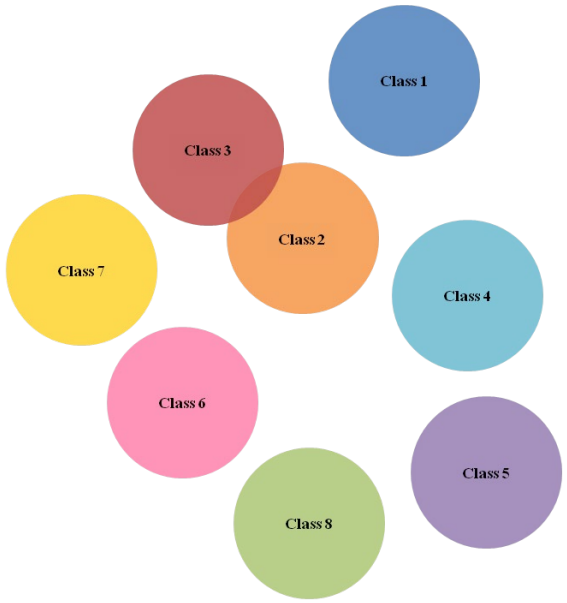


**Fig. 3.** The relationship between the different classes. Class 2 has a partial intersection with class 3.

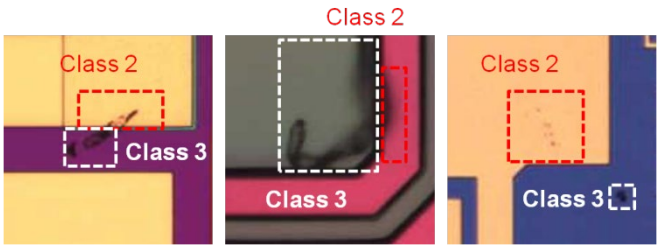


**Fig. 4.** Examples of class 2 data have a partial intersection with class 3.

## EXPERIMENT

### Image pre-processing

The image was shot by Rudolph's AVI machine. The shooting rule is comparing the image screen from the camera with the golden wafer image. Through the grayscale and brightness difference comparison between the image screen from the camera and golden wafer image, we can distinguish whether the area of image shot is flawed or not. If the difference between the grayscale and brightness is greater than the setting value, the machine will place the defect in the center and save the image automatically.

AVI camera lens has a magnification of about 10X, and the captured area of each image is about $262 \times 333$ um. However, such a wide image range is very difficult for the model to capture and learn for such a small defect. Therefore, we cropped the image and retained the center area of the image. The cropped image is shown in Figure 5.) The cropped image helps the model to learn the defect features easily, because the defect features takes a larger proportion of the entire image. It's like the features selection. We can use the more informative parameters to fit the training model.

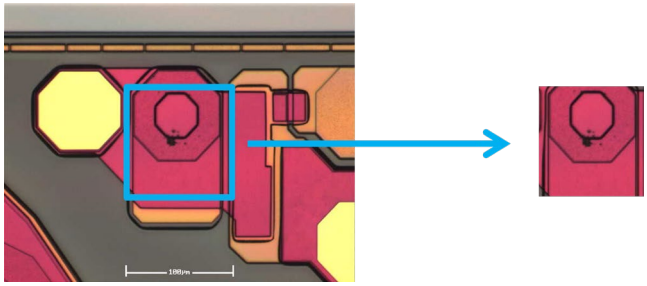

**Fig. 5.** Crop the image before model training.

Data generation

We consider the precision as well as accuracy the precision of the training model. Because of the limited number of input samples on some classes, CNN training would be over fitting on such more parameters [2]. In order to avoid reducing the precision, one solution is using the training data of the existing training set to generate more data [3]. Applying different techniques such as horizontal flip, rotation, and rotation scaling on the data set, we can create more training samples. The data expansion parameters which were used for all data sets are described in Table 1. The expansion is shown in Figure 6.

Table1. Data augmentation parameters.

| Parameter | Value |
|---|---|
| Rotational Range | -10~10 |
| Zoom Range | 0.7~1.3 |
| Vertical Flip | True |
| Horizontal Flip | True |
| Range of horizontal translation | ±5 |
| Range of vertical translation | ±5 |

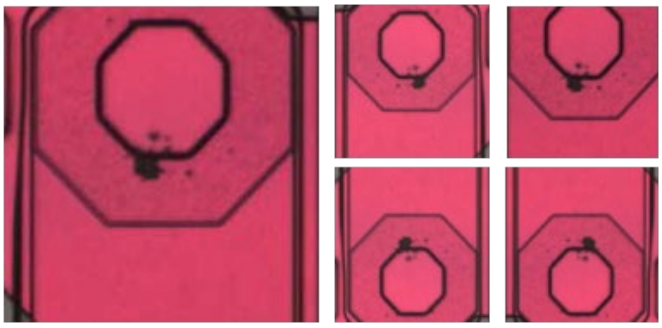

**Fig. 6.** Images obtained after data generation techniques. The left image is the original image and the right image share the artificially generated image after different data augmentation methods.

Model training settings

According to the input size of the selected InceptionV3 [1] model, we used bicubic interpolation to resize all images to 224x224 pixels. The batch size is set to 32, and the model is trained for 200 epochs. On the Adam optimizer, $^{2}1$, $^{2}2$ and learning rate are set to 0.6, 0.8 and 0.001, respectively. Also, we have modified the output of the last layer in all structure to correspond to eight classes, instead of the 1000 classes proposed by ImageNet. In addition, the network weights are initialized by the weights trained on ImageNet. The operating system is Windows with Intel(R) Core(TM) i7-9900KS 4 GHz processor with 32 GB RAM.

The training and testing have implemented the process by the proposed model in this experiment. We used the deep learning toolbox of MATLAB, and run on Nvidia GeForce GTX 2080 Ti GPU with 11GB RAM.

Result

After the two models are trained for 200 epochs, we load them and verify their accuracy. Figure 7 shows the classification results of the first-stage model. It can be seen that the accuracy of the second classification and the third classification are not as good as another classification, which are 65.7% and 83.8% respectively. As previously mentioned, such a special classification rule will affect the model learning. In the experiment results, the accuracy of classification 2 is not being as high as other classifications and it affects the accuracy of other classifications.

| | Predicted Class | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Class | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Acc |
| 1 | 293581 | 12443 | 4348 | 2282 | 993 | 1328 | 5854 | 2048 | 90.9% |
| 2 | 97302 | 482463 | 59427 | 13247 | 58033 | 5920 | 1277 | 16217 | 65.7% |
| 3 | 9579 | 11170 | 211773 | 641 | 13930 | 208 | 451 | 4988 | 83.8% |
| 4 | 1054 | 500 | 47 | 26195 | 181 | 89 | 5 | 46 | 93.2% |
| 5 | 227 | 721 | 920 | 192 | 41576 | 243 | 10 | 96 | 94.5% |
| 6 | 114 | 126 | 35 | 68 | 76 | 42136 | 0 | 3 | 99% |
| 7 | 222 | 12 | 29 | 5 | 8 | 20 | 19220 | 5 | 98.5% |
| 8 | 117 | 63 | 67 | 6 | 18 | 0 | 1 | 14183 | 98.1% |

True class

**Fig. 7.** Results of the first-stage model classification.

After we used the second-stage model to recognize again the class 1 to 3, the accuracy of these three classes has been greatly improved. The accuracy of class 2 has increased from 65.7% to 72.6%, and the accuracy of class 3 has increased from 83.8% to 89.1%. From the results, it can be clearly proved that the accuracy of a single model is enhanced by the multi-stage model without changing the first-stage model accuracy results of class 4 to 8. Figure 8 shows the accuracy result of the multi-stage model classification.

| | Predicted Class | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Class | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Acc |
| 1 | 292153 | 14545 | 3674 | 2282 | 993 | 1328 | 5854 | 2048 | 90.5% |
| 2 | 47121 | 532796 | 59275 | 13247 | 58033 | 5920 | 1277 | 16217 | 72.6% |
| 3 | 3232 | 3997 | 225293 | 641 | 13930 | 208 | 451 | 4988 | 89.1% |
| 4 | 952 | 596 | 53 | 26195 | 181 | 89 | 5 | 46 | 93.2% |
| 5 | 116 | 867 | 885 | 192 | 41576 | 243 | 10 | 96 | 94.5% |
| 6 | 69 | 171 | 35 | 68 | 76 | 42136 | 0 | 3 | 99% |
| 7 | 213 | 25 | 25 | 5 | 8 | 20 | 19220 | 5 | 98.5% |
| 8 | 92 | 87 | 68 | 6 | 18 | 0 | 1 | 14183 | 98.1% |

**Fig. 8. R**esults of combining the second-stage model classification.

## CONCLUSIONS

We propose a multi-model classification method for etching defect detection. This method of combining two models can improve the accuracy of special classification rules, while the accuracy of other classes will remain unchanged.

The experimental results showed that the proposed multi-model outperformed the single CNN model. The accuracy of Metal scum has increased from 65.7% to 72.6%, and the accuracy of passivation scum has increased from 83.8% to 89.1%. Therefore, the multi-model method based on deep learning can make full use of different model combinations to improve the prediction accuracy of the special classification rules.

## REFERENCES


[1] Szegedy, Christian, et al. "Rethinking the inception architecture for computer vision." Proceedings of the IEEE conference on computer vision and pattern recognition. 2016

[2] Hua Li, Shasha Zhuang, Deng-ao Li, Jumin Zhao, and Yanyun Ma. 2019. Benign and malignant classification of mammogram images based on deep learning. Biomedical Signal Processing and Control 51 (2019), 347–354.

[3]Sara Hosseinzadeh Kassani and Peyman Hosseinzadeh Kassani. 2019. A comparative study of deep learning architectures on melanoma detection. Tissue and Cell 58 (2019), 76–83.


## ACRONYMS

CNN: Convolutional Neural Network
AVI: Auto Visual Inspection

# Kelvin Force Microscopy and Micro-Raman Correlation Study of Triangular Defects in 4H-SiC

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**Keywords: triangular defect, KFM, Raman, defect inspection, surface voltage**

**Abstract**

**Triangular defects in epitaxial 4H-SiC are considered device performance and yield killers. This property has been linked to involvement of 3C-SiC inclusions. In the present work, we address this aspect using micro-scale compositional and electrical characterization. Thus, micro-Raman TO mode mapping is used to distinguish 3C-SiC and 4H-SiC. The results clearly demonstrate a pattern of 3C-SiC within the triangular defect. Kelvin Force Microscopy images of the same defect show patterns similar to Raman. In case of KFM the pattern shows 3C-SiC as a higher work function region compared to the lower work function 4H-SiC. Another very strong electrical effect of the 3C-SiC is observed in KFM charge assisted measurements of the depletion layer leakage and corresponding rapid depletion voltage decay after charging. Such electrical activity is consistent with the lower energy gap of 3C-SiC and may explain the detrimental effect of triangular defects on device performance.**

## INTRODUCTION

Control and elimination of extended crystal defects represent very important tasks for improving silicon carbide device performance and manufacturing yield. A great deal of attention in this area has been devoted to triangular defects. In epitaxial growth of 4H-SiC they develop easily due to incorporation of 3C-SiC inclusions and preferable nucleation of this polytype [1]. As a result of 3C-SiC inclusion and 4H-SiC overgrowth, the triangular defects may exhibit different microstructures [1]. In our recent study combining UV-photoluminescence imaging and micro-scale Kelvin Force Microscopy, we have found that micro-regions within triangular defects show different electrical activity [2].

The present study is a continuation that incorporates micro-scale Raman imaging. The micro-KFM and micro-Raman results enable us to see for the first time, a relationship between 3C-SiC Raman signal and electrical properties in the triangular defect microstructure.

## EXPERIMENTAL RESULTS AND DISCUSSION

Measurements were performed on n-type epitaxial 4H-SiC wafers with 8e15cm$^{-3}$ dopant concentration. The QUAD (Quality, Uniformity, and Defect) map of the surface voltage, shown in Fig. 1 reveals electrical defects that are manifested as sites with different voltages compared to surroundings [2,3]. The QUAD automated defect count identified 82 defects. The map in Fig. 1 was measured using a 2mm diameter Kelvin probe and a charge enhanced technique capable of revealing defects with sizes smaller than the probe, however without imaging of actual defect micro-structure. The electrical micro-structure of triangular defects is of primary interest in this study. The micro-Kelvin Force Microscopy image of the triangular defect in Fig. 2a represents the work function pattern obtained using 8μm diameter KFM micro-probe with the calibrated work function. In this image, the larger work function regions contain 3C-SiC inclusion, compared to the lower work function of 4H-SiC. The partial derivative, KFM pattern of this defect shown in Fig. 2b, reveals characteristic micro-structure elements discussed in Ref. 1.

The micro-Raman results in Fig. 3 are based on the intensity of the LO Raman mode with 797 cm$^{-1}$ and 777 cm$^{-1}$ lines representing 3C-SiC and 4H-SiC, respectively. The Raman image indicates a 3C-SiC pattern similarity to that in Fig. 2. It reveals: the downfall defect at the apex; the strong 3C-SiC intensity near the triangular top, the faceted 3C-crystal line; and finally decreasing at the base region overgrown by 4H-SiC.

The present results are consistent with the 3C-SiC involvement in the triangular defects investigated in Ref [1] and based also on Raman imaging of defect.

The KFM charge transient results in Table 1 quantify significant differences in depletion leakage current in the micro-regions. These results are based on charge bias pulsing to depletion and micro-KFM measurement of time resolved depletion voltage. The two leakage indicator parameters in Table 1 are the voltage magnitude $\Delta V$ just after charging and the current density $J_D=C_D \cdot dV/dt$ where $C_D$ is the depletion capacitance. Both quantities demonstrate a much larger leakage in the 3C-SiC region compared to the region of 4H-SiC outside the defect.

## REFERENCES

[1] J. Guo et al., Journal of Crystal Growth, 480 (2017) 119-125.
[2] M. Wilson, et.al in CS Mantech Conference Digest 2020
[3] M. Wilson, Compound Semiconductor, 25-6 (2019), pp. 20-26.

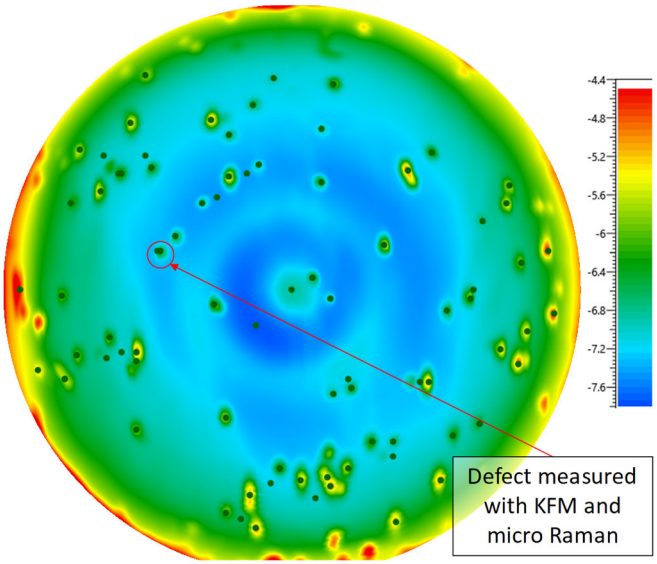


Figure 1. The QUAD map of electrically active defects in epitaxial 4H-SiC wafer.

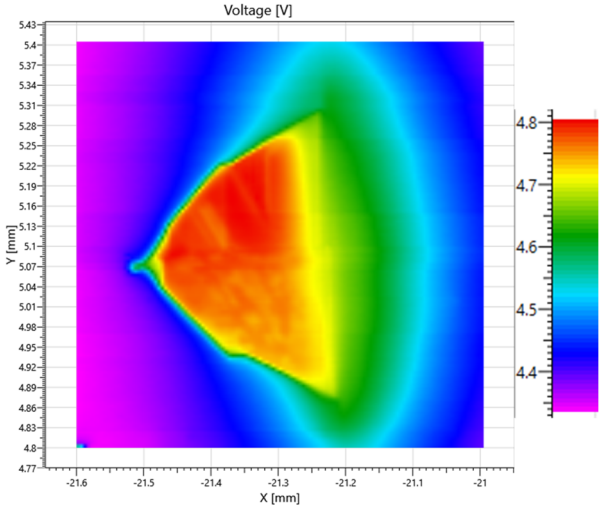


Figure 2a. Work function of a triangular defect measured with the KFM showing as much as 4.8eV for 3C-SiC within a defect decreasing to 4.3eV for 4H-SiC outside the defect.

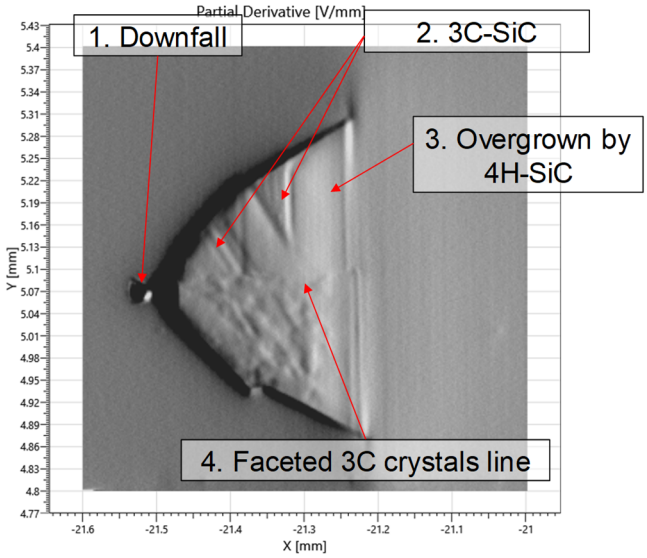


Figure 2b. 4 elements identified on the differential KFM map: downfall, 3C-SiC, faceted 3C crystals line, and the base with 3 C-SiC overgrown by 4H-SiC.

Table 1. Depletion leakage current indicators.

| Indicator | 4H-SiC outside defect | 3C-SiC region inside defect |
|---|---|---|
| Depletion voltage magnitude, ΔV; | -45V | -4.8V |
| Leakage current indicator $J_D$ at -5V (arb. units) | 0.025 | 0.20 |

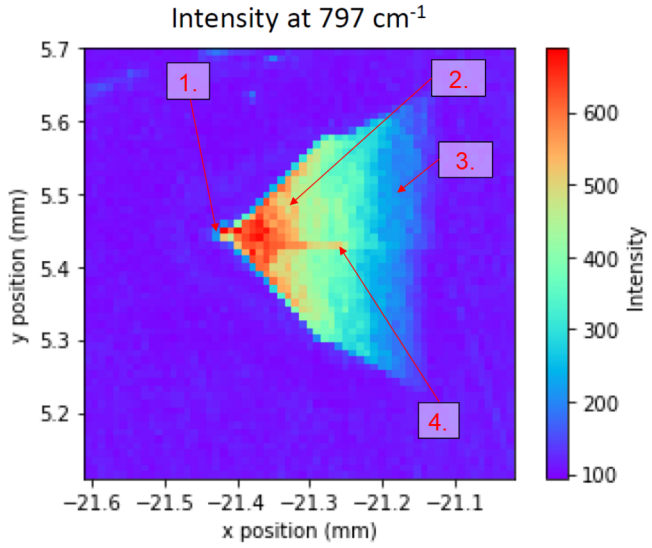


Figure 3. Micro Raman intensity of 797 $cm^{-1}$ line that corresponds to 3C-SiC.

# SESSION 3:
# PROCESS AND PACKAGING

# Fabrication of High-Performance Compound Semiconductor RF Circuits Using Heterogeneously-Integrated Transistor Chiplets in Interposers

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**Keywords: Heterogeneous Integration, Chiplet, GaN, mm-wave, RF IC, MMICs**

**Abstract**

**Heterogeneous integration technologies can greatly reduce the cost and fabrication cycle time of RF integrated circuits that rely on compound semiconductor devices. We present a technology called MECAMIC (Metal-Embedded Chiplet Assembly for Microwave Integrated Circuit), which features highly-scaled III-V transistor chiplets (e.g., GaN devices) embedded in the volume of integrated passive wafers (e.g., interposers) using a metal bonding matrix. A process design kit was developed to support the layout and simulation of the RF ICs, and circuits up to W-band have been demonstrated.**

## INTRODUCTION

Leading edge compound semiconductor device technologies are typically developed in low-volume high-mix research laboratories and foundries using state-of-the-art processes on small-diameter substrates. Scaling up to demonstrate high-performance circuits poses significant engineering challenges, which generally translates to long fabrication cycle time and low yield. Additionally, the surface area utilized by transistors in monolithic microwave integrated circuit (MMIC) designs is very small compared to the circuit area (between 1 to 10%) – the remaining area being used for inter-stage matching networks, transmission lines, decoupling capacitors, and other passive elements. None of these passive elements are making effective use of the small-diameter exquisite substrates and epi materials grown in III-V semiconductor wafers for RF applications.

As a result of these factors, heterogeneous integration technologies can provide a disruptive manufacturing model for high-performance III-V RF ICs by decoupling transistor design, development, and fabrication, from the circuit manufacturing (Fig. 1).

HRL has developed a technology called MECAMIC, which stands for Metal Embedded Chiplet Assembly for Microwave Integrated Circuits [1, 2]. Based on the wafer-level multi-chip module integration platform named MECA (Metal Embedded Chip Assembly) [3], MECAMIC enables highly-scaled heterogeneous integration of III-V transistors chiplets with Integrated Passive Device (IPD) wafers (or interposers).

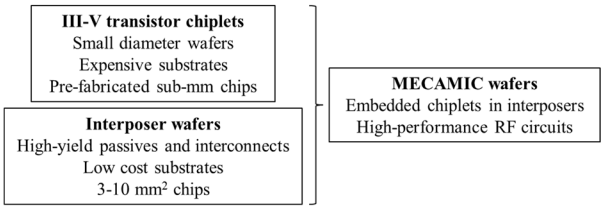


Fig. 1. Hybrid manufacturing techniques of III-V transistor chiplets such as the MECAMIC technology enables high-performance RF ICs with rapid fabrication capabilities.

Using heterogeneous integration techniques, high-performance RF ICs can be designed and fabricated using the best transistor technology for the function and combined with multiple device technologies on the same wafer. Further, hybrid manufacturing approaches such as MECAMIC reduce cycle time by pre-fabricating standards for the transistor chiplets and making them available off the shelf. Last but not least, the scaling of this technology result in comparable performance with monolithic circuits.

In this paper, we present an overview of the MECAMIC process flow, followed by key elements of the process design kit (PDK) in Microwave Office AWR, and some circuit demonstrators.

## MECAMIC FABRICATION PROCESS

The MECAMIC heterogeneous integration process is shown in Figure 2 [1]. First, the interposer wafers are designed and fabricated using 2 metal layers, TaN resistors (50Ω/□) and SiN capacitors (300 pF/mm2) and a layer of BCB dielectric (εr = 2.65). The substrate (SiC or Si) is subsequently thinned down to target thickness (e.g., 50 µm). Backside vias and chiplet cavities are etched in parallel.

Third, the transistor chiplets are placed face down on a temporary substrate. The SiC (or Si) thinned interposer wafers with pre-fabricated interconnects and passives are also temporarily bonded on the temporary substrate. A backside metallization process is used to mechanically embed the chiplets into the interposer wafer and to provide DC and RF ground. The source of the transistor chiplets can be grounded either through backside chiplet vias or by interconnecting the source pad to the grounded metallic ring surrounding the

chiplets. Additionally, the metallized backside encapsulation provides thermal management due to the material's high thermal conductivity (> 300 W/m·K). The MECAMIC wafers are then demounted from the temporary substrate, flipped, and processed with wafer-level 5-µm-thick gold plated interconnects using an air bridge process (M3). The metallic interconnects provide electrical connectivity between the transistor chiplets and the circuitry.

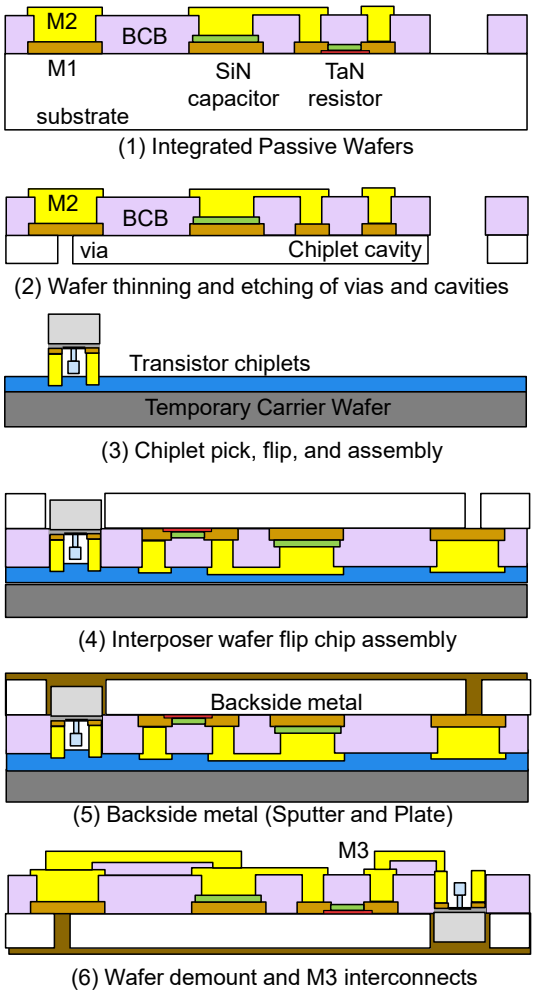


Fig. 2. MECAMIC Process Flow

The development of standardized 40 nm AlGaN/GaN HEMT chiplets to rapidly fabricate GaN circuits up to W-band are presented (Fig. 3). Such chiplets are realized by combining advances in e-beam gate processes and massively-parallel singulation techniques.

Specifically, we demonstrated a 5x decrease in e-beam cycle time through process optimization. GaN chiplets with fT > 110 GHz and Imax > 1.3 A/mm were fabricated in yielded quantities exceeding 50,000 per 4" wafer. The chiplets were singulated by plasma dicing (i.e., SiC etching) followed by a carrier-to-tape transfer approach. The chiplet design is based on HRL's scalable T3 GaN device model included in the T3 GaN PDK. Standardized off-the-shelf chiplets consist of device sizes ranging from 4x37.5 µm to 8x75 µm, which corresponds to gate peripheries ranging from 150 to 600 µm and can generally cover circuit frequency band from Ka- to W-band.

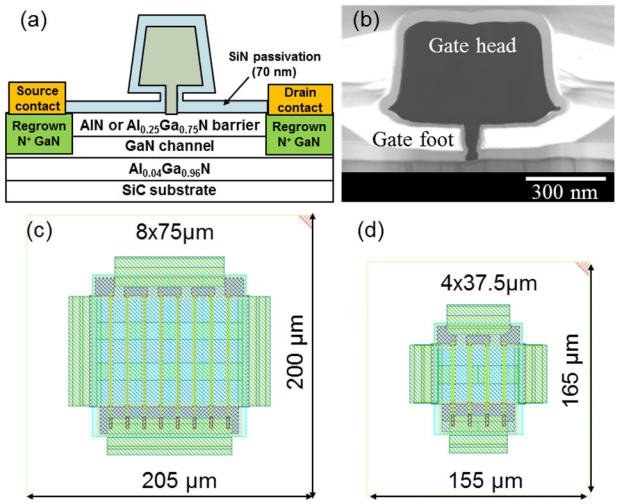


Fig. 3. T3 GaN chiplets: (a-b) 40 nm gate length T-gate structures on highly-scaled AlGaN/GaN epitaxial layer; (c-d) HEMT standardized chiplets.

Fig. 4 shows a large-area microscope image of a MECAMIC interposer wafer (Fig. 2(2)). The inset highlights the integrated passives, metal routing (M2), and chiplet cavities. The chiplet dimensional control is on the order of 2 µm, which enables accurate chiplet registration in the passive network. This process is currently being demonstrated on 3-inch-diameter high-resistivity silicon wafers (or SiC wafers), but can be scaled to large diameter wafers.

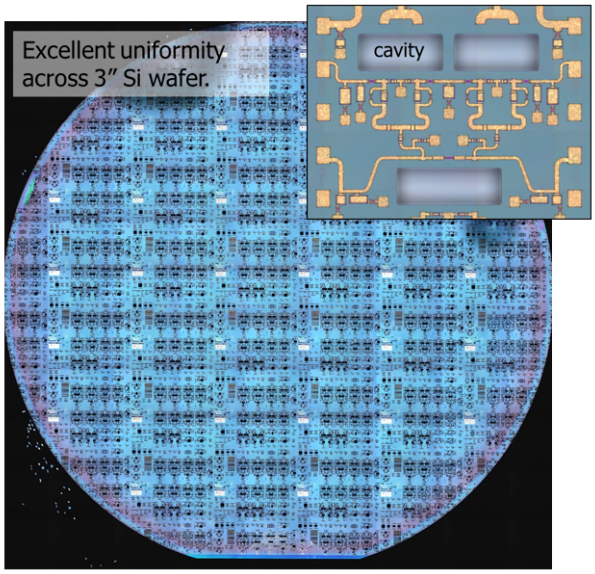


Fig. 4. MECAMIC integrated passive wafers before assembly.

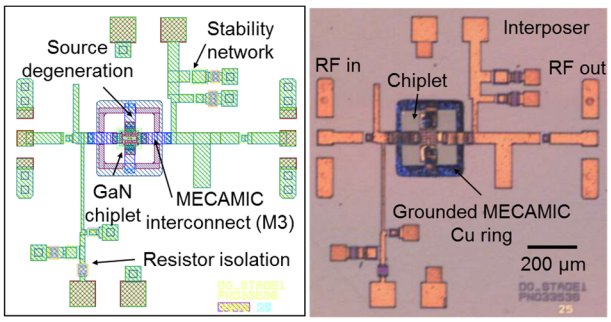


Fig. 5. MECAMIC single-stage 77 GHz circuit design and fabrication.

An example of a MECAMIC circuit with embedded GaN chiplets and MECAMIC interconnects (M3) is shown in Fig. 5. The chiplets are assembled using traditional pick and place tools. After the backside metal embedding process, the registration of the chiplet within the wafer is better than 5 µm, and the topography is comparable to the metal thickness, which is also on the order of 5 µm.

Using pre-fabricated transistor chiplets, the fabrication cycle time of GaN RF ICs was decreased by 5X when comparing the monolithic process to the heterogeneous integration approach.

## Process Design Kit (PDK)

A MECAMIC PDK was developed in Cadence AWR Microwave Office (MWO) to provide a design flow for working with multi-technology integration. The MECAMIC PDK is equipped with a palette of tools to help designers construct a MECAMIC design with a standard circuit design workflow. As with other traditional circuit design PDKs, the MECAMIC PDK has components that are pre-defined and have passed Design Rule Checks (DRCs). The design rules are critical for the success of the design-fabrication-testing workflow.

The MECAMIC PDK allows designers to use device technology PDKs available from AWR to create chiplet assemblies. These assemblies are a hierarchical integration of the device technology PDK and MECAMIC PDK. Several chiplet assemblies have been constructed in digital version and physically (off-the-shelf chiplets), allowing designers to drag and drop a chiplet from the element pallet directly onto the schematic as shown in Fig. 6. In this example, the chiplet has grounded source vias. In the layout, the chiplet is surrounded by the MECAMIC cavity/metal ring. New chiplets can also be created using the device technology PDK and be compliant with the MECAMIC chiplet design rules.

The transistor chiplets are connected to other chiplets (from the same or from a different device technology) using the interposer with MECA interconnects, which are parameterized cells and available in the MECAMIC PDK palette as shown in Fig. 7. Optimization can be performed using AWR Analyst for more accurate Electro-Magnetic (EM) simulations.

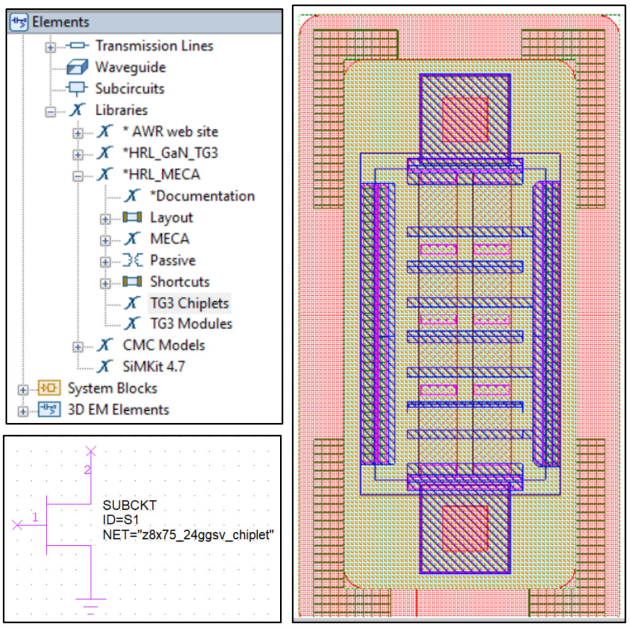


Fig. 6. Cadence AWR MWO MECAMIC transistor chiplet drag and drop from PDK palette to schematic with associated layout.

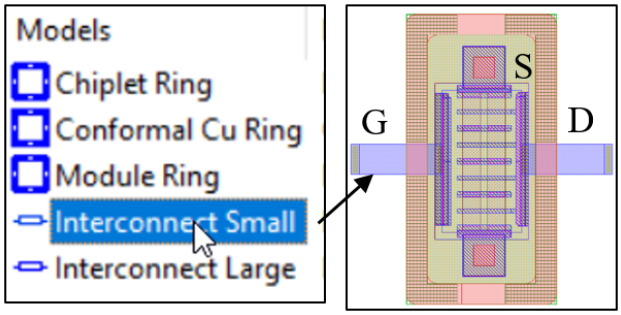


Fig. 7. Cadence AWR MWO MECAMIC transistor chiplet with added MECAMIC interconnects drag and drop from PDK palette to schematic with associated layout.

Using the MECAMIC PDK chiplet assembly library, circuit designers can use a traditional MMIC design workflow to construct and simulate heterogeneously-integrated circuits. Designers can build a schematic of their circuit with an associated layout and perform electrical simulations as shown in Figure 8. After initial electrical simulations, a designer can perform EM simulations using the MWO EM extract block to create EM structures from the elements in the schematic. The MECAMIC PDK provides a workflow that allows the extract blocks to extend to low levels in the hierarchy to accurately construct the needed EM structures. These EM structures are simulated, and the results are used to update the entire circuit performance.

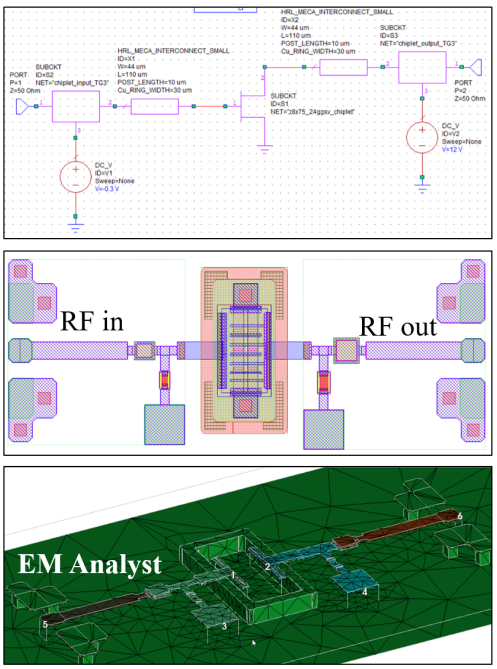


Fig. 8. Cadence AWR MWO MECAMIC transistor chiplet with added MECAMIC interconnects drag and drop from PDK palette to schematic with associated layout.

## MECAMIC Circuit Demonstration

S-parameter simulations and measurements of the single-stage circuit shown in Fig.5 were performed. The simulation used Microwave Office. Although higher gain was measured (6.5 dB vs. 5.5 dB for simulation), the measurements showed reasonable agreement with simulated values across the band of operation (70-80 GHz). This also compares well with the characteristics of a similar design in a T3 GaN MMIC process.

Further, a three-stage low-noise amplifier circuit was designed, simulated, fabricated and tested, and demonstrated a 4 dB noise figure at 77 GHz with a 16 dB gain. A microscope photograph, and S-parameter simluation and data are shown in Fig. 9 and Fig. 10, respectivley. The yield exceeded 66% across the wafer.

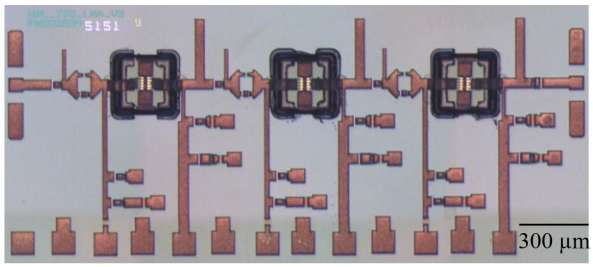


Fig. 9. Simulated and measured S-parameters of a heterogeneously-integrated single-stage RF MECAMIC circuit operating at W-band.

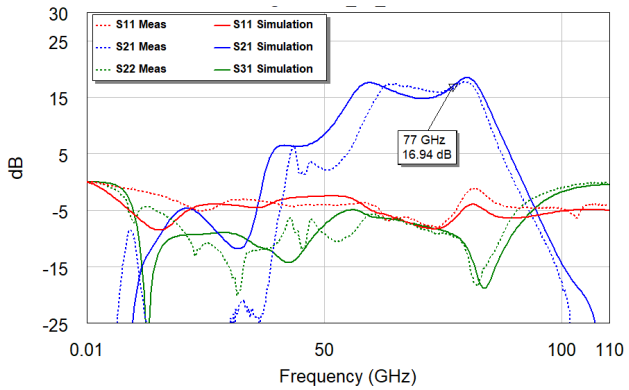


Fig. 10. Small-signal data of the 3-stage MECAMIC W-band LNA is in good agreement with simulated performance.

## Conclusions

Hybrid manufacturing techniques such as MECAMIC enable rapid prototyping and manufacturing of high-performance III-V integrated circuits for mm-wave applications.

## Acknowledgements

The author would like to thank the team members from the Sensors and Electronics Laboratory and the Microfabrication Technology Laboratory at HRL. The author would also like to thank the Microwave Office AWR team for the PDK development support.

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## References

[1] F. Herrault et al., "Metal-Embedded Chiplet Assembly for Microwave Integrated Circuits," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 10, no. 9, pp. 1579-1582, Sept. 2020.

[2] F. Herrault, et al., "Heterogeneously Integrated RF Circuits Using Highly Scaled off-the-Shelf GaN HEMT Chiplets," in IEEE Microwave and Wireless Components Letters, vol. 30, no. 11, pp. 1061-1064, Nov. 2020

[3] F. Herrault et al, "Heterogeneous Integration Technologies for Next-Generation RF and mm-Wave Subsystems," Cs Mantech 2018.

# Wafer-Level Packages for RF GaN Technologies & On-Wafer Humidity Test

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**Keywords: MMIC, CSP, WLP, HAST, GaN, THB, HPA, DUT, OWT**

**Abstract**

**Wafer-level chip-scale packaging is currently seen as a key technology affording a breakdown into integration of complex RF Front End with cost saving and performance enhancement.**

**Within this work, two chips scale packaging (CSP) concepts have been investigated in terms of manufacturability and process integration. In addition, a new Highly Accelerated Stress Test (HAST) configuration suited for on-wafer humidity testing has been designed to allow fast development cycles. A test vehicle circuit is used with a RF pre matched power transistor for the humidity tests.**

## Introduction

Two basic concepts are followed up for wafer level packaging (WLP). Concept A (Fig. 1) applies a BCB and a glass passivation. The MMIC is fully encapsulated by a BCB and a top glass layer.

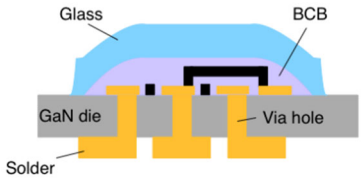


Fig. 1: Concept A – BCB & glass passivation

For the concept B (Fig. 2) an air-cavity package is realized using glass wafers having evaporated deposited glass walls that are joined to a GaN wafer by a bond process to achieve a hermetically closed chip-scale package. The electrical connection of the system is accomplished by a hot-via approach connecting signals and ground contacts from the backside of the wafer by through via-holes to the front side of the chip. An electroplated AuSn backside solder layer provides the interface to the system module. This approach suppresses the use of solder preforms.

The final hermitically sealed and small sized WLP MMIC product enables in both concepts the direct assembly on a PCB board without any additional packaging steps.

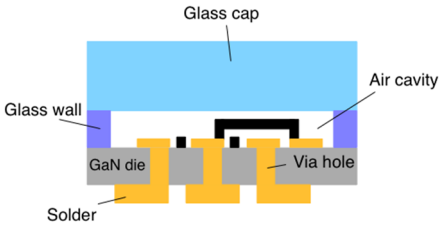


Fig. 2: Concept B – Hermetic air-cavity package

Both wafer level packaging approaches are based on the GH15 technology of UMS. This technology is a 150 nm gate GaN HEMT technology providing a power density of 4.0 W/mm for applications up to 35 GHz. Reference [1] shows additional information for both concepts.

Environmental reliability tests were carried out in order to show the evidence of a hermetical solution of concept A and B. The following paragraphs in this paper describes the test methodology and the results of humidity tests on WLP GaN test vehicles.

## Environmental Humidity Tests

In this work an environmental test methodology is presented applying a novel on-wafer humidity test system. It enables short development cycles in the Front End wafer manufacturing area by achieving fast feedback loops of reliability results. The evaluation of technological process concepts can be done already in the very first development phases. In addition, it saves time and costs for chip assembly processes in test packages for humidity tests. As such, also side effects from a classical chip packaging manufacturing spread are not present, which therefore allows a better interpretation of the humidity test results. Especially for wafer-level chip-size packages, the on-wafer reliability system can be used for process qualification for instance.

The wafer-level humidity tests are carried out in an HAST test system. The test system allows a temperature range

from 105°C to 143°C at a relative humidity range from 75% to 100% in unsaturated operation. In dry and wet operation, the system enables the operation from 50°C to 95°C and from 50% RH to 95% RH. These applicable test conditions enables THB as well as HAST tests as specified in common standards [2]. Up to 72 cable feedthroughs enable the connection to an electrical test system for voltage biased tests.

Fig. 3 shows the test fixtures and the wafer test cards for the wafer biasing inside the chamber. Three wafer test cards have been manufactured in order to enable parallel wafer testing. The wafer test cards moved into individual slots of the cassette. The cassette comes with three plug-in card holders, which are wired to the feedthrough connectors inside the chamber. This configuration consists of 54 cable feedthroughs applied for connecting 6 DUT's (devices under test) per wafer at gate, drain and source.

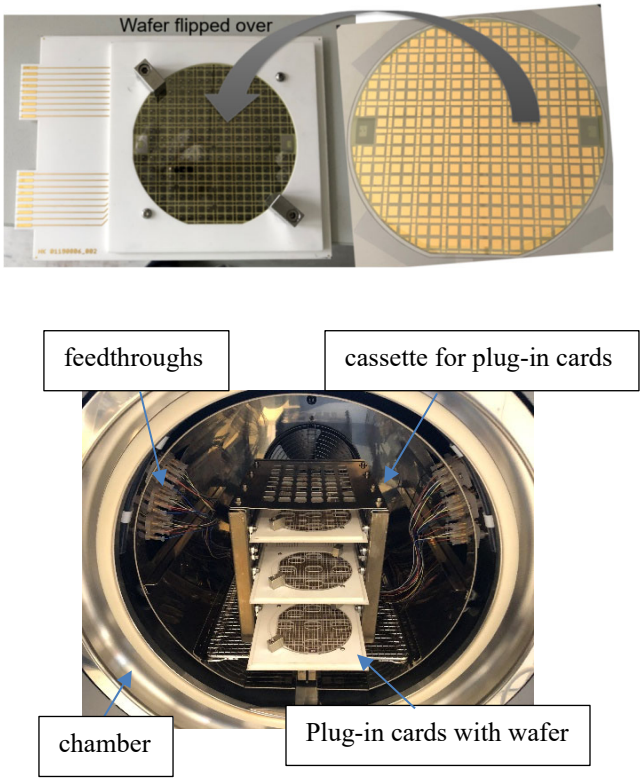


Fig. 3: On-wafer humidity test system setup

## Test Conditions and Procedure

The wafer backside metal is used for the interconnection of the test vehicles on the wafer. A 1-mm gate width pre-matched transistor circuit is used. This design integrates active and passive elements and RF pads in ground-signal-ground (GSG) configuration. Through wafer via-holes are connecting the front side pads to the backside metallization of the wafer. The biasing of the devices is performed by needle that connects the plug-in card to the backside metal of the wafer.

Fig. 4 (top) shows the front side of the test vehicle. The Fig. 4 (bottom) depicts the contact pins locations on the backside of the test vehicle with the gate, source, and drain interconnections.

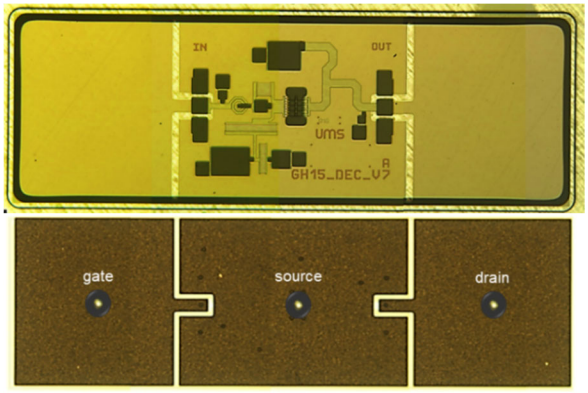


Fig. 4: Contact pin interconnection to test vehicle – test vehicle DEC (top); back side of test vehicle (bottom) & contact pin location from test card

After the wafer is mounted on the test card, a procedure is performed to manage a good electrical contact to each DUT's. In case of the GH15 technology the biasing conditions are Vg = -7 V for the gate voltage and Vd = +20V the drain voltage. As mentioned above, up to 18 DUT's can be biased and monitored on three wafers in parallel per test setup. Each DUT is biased separately before the test starts in order to identify any issue due to a poor electrical contact. After the contact test, a biased HTRB step is performed for 24 h at target temperature without humidity in order to sort electrical weak DUT's. Then all devices are again unbiased. After the humidity is switched on and the bias is applied again after the temperature and humidity reaches the target values. Test standards [2] specify HAST conditions with 130°C@85% RH associated to a criteria of 96 h test duration without any DUT failure. For THB conditions defined at 85°C@85% RH, the pass criteria is specified to get no failure within 1000h. Gate and drain currents are monitored by the electrical measurement system. In case of degradation of one device the electrical biasing stops at a current compliance of 2 mA. During THB test, interim visual inspections are done approximately every 300 h. In case of the HAST the test duration of >96 h will be performed without any interim inspection. Visual inspections of the DUT's are carried out before and after the test to identify any optical change for failed and passed devices.

## Test Results of WLP Processed Wafer

In both evaluated WLP concepts the devices are packaged utilizing glass as final protection. A hermetic package solution is one major objective of the project. The

humidity tests should illustrate the need and correct integration of the glass for sufficient protection.

**Concept A**– BCB & glass passivation

Two wafers of concept A were mounted into the test chamber. One wafer is fully processed with BCB and glass and the other one without glass passivation. The motivation of this test configuration was to reveal the improved humidity protection of the glass in addition to the BCB passivation. Fig. 5 shows the failure plot of DUT's versus time tested with BCB & glass versus BCB only passivation. THB and HAST tests applied with a test duration of 1000 h and 150 h, respectively. Failures shown in the graph correspond to electrical sudden breakdown of the device in all the cases hitting the compliance at 2 mA gate or drain current. The humidity degradation of the device leads to a short of drain or gate to source. In case of the concept A the additional glass layer reduces drastically the failure rate in time. Two sudden failures of DUT occurred after re-start of interim inspection at around 667 h for the BCB & glass layer.

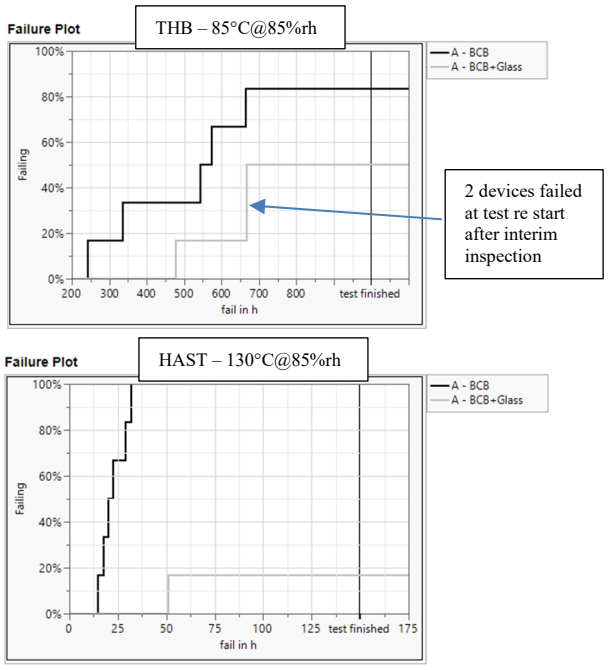


Fig. 5; Failure plot of THB (85°C@85% RH) in comparison of HAST (130°C@85% RH) of concept A

Optical inspection of all failed dies have shown one crack inside the glass and an electrical over stress (EOS) at the gate electrode (Fig. 6 a) for BCB & glass passivation. These failures are expected to have its root cause by uncontrolled change of glass layer stress and CTE mismatches of the passivation layers. Thermal cycling tests indicates a change of strain of the layers that lead to glass delamination. Consequently, the DUT reveals an electrical breakdown at the active device. In case of the BCB, the failed devices showed inside the active area a degradation of the semiconductor. This failure is identified typically as humidity related degradation in between the gate at -7V and drain area biased at +20V that result in a maximum applied voltage difference of 27 V. The mean failure rate of failed DUT's in case of the BCB passivated wafers for THB and HAST are in 471 h and 22.5 h, respectively. The degradation depicted in Fig. 6 b) occurs under HAST conditions 21 times faster compared to THB conditions.

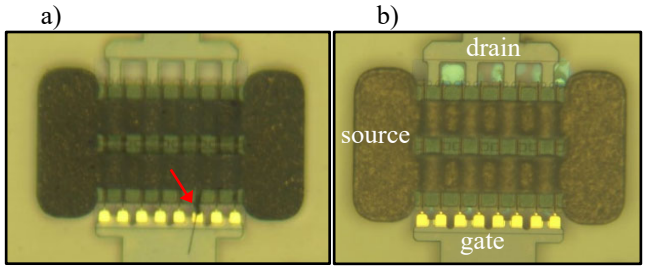


Fig. 6: Optical view of failed DUT's – a) BCB & glass (51 h) and b) BCB

Finally, the test shows a clear improvement of humidity protection by applying the glass passivation layer as expected. The reliability of the package A depends strongly on the mechanical strain control of the BCB and glass layer.

**Concept B** - Hermetic air cavity package

For concept B one wafer was tested in unbiased HAST conditions for 150 h. Unexpected process issues appeared due to layout reasons that made it impossible to finish the wafer at the backside process. The wafer was bonded to the glass cap wafer after completion of the front side process. Then the wafer was thinned down to a target thickness of 70 µm. The wafer manufacturing stopped after the grinding step. In order to investigate the humidity resistance of the air cavity package, the edge of the bonding interface had to be exposed first. A groove was sawed into the WLP wafer through the GaN on SiC Epi wafer up to the glass wafer allowing humidity penetration to the outer chip edges as shown in the SEM picture of Fig. 7 b).

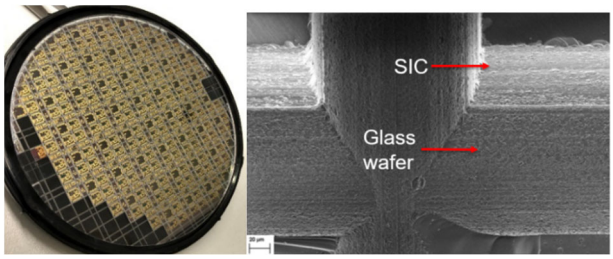


Fig. 7: a) WLP wafer after groove sawing – lower left part of wafer shows low bonding strength; b) tilt SEM view of groove with exposed bonding interface

The lower left part of the WLP wafer showed a small area with package yield loss after the sawing process. At this wafer area, a weak bonding interface could be identified as root cause (Fig. 7 a). After this preparation the WLP wafer was submitted to an unbiased HAST test for 150 h.

After 50 h and 100 h, an optical inspection was performed to evaluate any change or degradation of bonding interface by optical and mechanical characterization. Fig. 8 shows the top view of the test vehicle through the glass cap after 150 h unbiased HAST testing. No changes of the bond interfaces as well as no indications of humidity entrance into the air cavity have been detected by visual inspection.

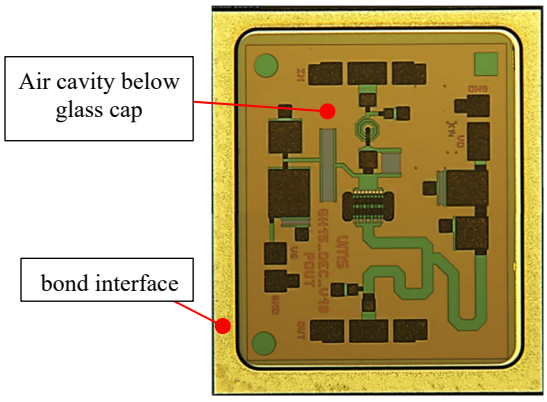


Fig. 8: top view of the test vehicle after 150h unbiased HAST exposure

Both wafer-level chip-scale packaging concepts had shown a clear step towards a hermetic packaging solution. The material glass supports this solution by its superior properties to stop moisture diffusion through the bulk.

## Development Cycle

The application of on-wafer reliability tests enables a first and fast feedback about the process integration at the FE wafer manufacturing. On-wafer tests (OWT) should allow to reveal unexpected failures and to confirm the effectiveness of the process integration approach applied. However, it is important to apply representative tests taking into account the requirements for the technology processes. These requirements usually derived from final product specifications. Applying correct pass/fail criteria for on-wafer tests are mandatory prerequisites to sort the right variants for final product qualification in the right manner. Fig. 9 illustrates the flow diagram of the development cycle and the role of the OWT.

The on-wafer humidity test system in this work enables after completion of wafer manufacturing an HAST test result within around 15 days. The test in oven lasts around 6 days, 2 days for data analysis and additional 7 days for physical failure analysis if required.

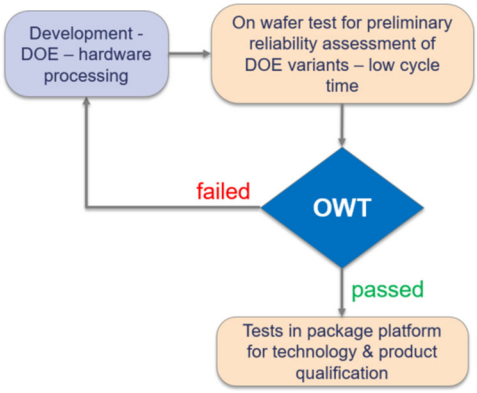


Fig. 9: Flow diagram for process development and testing

## Conclusion

This work summarizes the implementation of an on-wafer humidity test system with the capability of DC biasing of test circuits. Two different WLP concepts were tested in this new designed OWT system using THB and HAST conditions in the frame of this work. The fast feedback loop and the objectives of on-wafer tests as well its results are extensively discussed.

## Acknowledgements

This work was done within the project CoGaN, which was funded by the German federal ministry of education and research – BMBF (Funding number: 16ES0684K).

## References

[1] H. Stieglauer, et al., *Wafer-Level Packaging for Electronic RF Systems Using GaN Technologies*, 2020 GaAs MANTECH

[2] JEDEC PUBLICATION, JEP001-3A, (Revision of JEP001A, February 2014)

## Acronyms

CSP: Chip Scale Packaging
DUT: Device under Test
WLP: Wafer Level Packaging
CoGaN: Covered Galium Nitrid
THB: Temperature Humidity Bias
HAST: Highly Accelerated Stress Test
HTRB: High Temperature Reverse Bias
OWT: On Wafer Test

# Wafer Breakage Reduction in Cu Bump Processing of GaAs Technologies

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**Abstract**

**Efforts to reduce wafer breakage events during Cu bump manufacturing of GaAs technologies were discussed in this paper. Wafer backside residue and scratches formed during upstream processes were found to cause stress breaks at the Cu plating step. A correlation of wafer edge chipping at the lamination process and downstream finish processes was discovered. The fishbone diagram was used to investigate frequent wafer stress breaks at Cu field metal etch process. As a result, the overall wafer breakage rate was reduced by more than 50% in Cu bump processing.**

## INTRODUCTION

GaAs devices have been widely used in RF applications and the GaAs manufacturing wafer yield has been significantly improved over the last two decades [1-4]. One of the challenges with GaAs fabrication is high wafer breakage rate due to its brittleness. Many research studies have shown that the GaAs wafer breakage rate was reduced from up to 25% during the initial development to less than 0.5% in high volume manufacturing through equipment modification and process improvement [1-4]. With the increasing requirement of cost effectiveness, the goal of wafer yield of GaAs manufacturing has been continuously raised. At Qorvo, wafer breakage is the second largest contributor to wafer yield loss of GaAs technologies.

To understand the causes of high wafer breakage rate, the broken wafer scrap data was analyzed by process steps. Figure 1 shows the GaAs wafer breakage events at different manufacturing process steps. The data indicated baseline level wafer breakage across front-end-of-line processes, but wafer breakage occurred more often during Cu bump and fab finish process steps. Since wafers are more valuable at the backend of the process, this study is focused on reducing wafer breakage rate during Cu bump processing.

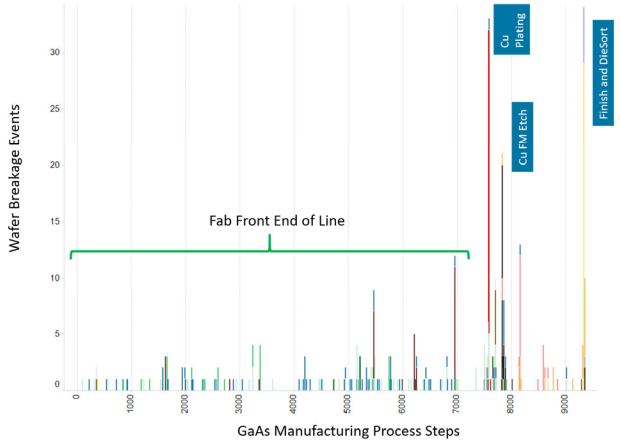


**Figure 1. Wafer breakage scraps at different process steps during GaAs manufacturing**

## RESULTS AND DISCUSSION

### Stress Breaks at Cu Bump Plating Step

As shown in Figure 1, the first high wafer breakage rate step in Cu bump fabrication is the Cu bump plating step. Wafers were normally found broken during handling into/out from the plating equipment. The frequent wafer breakage events have not only caused wafer yield issues, but also reduced the equipment availability, therefore impacting manufacturing cycle time. Adjusting tool parameters including robot handling and vacuum levels were attempted and reduced the wafer breakage rate.

However, frequent wafer breakage was still observed.

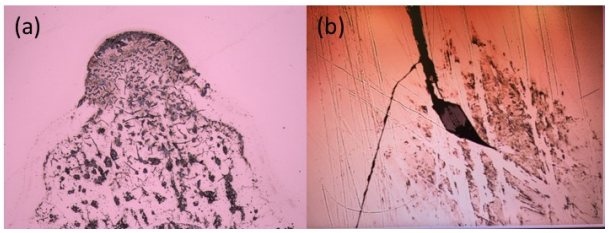


**Figure 2. (a) Residues present on the backside of the wafer incoming to Cu bump plating step (b) Microcrack observed after removing the residue**

Further investigation of the broken wafers indicated residues on the backside of the wafers makes the wafers more susceptible to breakage during Cu bump plating handling. The residue was normally found at the center of the wafer and could cause vacuum issues. The wafers may drop during handling or become misaligned inside of the tool. For the wafers that cannot be picked up by the tool and are still intact, manual scraping is required to remove the residue. However, microcracks will be introduced during manual residue removal and will lead to stress breaks later as shown in Figure 2(b).

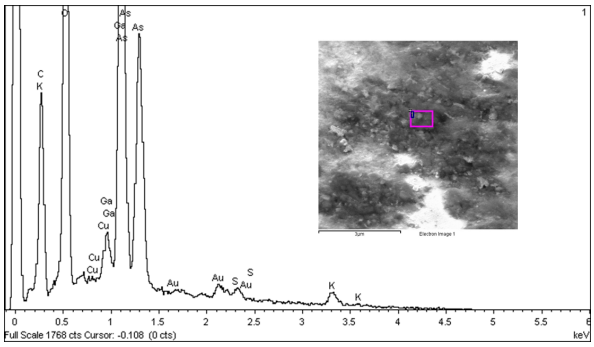


**Figure 3. EDS analysis of wafer backside residue incoming to Cu bump plating process**

EDS analysis of the wafer backside residue revealed the presence of K and Au elements. This indicated the residue was formed during an upstream sink process. Inline inspection was performed and confirmed the root cause of residue formation.

A combination of efforts to reduce wafer backside residue at upstream process steps and the subsequent residue removal process on the incoming wafers have reduced the wafer breakage rate at Cu bump plating step by > 70%.

## Investigation of Wafer Stress Breakage at Cu Field Metal Etch Process

The second highest wafer breakage step during Cu bump fabrication is the field metal etch process. The broken wafers were found to have a specific stress break pattern. When the stress break was found, the broken wafers were always sitting in the cassette broken into two pieces with the breakage plane facing the top of the cassette. The wafers were not typically aligned at the field metal etch process, but the broken wafers were always the ones with 8 o'clock or 2 o'clock at the top of the cassette, as shown in Figure 4.

**Figure 4. Pictures of broken wafers found at field metal etch process. Signature of 8 to 2 o'clock stress break with breaking plane always facing the top of the cassette.**

This unique breakage pattern indicated two potential failure modes. One hypothesis is that there was excessive force applied to the wafer edge that caused stress break when the force was applied to 8 or 2 o'clock. This failure mode pointed to the slide transfer used at Cu field metal etch process. Multiple wafer transfers between PEEK and teflon cassettess are required during preclean and field metal etch processes. The wafer transfers are performed using a manual slide transfer. It was found that the handle of the slide transfer arm drifted down. If the handle was not lifted properly, there will be an angle between the pusher and wafers therefore cauing extra force

on the wafers. If the slide transfer was touching at the crystal plane of the GaAs wafers, the wafers were likely to break along the plane.

After replacing the slide transfer for Cu bump processing and refreshing slide transfer training, the wafer breakage rate was reduced at Cu field metal etch process. However, frequent breakage events still remained.

The other failure mode that could explain the 8 or 2 o'clock breakage was damage from a previous step that only broke after the slide transfer motion. The backend engineering team did a Fishbone analysis to identify possible steps/processes that could cause micro damage on the wafer, as shown in Figure 5.

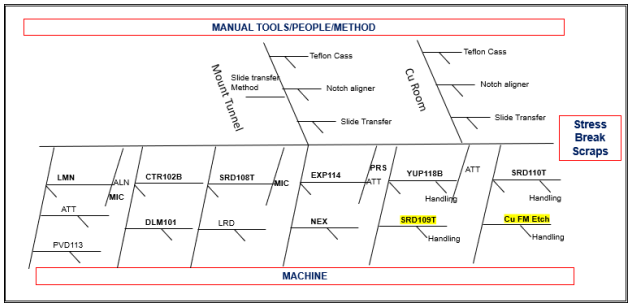


**Figure 5. Fishbone diagram to troubleshoot root cause of stress break at field metal etch process.**

During an extensive equipment handling check, it was found that a tool cover was slightly touching the wafer edge when the robot was moving the wafer into the tool as shown in Figure 6. The wafer did not break at this step and no obvious damage was observed, but if the wafer was rotated so that the 8 or 2 o'clock crystal plane touched the tool cover, the wafers were more likely to break during a later slide transfer process step. The tool cover was then modified to have more clearance during the wafer handling. With these combined improvements, the wafer breakage rate was significantly reduced at the field metal etch process.

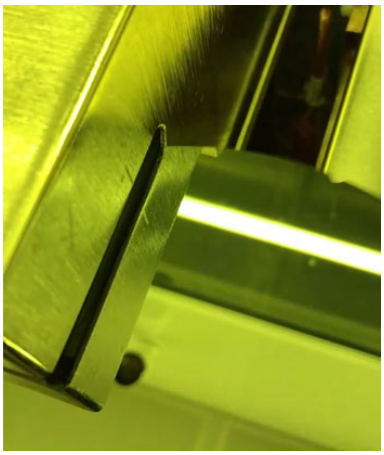

**Figure 6. A tool cover was found touching the wafer edge when the wafer is moving into the tool.**

## Correlation of Edge Chipping and Wafer Stress Breaks at Subsequent Finish Processes

After Cu bump processing, wafers are sorted and then go to the finish process. It was found that some wafers were broken during the sort or finish processes without apparent root causes. The equipment in sort and finish areas were checked but no cause of the breakage was identified.

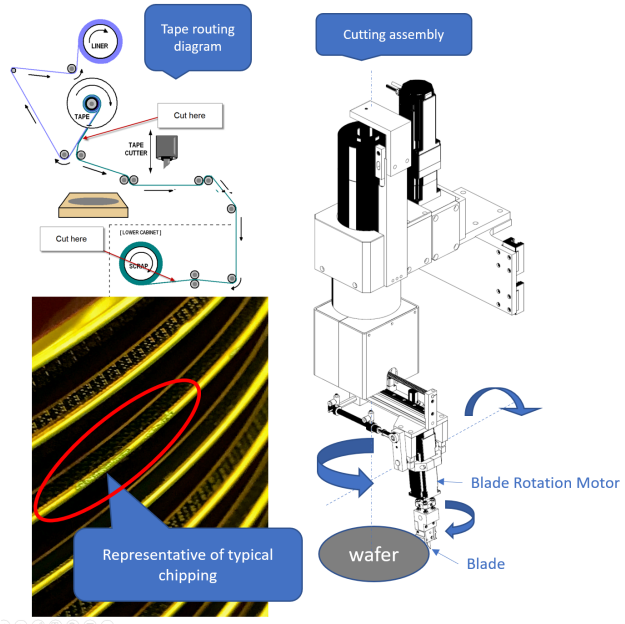


**Figure 7. Wafer edge chipping formed during lamination cutting step. Equipment schematics is from Microcontrol Electronic.**

During an investigation of multiple lots having wafer breaks, it was found that the broken wafers were from the same parent lot in the upstream process. A closer look at the broken wafers revealed commonality of wafer edge defects that contribute to the origination of the wafer breakage. The wafer edge was covered with metals, so the defects were hard to detect. Inline inspection was implemented at upstream processes to identify the source of wafer edge defects.

Upstream inline inspection showed that intermittent wafer edge chipping was observed after the lamination process, from particular lamination equipment. Minor edge chipping/scraping was found after the cutting step. The cutting blade also showed abnormal wear prior to a scheduled PM, validating the failure mode.

Tool matching work including cutting angle adjustment and PID setting optimization to reduce vibration of the cutting process was performed reducing wafer edge chipping at this step and wafer breakage in the sort and finish areas.

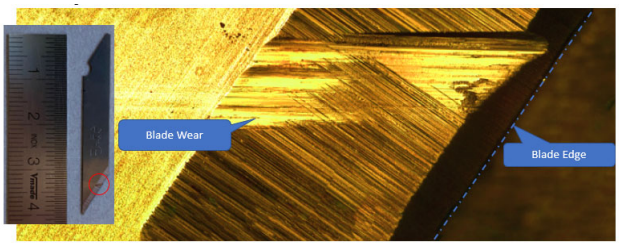


**Figure 8. Wearing of the cutting blade indicated vibration causing wafer edge chipping.**

## CONCLUSION

In this paper, we discussed three wafer breakage reduction improvement projects in Cu bump process. With the implemented preventative actions, the wafer breakage rate of Cu bump fabrication has been reduced by more than 50%, and a new baseline with a lower wafer breakage rate was achieved, as shown in Figure 9.

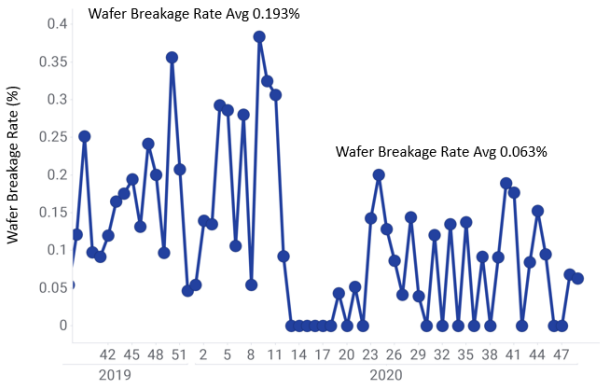


**Figure 9. Wafer breakage rate of Cu bump process by work week. New low wafer breakage baseline was achieved after the improvement project.**

## REFERENCES:


1. T. Gordner, B. Marks, *GaAs Wafer Breakage: Causes and Cures, Growth and Process*, GaAs IC Symposium 1993, 317-320.
2. T. Hsiao, G. Chen, S Chou, H. Liao, Manufacturing of Cu-pillar Bump for III-V MMIC Thermal Management, 2012, CS MANTECH Conference.
3. B. Darley, M. Singh, P. Santos, E. Ambrocio and S. Tiku, *GaAs Wafer Breakage Reduction,* 2014, CS MANTECH Conference.
4. M. Schaper, M. Jurisch, F. Bergner, R. Hammer, *Fracture Mechanical Evaluation of GaAs Wafers,* Mat. Res. Sco. Symp. Proc. Vol. 744, 2003, Materials Research Society.


## ACKNOWLEDGEMENTS


The authors would like to thank Fab process and maintenance technicians for all the data collection, inline inspection, and equipment modification/adjustments.

# Seeing the World from a Drop of Water: A Novel Environment-Protecting Technique for Photoresist Strip, Metal Lift-off, and Etching Byproduct Removal

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**Keywords: Water, Moisturization, Byproduct removal, Photoresist strip.**

## Abstract

**Post etch residue and photoresist cleaning typically use several specialty solvents and multiple processing steps leading to clean the substrate. In this paper we present a novel and environment-protecting technique for photoresist and post etch residue strip process which uses DI water as main strip agent in semiconductor mass-production. This technique reduces harsh chemical and solvent usage and has remarkable performance on photoresist strip, metal lift-off, and removal of post etching byproducts. WIN Semiconductors Corp. is the first to implement this eco-friendly process into mass-production in the world. This new process establishes excellent corporate social responsibility to WINs workforce, customers, and environment.**

## INTRODUCTION

Photoresist cleaning and stripping is widely used in the semiconductor manufacturing industry. It needs solvent combined with reactive agents, such as NMP, DuPont™ EKC922™, acetone, IPA, etc., which are hazardous to the environment and the human body. Byproducts of plasma dry-etch is hard to remove. In this paper, we present a novel and eco-friendly technique to use DI water as the primary cleaning agent with showing remarkable performance on removal of photoresist and post etch residue, and also for metal lift-off processes.

The typical process that we use in manufacturing is to immerse batch-type wafers into NMP or DuPont™ EKC922™, and follow this with a single wafer spray with acetone and IPA to clean wafer. In the new process we immerse the batch of wafers in NMP as the first chemical treatment, then spray moisturized DI water to clean wafer. By reducing the use of the immersion bath, this is a more environmental protecting because most usage and waste of process is water, not chemical and solvent. We developed the moisturization procedure to nebulize DI water into very small droplet size, which looks like fog but with sprayed pressure. The novel process is much friendly to environment and human body. We have also found that the process tool is easier to maintain with less working hours.

## HYPOTHESIS

There are three steps in the novel process to complete this strip technique, showed in Figure 1. In step 1, an immersion bath is used for a batch of wafers into NMP to do chemical treatment first, to swell the polymer such as photoresist or byproducts of plasma dry-etch. In step 2, we spray moisturized DI water to penetrate into the swelled polymer. The water will penetrate into and accumulate at the interface between polymer and substrate structure to become the water film. When the water film is in saturation, polymer would separate from substrate structure by surface tension of water and the lift-off happens, and this is step 3. [1][2][3].

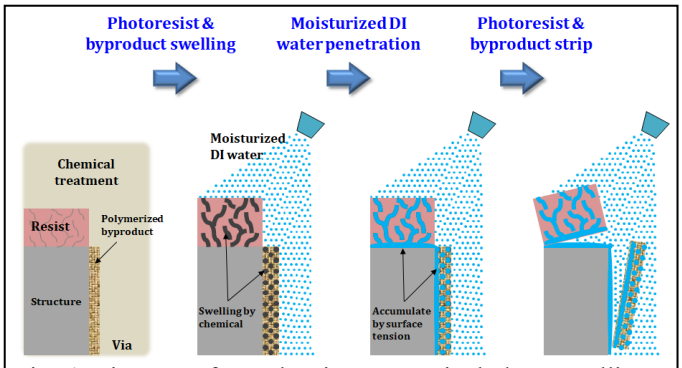


Fig. 1 Diagram of novel strip process includes "Swelling", "Penetration", and "Lift-off".

There is the counterevidence to verify the hypothesis. Figure 2 shows polymer residue remaining, which is worse case. If there is no swelling step before spraying moisturized DI water, the "Penetration" is low efficiency and hard to form water film for "Lift-off". If the moisturization is worse, the water film formation will be low efficiency. They are bad for this novel process and would cause residue remaining after moisturized spray-strip.

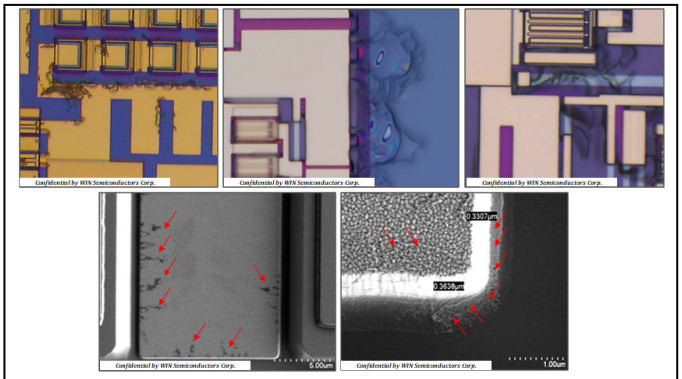

Fig. 2 Remained residue is caused by non-swelling or worse moisturizing.

## REMARKABLE PERFORMANCE

Considering the impact to the environment and the human body, we summarize and normalize the usage for two mass-production processes, typical one and novel one. Figure 3 shows total usage for chemical and solvent, which is normalized to one wafer. There is almost 10 L of chemical and solvent used since from first process layer to the end process layer in cleaning tool, normalized to every wafer which is an average value. Compare with typical process, it is a benefit to reduce total 90.7% usage for each wafer in novel process. We also note that using DI water as main strip agent is easier to maintain equipment. The typical process takes 1.1% working hours per year in tool maintenance, but the novel process only needs 0.49% working hours per year which is 55% reduction.

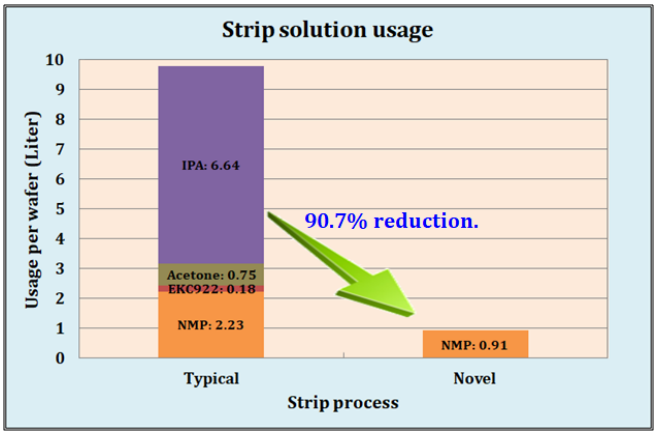


Fig. 3 The novel process can reduce about 90.7% usage than typical process, normalized to each wafer.

For byproducts removal of plasma dry-etch on polyimide structure, there is a very excellent result with novel process. Typical process has very thick and polymerized byproducts remaining on sidewall and it becomes a fence and then peels down making it unable to be effectively removed in Figure 4 (a). This is a wafer defect and would cause reliability and electrical fail. Figure 4 (b) shows novel process has excellent result to remove polymerized byproducts on same structure. To swell byproducts first and spray moisturized DI wafer to penetrate into to form water film at the interface between polyimide structure and polymerized byproducts. Then complete "Lift-off" by water surface tension. This great result also proves our hypothesis is correct.

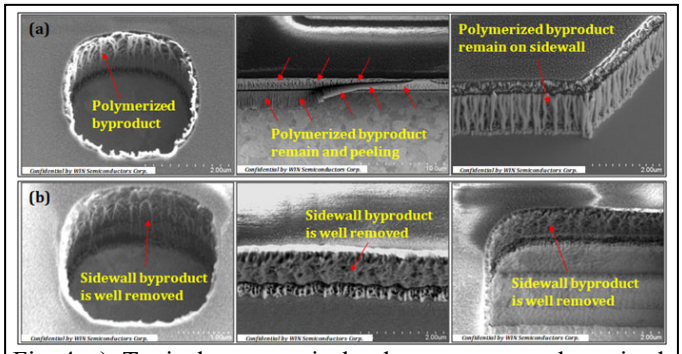


Fig. 4 a) Typical process is hard to remove polymerized byproducts after plasma dry-etch on polyimide via and structure; b) Novel process can easily remove same byproducts and the wafer is well-cleaned.

Through-wafer-via etching is a commonly used process. The byproducts after plasma dry-etch is hard to remove in deep via and becomes a side effect to interconnection. In Figure 5 (a), there is thick and polymerized byproducts adhere to sidewall of deep via and unable to be removed by typical process. It is very serious at the bottom of deep via and easy to remain and peel to induce reliability and electrical fail. When WIN implemented the novel process to same via structure and the result is perfect which is in Figure 5 (b). The byproducts no matter on via sidewall or at bottom of via is all well-cleaned. Of course, the quality of photoresist removal after plasma dry-etch is same as typical process for sure.

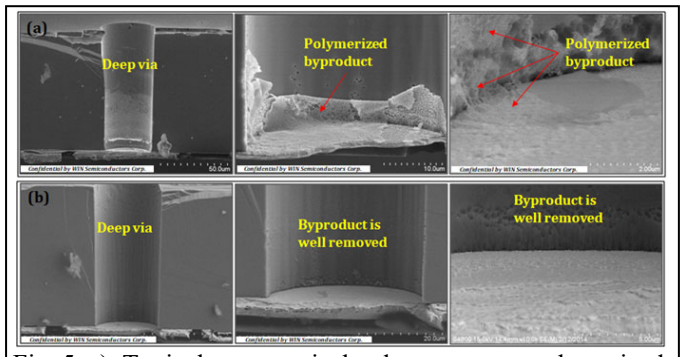


Fig. 5 a) Typical process is hard to remove polymerized byproducts after through-wafer-via plasma dry-etch; b) Novel process can remove same byproducts, no matter on via sidewall or at bottom of deep via.

There is one more benefit contributed by novel process. Figure 6 (a) is the result of typical process on photoresist

strip and metal lift-off. There are silk remains and unable to be cleaned well after re-work. Novel process can avoid this defect happens on same structure, showed in Figure 6 (b).

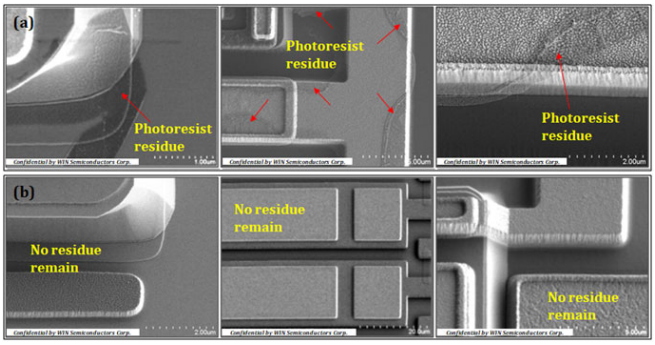


Fig. 6 a) Typical process has silks remain and unable to be cleaned after re-work; b) Novel process can avoid silks defect happens on same structure.

## CONCLUSIONS

WIN Semiconductors Corp. is the first to implement novel and environment-protecting strip process which uses DI water as main strip agent to mass-production in the world. This process establishes excellent corporate social responsibility to WINs workforce, customers, and environment. It achieves remarkable performance to remove byproducts and photoresist, and also reduces chemical and solvent usage.

## REFERENCES

[1] Song, Jae-Inh, et al. "*Using an ozonated-DI-water technology for photoresist removal*", Micro Magazine (2001).

[2] Rudolph, Matthias, et al. "*Introduction of an innovative water-based photoresist stripping process using intelligent fluids*", Advances in Patterning Materials and Processes XXXI., Vol. 9051, International Society for Optics and Photonics (2014).

[3] Rudolph, Matthias, et al. "*Evaluation of water based intelligent fluids for resist stripping in single wafer cleaning tools*", Advances in Patterning Materials and Processes XXXIII., Vol. 9779, International Society for Optics and Photonics (2016).

## ACRONYMS

DI water: De-ionized water.
EKC922™: DuPont's universal photoresist remover.
IPA: Isopropyl alcohol.
NMP: N-Methyl-2-pyrrolidone.

# LOL 1000 Liftoff Resist as an Antireflective Coating for MMIC Electroplating

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**Keywords: Electroplating, Air Bridge, GaN, SiC, Antireflective coating, MMIC**

**Abstract**

**This work demonstrates the use of Liftoff Layer (LOL) 1000 as an antireflective coating (ARC®) that reduces process variability and increases device yield. Using LOL 1000 resist as an ARC® layer, we have yielded 6 µm pads 7 µm apart. Replacing a standard ARC® eliminated an dry etch from the monolithic microwave integrated circuit (MMIC) air bridge process as well as reduced critical error-prone process steps leading to wafer-scale fabrication failure.**

## INTRODUCTION

Thick gold electroplating is an essential step in the fabrication of compound semiconductor devices due to the high current densities offered by the GaN high electron mobility transistor (HEMT) material system [1]. The process enables air bridges for multi-fingered devices. Air bridges are commonly found in compound semiconductor manufacturing, but are one of the more difficult processes in monolithic microwave integrated circuit (MMIC) fabrication due to several irreversible processing steps. An ARC® serves to reduce reflections from topography which can interfere with processing.

An antireflective coating (ARC®) is necessary in air bridge fabrication to reduce the lithography illumination reflecting off the sputtered gold seed layer and exposing the underside of the AZ® 15nXT resist. This leads to exposed AZ® 15nXT which blocks plating in that area. This compels us to use an ARC®. This paper explores the fabrication of air bridges without an ARC® and with the use of two separate ARCs®, XHRiC-16 and LOL 1000.

## METHODS

Air bridges are fabricated as follows: 1) interconnect metal is evaporated, 2) a sacrificial 2.2 µm polymethylglutarimide (PMGI) (Kayakli Advanced Materials) *post* layer is patterned which defines contact to the bottom interconnect layer; 3) a sputtered Au layer of thickness 1500 Å is deposited which is used to seed electroplating; 4) an ARC® is used to reduce light scattering during the following *bridge* lithography step which defines the air bridges; 5) AZ® 15nXT negative photoresist is used to pattern *bridge;*.6) thick gold is electroplated to define the post and bridge structures.

## DISCUSSION

Electroplating is the primary method of air bridge fabrication. This method is more cost-effective than sputtering or evaporating thick gold. AZ® 15 nXT (AZ Electronic Materials) is a thick negative resist generally used for defining bridge lithography for electroplating. Since there is a gold seed layer under the AZ® 15 nXT, the i-line exposure reflects off the seed layer, thus exposing the underside of the AZ® 15 nXT, as demonstrated in Figure 1 a) and Figure 1 b). This inadvertently exposed resist will not develop away and prevents plating on the gold metal pads.

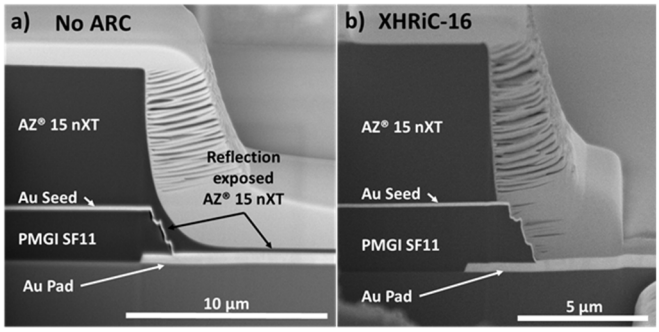


Figure 1 a) Cross-section of reflection exposed AZ® 15 nXT resist layer undeveloped on gold pads and b) cross-section of a straight sidewall profile using XHRiC-16.

XHRiC-16, manufactured by Brewer Sciences, was evaluated first. XHRiC-16 is able to absorb the reflected i-line exposure, so the underside of the AZ® 15 nXT remained un-exposed, as shown in Figure 1 b). XHRiC-16 requires a dry etch and is not affected during the AZ® 15 nXT develop

process with AZ® 300 Metal Ion Free (MIF) (EMD Performance Materials). After wet-developing AZ® 15 nXT, the XHRiC-16 is removed with an $O_2$ reactive ion etch (RIE) which causes the gold seed layer to sputter onto the sidewalls of the AZ® 15 nXT as seen in Figure 2 a) and Figure 2 b).

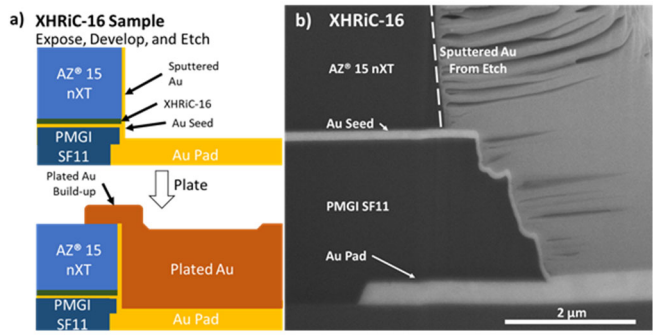


Figure 2 a) Schematic cross-section and process for plating a sample using XHRiC-16 and b) cross-section of sputtered gold along the sidewall after etching XHRiC-16.

The sputtered seed causes a conduction pathway during electroplating, which produces gold plating build-up on the edges of the structures. This plating build-up can cause tight geometries to become shorted to one another, demonstrated in Figure 3.

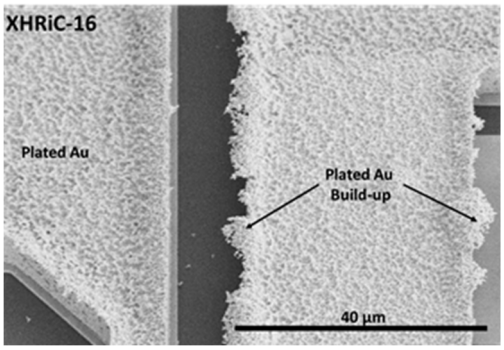


Figure 3 Top-down SEM of plated gold build-up from sidewall sputtered gold after etching XHRiC-16 as an ARC®.

After plating, the XHRiC-16 must be dry-etched again to expose interconnect metal for device testing. Ideally, ARC® can wet-develop concurrently with the AZ® 15 nXT process.

LOL 1000 (Dow), a liftoff resist, is also evaluated as an ARC®. During lithography, it absorbs reflected i-line illumination, which protects the underside of the AZ® 15 nXT from exposure, as seen in Figure 4 a). LOL 1000 is wet-developed concurrently with AZ® 15 nXT using AZ® 300MIF developer. This eliminates the dry etch requirement and prevents gold seed sputtering onto the AZ® 15 nXT sidewalls. The combination of LOL1000 and AZ® 15 nXT results in the best electroplating process for air bridges, as shown in Figure 4 b). LOL1000 has yielded tight geometries, such as 7 µm between 6 µm of plated gold on pads.

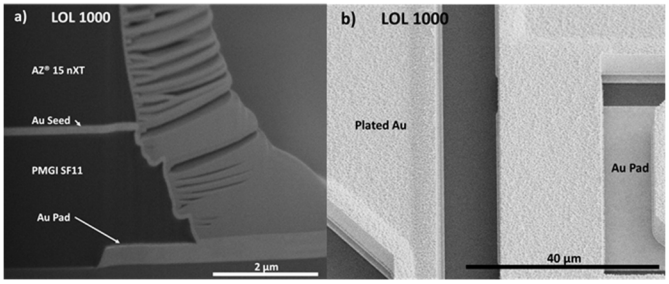


Figure 4 a) Cross-section of a clean AZ® 15 nXT sidewall profile after developing LOL 1000 and b) top-down SEM of clean plated gold after using LOL 1000 as an ARC®.

## CONCLUSION

Using LOL 1000 resist as an ARC® layer, we have yielded tight geometries of 7 µm between 6 µm of plated gold on pads. Using this process, we have eliminated an RIE etch from the MMIC air bridge process as well as reduced critical error-prone process steps leading to wafer-scale fabrication failure.

## ACKNOWLEDGEMENTS

The authors would like to thank Joseph Breedlove, Jason Hickey, and Andrew Browning for maintaining and running the Air Force Research Laboratory Cleanroom.

## REFERENCES

[1] RC Fitch, et al., *Implementation of High-Power-Density X-Band AlGaN/GaN High Electron Mobility Transistors in a Millimeter-Wave Monolithic Microwave Integrated Circuit Process*, 2015 IEEE Electron Device Letters, Vol. 36, No. 10, pp 1004-1007, October 2015.

## ACRONYMS

ARC®: Antireflective coating
HEMT: High electron mobility transistor
LOL: Liftoff layer
MIF: Metal ion free
MMIC: Monolithic microwave integrated circuit
PMGI: Polymethylglutarimide
RIE: Reactive ion etch

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# Theoretical study of recoil-implanted N atoms in Mg-implanted GaN

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**Keywords: GaN, ion implantation, Magnesium (Mg), stoichiometry, Boltzmann transport equation**

**Abstract**

**We calculated the depth distribution of implanted primary Mg ions and recoiled Ga and N atoms in a semiconductor by using a Boltzmann transport approach. It was found that the stoichiometric disturbance by Mg implantation was most significant for GaN, as compared to that for GaP, GaAs and GaSb. The peak density ratio (PDR), defined as the peak density of recoil-displaced group V atom with respect to that of group III atom, reached as high as 2.6 for GaN. Our calculation also proved that the PDR was rather insensitive to the changes in the implanted ion energy and the atom density in the target material. These results reveal that electrical activation of implanted Mg acceptors in GaN is more complicated and difficult than that in other semiconductors.**

## Introduction

Ion implantation is recognized as a precise and high-yield doping technique. Thanks to its capability of selective-area doping, planar semiconductor structures can be prepared with well-defined lateral controllability for both p-type and n-type conductivities. In fact, it is widely used for the fabrication of various Si and SiC devices. Vertical GaN-based MOSFETs are attracting increased attention as low-loss and high-voltage power switching devices [1-3]. Magnesium (Mg) ion implantation into GaN is now extensively studied to make p-type channel layers as well as to achieve high-density p-type contact layers [4-10]. Optical characterization indicated formation of acceptor centers after thermal annealing of Mg-implanted GaN [4, 5]. However, except recent results using ultra-high-pressure annealing [6,7], only partial electrical activation has been reported on Mg-implanted GaN layers by using conventional activation annealing methods [8-10 oikawa2015, niwa2017, tanaka2019]. Contrary to the case for element semiconductors such as Si, it is predicted that ion implantation into GaN induces local stoichiometry imbalance in addition to generation of various point defects. Such additional difficulties might result in insufficient electrical activation of Mg acceptors implanted into GaN.

Christel and Gibbons proposed an efficient algorithm to calculate the momentum distributions of moving atoms in the material by using Boltzmann transport equation [11,12]. In this method, distribution functions of moving atoms, including both primary and recoil-implanted atoms, are numerically solved with respect to the depth from the semiconductor surface, thus enabling the calculation of redistributed atoms in the target material. In this way, one can calculate in-depth local imbalance of stoichiometry after ion implantation.

In this work, we have applied this approach to Mg-implanted GaN and calculated the momentum distributions of recoil-implanted Ga and N atoms. As a result, it was found that the implantation-induced stoichiometry disturbance became most significant in GaN, as compared to that induced in other III-V compound semiconductors. Possible mechanisms for the stoichiometry imbalance are discussed.

## Calculation Procedure

Following the approach proposed by Christel and Gibbons [11,12], momentum distributions of moving atoms, including primary and recoil-implanted atoms were calculated stepwise as a function of the depth $z$ based on the Boltzmann transport equation:

$$\frac{\partial F(\boldsymbol{p})}{\partial z} = N \int \left( \frac{F(\boldsymbol{p}\prime) d\sigma(\boldsymbol{p}\prime \rightarrow \boldsymbol{p})}{\cos\theta_{\boldsymbol{p}\prime}} - \frac{F(\boldsymbol{p}) d\sigma(\boldsymbol{p} \rightarrow \boldsymbol{p}\prime)}{\cos\theta_{\boldsymbol{p}}} \right) + Q(\boldsymbol{p})$$

Here, $F(\boldsymbol{p})$ denotes the momentum distribution function of atoms with momentum $\boldsymbol{p}$, and $d\sigma$ is the scattering cross section. In our calculation, momentum $\boldsymbol{p}$ was represented by the kinetic energy $E$ of the atom and the angle $\theta$ of its moving direction with respect to the target surface normal direction. $Q(\boldsymbol{p})$ is the generation term, corresponding to the distribution of recoil atoms created from rest. The target material was assumed amorphous. The depth dependent distribution function of each atom is schematically illustrated in Fig. 1.

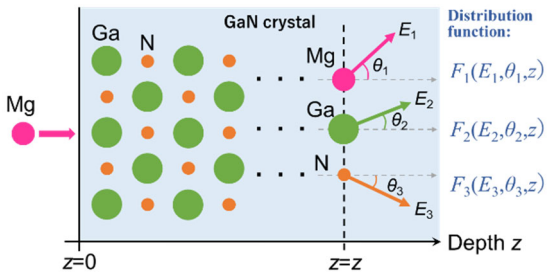


Fig. 1 Illustration of distribution functions of atoms.

Nuclear collisions (elastic) and electronic stopping process (inelastic) were considered as two independent scattering mechanisms. The elastic nuclear event was assumed as classical two-body mechanics, in which angular deflections of both incident and recoil atoms occurred with energy transfer between those atoms. Thus, only nuclear events generated recoil atoms. For the elastic nuclear cross section, we adopted the hybrid formula proposed by Christel and Gibbons [11,12].

Each atom was assumed stopped when its kinetic energy was reduced to nearly zero ($E < E_S$) or when it was directed toward the semiconductor surface. The range distributions of both primary and recoil particles were thus determined at each depth.

## RESULTS

Figure 2 shows the concentrations of vacancies and displaced atoms of Ga and N as a function of the depth, together with the implanted Mg atom profile (220 keV, $10^{15}$ $cm^{-2}$). Open squares and triangles indicate a net vacancy concentration, while closed squares and triangles indicate a net displaced atom concentration. Note that a high density of vacancies (Ga and N) is introduced in the shallow region, while recoil atoms are accumulated in the deeper region. The projected range was defined as the depth of the peak concentration for the implanted Mg. This projected range is 0.21μm by our calculations, although SRIM software calculations suggest a slightly larger range of 0.26 μm. By comparing the effect of recoil implantation for Ga and N atoms, the N atoms have a much larger concentration in both profiles of vacancy and displaced atoms. When the peak density ratio (PDR) is defined as the peak density of displaced N divided by that of displaced Ga, it reaches as high as 2.6. Considering that implanted Mg should occupy Ga sites as acceptors, the formation of much higher density of N vacancies in the shallow region (less than 0.15 μm) is not beneficial for achieving increased electrical activation by Mg implantation into GaN.

Figures 3 and 4 show the concentrations of vacancies and displaced atoms as a function of the depth, together with the implanted Mg atom profile (220 keV, $10^{15}$ $cm^{-2}$) in GaAs and GaSb. For GaAs, there is not a large concentration difference between Ga and As atoms. For GaSb, the concentration of Sb appears to be lower than the profile of Ga. When the PDR is similarly calculated as the peak density of displaced group V atoms (As and Sb) divided by that of displaced Ga, it reaches 1.0 and 0.7.

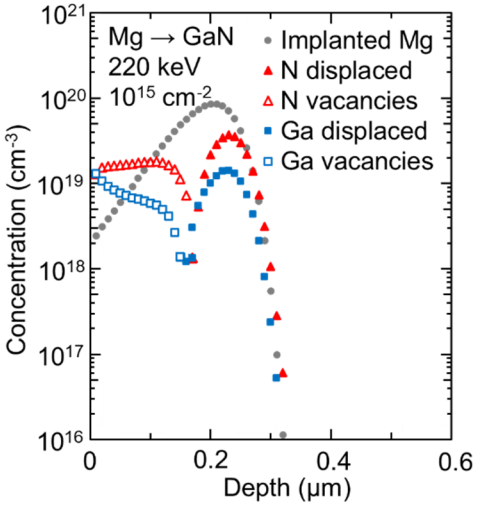


Fig. 2. Stoichiometric distribution in GaN implanted with 220 keV Mg.

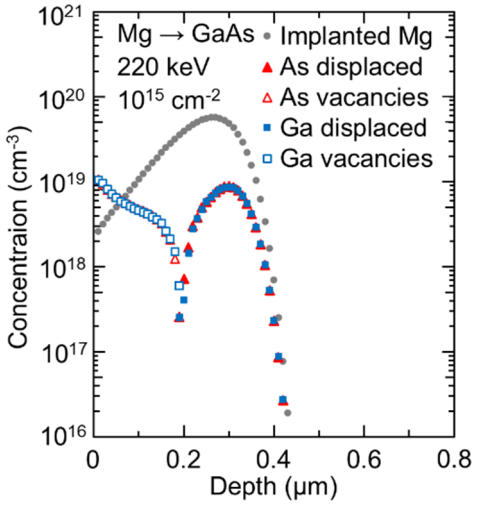


Fig. 3. Stoichiometric distribution in GaAs implanted with 220 keV Mg.

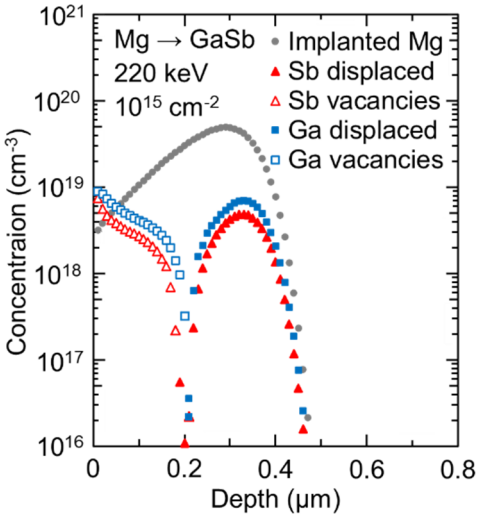


Fig. 4. Stoichiometric distribution in GaSb implanted with 220 keV Mg.

Figure 5 shows the calculated PDR as a function of the atom number of group V atoms in III-V semiconductors. The results show that PDR decreases with the increase in the group V atom number, indicating the PDR is the highest in GaN as compared to that in other III-V materials, such as GaP, GaAs and GaSb. In other words, the induced stoichiometric disturbance (N-rich) becomes most significant in GaN. We have also performed similar calculations by changing the primary Mg ion energy from 100 to 330 keV. However, it was found that the trend of PRD was calculated to be essentially the same as that in Fig.5 with only a small deviation of 3 %.

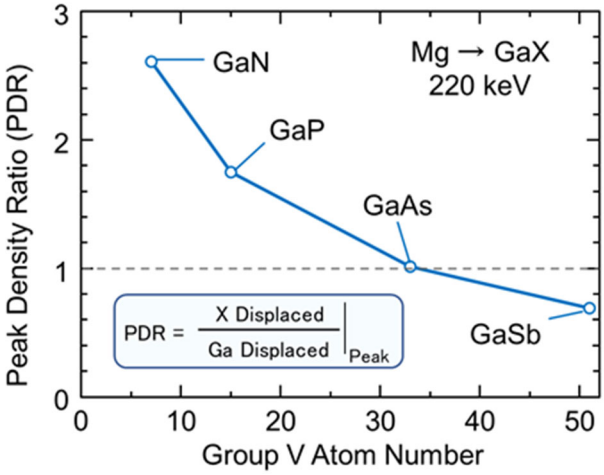


Fig. 5. Peak density ratio of displaced group III and V atoms as a function of group V atom number for GaN, GaP, GaAs, and GaSb.

## Discussion

For PDR calculation, each atom density was precisely chosen for GaN, GaP, GaAs and GaSb as $8.8\times10^{22}$, $4.9\times10^{22}$, $4.6\times10^{22}$, $3.5\times10^{22}$ $cm^{-3}$, respectively. From Fig.5, we see that the atom density gradually decreases with increasing the atom number. To see if the decrease in PDR is attributed to the atom density, the atom density was fixed at $8.8\times10^{22}$ $cm^{-3}$ (corresponding to the atom density of GaN) and the PDR was again calculated. Nevertheless, the PDR results were almost unchanged with only a slight deviation of 4%. In other words, the effect of the target material atom density on PDR is almost negligible.

To see how group V atoms affect the formation of PDR, similar calculation was performed while artificially varying the group V atom number (or atom weight). Figure 6 shows the calculated PDR as a function of the atom number of group V atom. In this calculation, the atom density was fixed at $8.8\times10^{22}$ $cm^{-3}$. Contrary to the initial expectation, PRD was found to saturate and decrease when the group V atom number was virtually reduced to less than 7, which corresponds to the atom number of N atom.

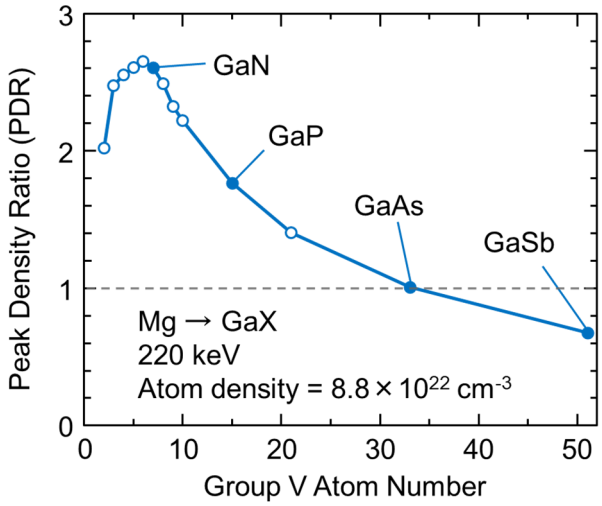


Fig. 6. Peak density ratio of displaced group III and V atoms as a function of group V atom number for GaX.

Figure 7 shows the calculated concentrations of recoil-displaced atoms as a function of the depth, together with the implanted Mg atom profile in GaX. Here, GaX is an artificial semiconductor material composed of Ga as a group III atom and X as a group V atom. When the atom number of X is 4 ($Z_X$=4), the displaced X atom profile shifts to a deeper range, as compared to the implanted Mg. On the other hand, when the atom number X is 10 ($Z_X$=10), the displaced X atoms are within the Mg profile. With a lighter atom number of X, the displaced X atoms become easier to move into a deeper region. This may presumably be the reason why PDR presented a saturated trend around an atom number of 7 and then started to decrease again when the atom number of X was further decreased to less than 7.

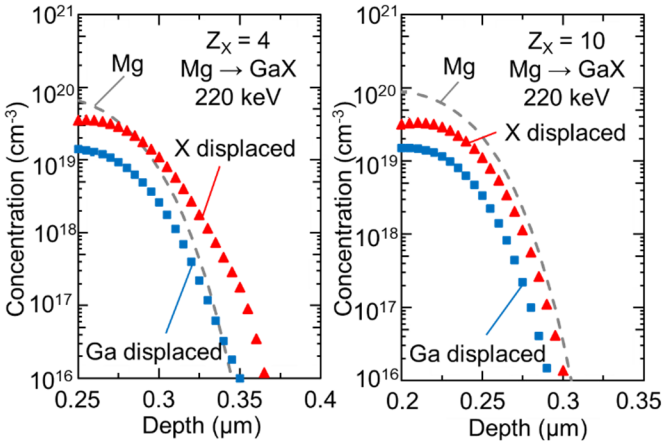


Fig. 7. Recoil-displaced atom distribution in GaX for $Z_X$=4 and $Z_X$=10.

## CONCLUSIONS

We used a Boltzmann transport approach to calculate the depth distribution of implanted primary Mg ions and the recoiled Ga and N atoms. As a result, we found that the stoichiometric disturbance is significant for Mg implanted GaN, comparing it with GaP, GaAs and GaSb. The peak density ratio of the displaced Ga and N reached 2.6. Also, we found that the stoichiometric disturbance is insensitive to the change in the implanted ion energy and the target material atom density. Among various III-V materials investigated, Mg implantation into GaN revealed the largest stoichiometric disturbance, making the formation of p-type GaN by Mg implantation more complicated and difficult than other semiconductors.

## REFERENCES


[1] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, IEEE Trans. Electron Devices 62, 414 (2015).
[2] M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, Appl. Phys. Express 1, 021104 (2008).
[3] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, Appl. Phys. Express 7, 021002 (2014).
[4] B. N. Feigelson, T. J. Anderson, M. Abraham, J. A. Freitas, J. K. Hite, C. R. Eddy, and F. J. Kub, J. Cryst. Growth 350, 21 (2012).
[5] T. Narita, T. Kachi, K. Kataoka, and T. Uesugi, Appl. Phys. Express 10, 016501 (2017).
[6] H. Sakurai, M. Omori, S. Yamada, Y. Furukawa, H. Suzuki, T. Narita, K. Kataoka, M. Horita, M. Bockowski, J. Suda, and T. Kachi, Appl. Phys. Lett. 115, 142104 (2019).
[7] H. Sakurai, T. Narita, M. Omori, S. Yamada, A. Koura, M. Iwinska, K. Kataoka, M. Horita, N. Ikarashi, M. Bockowski, J. Suda, and T. Kachi, Appl. Phys. Express 13, 086501 (2020).
[8] T. Oikawa, Y. Saijo, S. Kato, T. Mishima, and T. Nakamura, Nucl. Instrum. Methods Phys. Res. Sect. B 365, 168 (2015).
[9] T. Niwa, T. Fujii, and T. Oka, Appl. Phys. Express 10, 091002 (2017).
[10] R. Tanaka, S. Takashima, K. Ueno, H. Matsuyama, M. Edo, and K. Nakagawa, Appl. Phys. Express 12, 054001 (2019).
[11] L. A. Christel, J. F. Gibbons, and S. Mylroie, J. Appl. Phys. 51, 6176 (1980).
[12] L. A. Christel and J. F. Gibbons, J. Appl. Phys. 52, 5050 (1981).


## ACRONYMS

MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
GaN: Gallium Nitride
GaP: Gallium Phosphide
GaAs: Gallium Arsenide
GaSb: Gallium Antimonide
PDR: Peak Density Ratio

# SESSION 4:
# PLENARY 2

# Progress Towards Prolonged IC Deployment Into Previously Inaccessible Hostile Environments Via Development of SiC JFET-R ICs

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**Keywords: SiC, JFET, Integrated Circuits, High-Temperature**

**Abstract**

**This invited plenary paper summarizes recent significant progress towards development and deployment of manufacturable SiC JFET-R ICs technology for beneficial prolonged use in extreme environmental conditions previously inaccessible to semiconductor electronics.**

## INTRODUCTION

Substantial expansion of the practical environmental envelope for integrated circuit (IC) operation offers important benefits to a variety of automotive, aerospace, deep-well drilling, and manufacturing applications [1]. For the majority of these applications, ICs that can reliably operate for long time periods (years) in a harsh environment without degradation or need of diagnostic/maintenance intervention enable the largest benefits compared to IC technologies requiring added shielding, cooling, remote-location, maintenance, or other overhead in order to perform beneficial system functions. The ability to "cold-start" at low temperature (T ≤ -55 °C), continuously function through "warm-up" to reliably function at extremely high temperature (T ≥ 500 °C) through many operational cycles over years would enable significant advancements in aerospace systems including jet engines.

## DESIGN FOR HIGH-T DURABILITY

As premature failure of any weakest link would invalidate desired application benefits, a robust chain of "over-designed" technologies were developed and implemented with the overriding goal of establishing application-viable stable and prolonged operation in the most challenging environment of 500 °C air-ambient that is far beyond existing silicon and silicon-on-insulator (SOI) IC capability. In the drive to achieve 500 °C durability, other common IC performance metrics (such as high-frequency operation) were relegated to lesser priority. Key links in this durable technology chain include:

1) 4H-SiC: Among the most chemically inert of the wide band gap semiconductors, which enables dopants and interfaces to remain fixed/stable over long 500 °C operating times. Defects and thermal expansion mismatch stress present in heteroepitaxial semiconductor device systems are importantly avoided given the larger temperature span. Furthermore, there is well-established 4H-SiC wafer, homoepilayer, and power diode/transistor mass-production infrastructure that can be leveraged into manufacturing of extreme-environment ICs.

2) N-channel JFETs and resistors: The integrated device structure of Fig. 1 features inherently robust SiC pn-junctions and is thus not subject to high-T gate-oxide degradation mechanisms that preclude long-term 500 °C durability from being realized in SiC MOSFETs. Compared to SiC BJT, SiC n-JFET is far less sensitive to p-type ohmic contact resistance. Epitaxial pn junctions structurally minimize high-T leakage currents along with negative signal voltage circuit architecture that avoids forward-biasing these pn-junctions. The JFETs are depletion mode, with negative threshold voltage $V_T$ exclusively determined by the as-grown SiC homoepilayers, which to date have exhibited a systematic thickness dependence upon distance from the SiC wafer center [3].

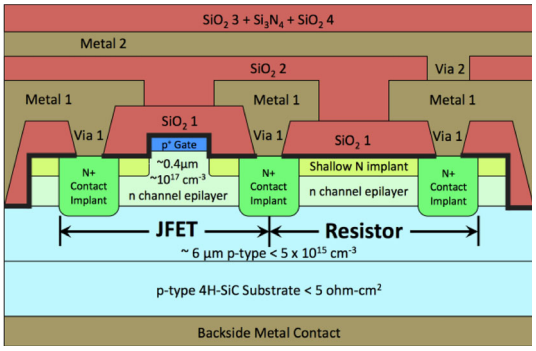


Fig. 1. Simplified cross-sectional illustration of NASA Glenn 4H-SiC JFET-R integrated device approach with two levels of interconnect [2]. The implementation of JFET and Resistor in 4H-SiC facilitates straightforward circuit design and operation over wide temperature range.

3) Layout ratio circuit design: Since JFET and resistor conductance is governed by the same 4H-SiC n-channel in Fig. 1, the temperature compensation of circuits is effectively built-in to the JFET-R IC approach as evidenced in Fig. 2 [2-5]. Circuit design is therefore specified using component dimensional layout ratios instead of T-dependent current/resistance values that can change roughly 400% between 25 °C and 500 °C. The logic gate power also changes correspondingly with temperature (e.g., from ~ 8 mW at 25 °C to ~ 2 mW at 460 °C for the Gen. 11 "Base Power" gate design). The circuit topology requires $+V_{DD}$ and $-V_{SS}$ power supplies and the signal voltages are designed negative with respect to GND. As evidenced in Fig. 2 measured data, this layout ratio topology accommodates both wafer position $V_T$ variation and T dependence.

4) Two-level 500 °C durable interconnect: The two interconnect levels enable increased circuit densities to be realized over single-level interconnect designs. Details regarding the two-level interconnect implementation and its manufacturing requirements are described in a separate invited paper at this conference [6].

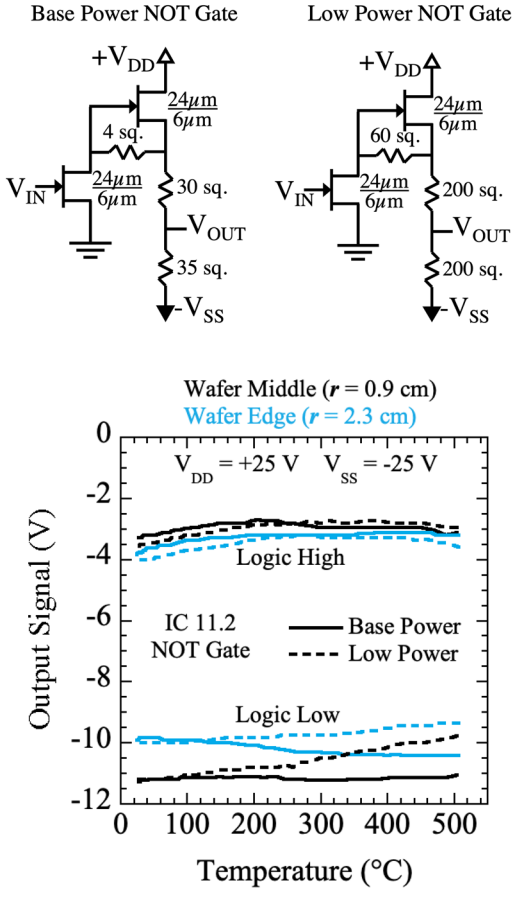


Fig. 2. SiC JFET-R logic based on shared FET/resistor n-channel and dimensional ratio design (top, schematics) enables in built-in temperature compensation (bottom, measured Gen. 11 results) [5].

5) Bond pads: Specialized "IrIS" metal stack anchored directly to SiC around the chip periphery to support gold ball wire bonds will also be described in more detail elsewhere at this conference [6].

6) Ceramic packaging and multi-chip circuit boards: Fig. 3 shows a 4-layer ceramic circuit board with SiC ICs under preparation for upcoming Venus chamber functional test. The packages and boards are implemented using custom-designed but commercially manufactured High Temperature Cofired Ceramic (HTCC) alumina packages and circuit boards with co-fired platinum conductive traces. Gold die attach is employed as described in [7]. It is worth noting that since the chips themselves withstand extremely harsh environments, the packages need not to be hermetically sealed. The attached gold wires seen in Fig. 3 will connect to nearby boards inside the chamber as well as to high-T/high-P chamber-wall feedthroughs leading to test instruments outside the chamber.

## Extreme Environment Results

Analog and digital SiC JFET-R circuits have been prototyped and tested in extreme environments. The following summarizes the pioneering results obtained during testing of various ICs fabricated during the NASA Glenn "Generation 10" prototype wafer run:

1) -190 °C to +812 °C operation: This 1022 °C temperature span was demonstrated for logic circuits without any adjustments to input voltages (Fig. 4) [4]. It is also worth noting that an 11-stage ring oscillator achieved very brief +961 °C operation [8].
2) 1 year of stable 500 °C operation: ICs approaching 200 transistors/chip were electrically operated for over 1 year

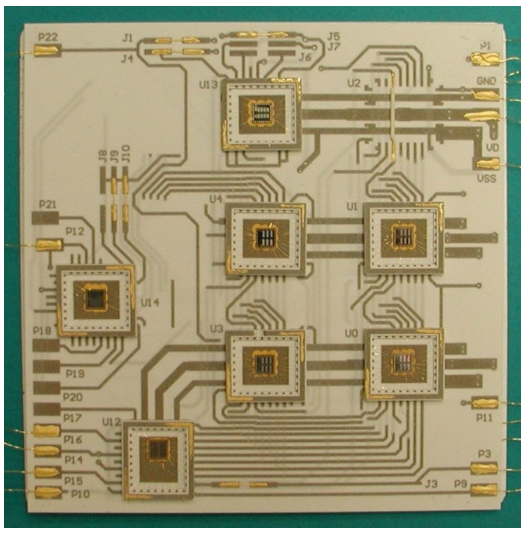

Fig. 3. Photo of 11 cm x 11 cm prototype ceramic circuit board with packaged Gen. 11 SiC JFET-R chips (prior to attaching lids) in preparation for upcoming 460 °C, 91 atmosphere Venus chamber testing [5].

in 500 °C air-ambient ovens with negligible change in circuit characteristics. 500 °C oven-testing was ended prior to all ICs failing [2].

3) Total Ionizing Dose (TID) Radiation: Gen. 10 JFET-R ICs successfully withstood 7 Mrad(Si) TID at 25 °C without any observed device failures [9]. While additional TID testing is needed to reach the TID limits of NASA Glenn SiC JFET-R ICs, prior TID studies of other SiC JFETs indicates TID immunity in excess of 100 Mrad(Si) dose levels might be obtained [10].
4) Single-Event Heavy Ion Strike Radiation: Gen. 10 ICs were tested through linear energy transfer (LET) of 86 MeV-cm$^2$/mg at 25 °C under electrical bias, and no destructive failure was observed. Soft errors were observed on some devices starting at LET of 3.5 MeV-cm$^2$/mg, but regenerative flip flops exhibited no such errors through 86 MeV-cm$^2$/mg LET [9].
5) Venus surface environment: Gen. 10 JFET-R ICs operated unprotected in 9.3 MPa 460 °C chemically caustic Venus surface environment in test chamber for 60 days without failure. The 60 days was limited by Venus test chamber availability, not the SiC ICs [11].

The number of chips subjected to each test was less than 10, and a few cases of "infant 500 °C fail" (< 2000 hours) were observed [2]. Laboratory upgrades are presently underway towards achieving greatly improved testing statistics for T ≥ 500 °C and additionally facilitate more rapid repetitive thermal cycling. Even under limited statistics, cracking of dielectric layers leading to oxidation of underlying interconnect metals has been elucidated as the clearly dominant mechanism limiting long-term high-temperature IC durability [12].

As seen in Table I, Gen. 11 ICs implemented roughly 5-fold more complex ICs than Gen. 10. This increased complexity enabled recent 500 °C demonstrations of 8-bit analog to digital converter IC as well as ~1 kbit read only memory IC (Fig. 4), among a number of other relevant capabilities including the application specific ICs (ASICs) for the Venus mission circuit board depicted in Fig. 3 [5,13]. However, the Gen. 11 interconnect process, which was altered from Gen. 10 in effort to mitigate dielectric cracking as well as enable larger die size, resulted in metal peeling near the wafer periphery, degraded dielectric cracking properties, and subsequently inferior circuit yields [14]. In contrast to yearlong 500 °C durability achieved in Gen. 10, no Gen. 11 chips oven-tested to date have reached 1000 hours of 500 °C operation without malfunction. Therefore, presently on-going development of improved interconnect/dielectric is paramount to successful realization of 500 °C durable Gen. 12 prototype ICs.

## Progress Towards Manufacturing

With the initial technical foundation of greatly expanded environmental envelope established, present work beyond further interconnect optimization includes upscaling chip-complexity in parallel with lowering barriers to manufacturability and application infusion. Table I shows progress in relevant IC benchmarks for the most-recent successive developmental prototype generations of NASA Glenn JFET-R chips.

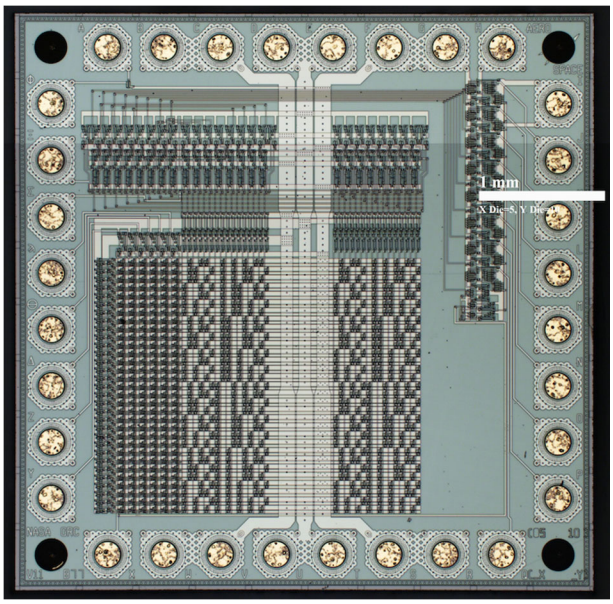

Fig. 4. Photo of 4.65 mm x 4.65 mm 992-bit IC Version 11.3 read-only memory chip prior to packaging and testing at 500 °C.

TABLE I
Major Design Metrics for Recent Generations of Extreme Environment Durable SiC JFET-R ICs

| | **Gen. 10** | **Gen. 11** | **Gen. 12** | **Gen. 13** |
|---|---|---|---|---|
| Gate Length | 6 µm | 6 µm | 3 µm | 3 µm |
| Res. Width | 6 µm | 3 µm | 2 µm | 1 µm |
| Contact Via | 6 µm | 6 µm | 3 µm | 2 µm |
| JFETs/Chip | ~ 200 | ~ 1000 | ~ 3000 | ~ 10000 |
| Die Width | 3 mm | 4.65 mm | 5 mm | 5 mm |
| Year | 2017 | 2019 | 2022* | 2023 |

* Delayed by prolonged COVID-19 NASA Glenn lab closure.

With modest adjustments, the SiC JFET-R fabrication process is compatible with semiconductor mass-production tools and materials. A separate paper at this conference will describe key issues to be addressed in transferring the SiC JFET-R IC process to semiconductor foundry manufacturing [6]. Towards this end, the processing that forms the SiC JFETs and resistors (without interconnect) for the IC Gen. 12 prototype IC run was recently competitively outsourced [15]. However, completion of the IC Gen. 12 fabrication run has been postponed by prolonged closure of the NASA Glenn SiC microfabrication laboratory arising from the COVID-19 pandemic.

Since accessibility and commercialization are key to technology infusion, NASA Glenn has entered formal partnerships to prototype limited numbers of developmental SiC JFET-R IC chips. Likewise, basic device/circuit models and mask layout design guidelines were publicly posted [16] and a basic device process development kit (PDK) was implemented for the design phase of the NASA Glenn JFET-R IC Gen. 12 wafer run. Potential users can thus explore circuit capabilities and possible benefits via design and simulation of their own application-specific JFET-R ICs. SiC JFET-R IC design services are also commercially available [17]. Under negotiated technology transfer and licensing agreements, a number of outside-user device designs have been prototyped in NASA Glenn SiC JFET-R wafers starting with IC Gen. 11. The next opportunity for prospective users to have devices fabricated on NASA Glenn developmental wafers will be the IC Gen. 13 SiC JFET-R prototype run slated to start in 2022. To facilitate substantial device shrinkage and corresponding chip complexity upscaling over Gen. 12 (as seen in Table I), stepper-based photolithography is planned for Gen. 13 IC fabrication. IC Gen. 13 calculated SPICE JFET and resistor device models and mask layout rules are posted online, and a basic Gen. 13 PDK will also become available in the near future [16].

Completing the SiC JFET-R electronics commercial design and production chain will lower investment and risk barriers to useful application deployment. Demonstrations of system benefits are also important. For NASA, an initial high-value deployment is opening the Venus surface to extended missions with greatly improved robotic scientific data return.

## Enabling Infusion At NASA: Venus Landers

Long-term operation of silicon-based integrated circuits (ICs) has enabled a variety Mars lander missions to successfully operate in its cold (-143 °C to +27 °C) atmospheric environment returning valuably insightful scientific data for years. However, since Venus surface conditions fall well beyond the operating realm of silicon-based ICs, all prior Venus landers have employed high-mass pressure vessels and/or thermal insulation systems to protect mission-critical IC electronics from the ~ 460 °C, ~ 91 atm. pressure highly reactive atmospheric environment. Such protection measures have only worked for an hour or two before the surrounding Venus environment overcame the protection and thermally failed the silicon IC-based lander electronics. To date, the longest duration of data return from the surface of Venus surface is 2 hours and 7 minutes in 1978 by the ~760 kg Venera 13 lander [18,19]. A number of updated Venus lander designs relying on sheltered electronics have been studied over the intervening decades, including combinations of active cooling (refrigerator) subsystems and expanded silicon-IC capabilities. None of these sheltered-electronics approaches have increased surface science duration beyond a single day, and none have come in at less than 500 kg mass [18,19]. *The historical consequence of these severe drawbacks has been that no landers have touched down on the surface of Venus in over three decades, despite the widely recognized high scientific value of obtaining more comprehensive observations from the surface of Venus.*

Fig. 5. Comparison of proposed NASA Venus lander designs based upon sheltered electronics (left, [18]) versus unsheltered SiC electronics (right, [20]).

The proven ability of NASA Glenn SiC JFET-R ICs to function for 60 days immersed in the Venus surface environment without sheltering [11] offers sea-change improvements to Venus surface missions and scientific understanding. Based upon this realization, NASA has now initiated development of paradigm-shifting Venus surface mission concepts and demonstration hardware. One example of such a mission concept is the ~ 10 kg Long-Lived (or Long-Life) In-Situ Solar System Explorer (LLISSE) lander designed to return Venus surface meteorological data (including temperature, pressure, wind, and concentrations of selected atmospheric gasses) for more than 60 days [20]. Another example based on the same fundamental approach but with emphasis on seismology is the Seismic and Atmospheric Exploration of Venus (SAEVe) lander [21]. *By eliminating the need to protect its electronics from the Venus surface environment, the LLISSE and SAEVe concepts promise the order of 50-fold improvements in both mission duration and lander mass compared to designs that rely on environmentally sheltered electronics.* To complete such landers, sensors, energy storage (batteries), antennas, mechanical structure, etc. that are simultaneously low-mass, compact, and can effectively function for months immersed in the Venus surface environment without any cooling are undergoing parallel development along with mission-specific SiC JFET-R ICs. Landings on Venus are anticipated following long-term proofs of completely functional prototype landers in Venus atmospheric test chambers [22].

## Conclusion

With the recent advancements in SiC JFET-R IC technology summarized in this paper, beneficial long-term IC deployment into previously unreachable extreme application environments is becoming enabled. This uniquely durable technology chain, starting from commercial SiC epiwafers through ceramic multi-chip circuit boards, can be realized via

modest modifications to standard IC design and mass-production practices and tooling. Further maturation and upscaling of this new capability is expected to take place in parallel with initial infusion deployments and transition to commercial manufacturing.

## Acknowledgements

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## References

[1] J. D. Cressler and H. A. Mantooth, *Extreme Environment Electronics* Boca Raton: CRC Press, 2013. https://doi.org/10.1201/b13001

[2] P. Neudeck, et al., *Proc. 2018 IMAPS Int. Conf. High Temperature Electronics*, pp. 71-78. https://ntrs.nasa.gov/citations/20180003391

[3] P. Neudeck, et al., *Proc. 2016 IMAPS Int. Conf. High Temperature Electronics*, pp. 263-271. https://ntrs.nasa.gov/citations/20160014886

[4] P. Neudeck et al., Materials Science Forum, vol. 963, pp. 813-817 (2019). https://ntrs.nasa.gov/citations/20190027358

[5] P. Neudeck et al., to appear in *Proc. 2020 IEEE Int. Electron Devices Meeting (IEDM 2020)*.

[6] D. Spry et al., to be presented at CS MANTECH 2021.

[7] L. Chen et al., *Proc. 2016 IMAPS Int. Conf. High Temperature Electronics*, pp. 66-72. https://ntrs.nasa.gov/citations/20160014867

[8] P. Neudeck et al., IEEE Electron Device Lett., vol. 38, pp. 1082-1085 (2017) https://doi.org/10.1109/LED.2017.2719280

[9] J. Lauenstein, et al., *Proc. 2019 IEEE Radiation Effects Data Workshop.* https://ntrs.nasa.gov/citations/20190031951

[10] J. McGarrity, et al., IEEE Trans. Nuclear Science, vol. 39, pp. 1974-1981 (1992) https://doi.org/10.1109/23.211393

[11] P. Neudeck, et al., IEEE J. Electron Devices Soc., vol. 7, pp. 100-110 (2018) https://doi.org/10.1109/JEDS.2018.2882693

[12] D. Spry, et al., *Proc. 2016 IMAPS Int. Conf. High Temperature Electronics*, pp. 249-256. https://ntrs.nasa.gov/citations/20160014879

[13] P. Neudeck, et al., to appear in *Proc. 2021 IMAPS Int. Conf. High Temperature Electronics*.

[14] D. Spry, et al., Materials Science Forum, vol. 1004, pp. 1148-1155 (2020). https://doi.org/10.4028/www.scientific.net/MSF.1004.1148

[15] GE Research, Niskayuna, NY USA, as a subrecipient under OASIS Contract GS00Q140ADU106; Pool 1

[16] NASA Glenn SiC JFET IC Tech Guide http://go.nasa.gov/jfetic

[17] Ozark Integrated Circuits, Inc. https://www.ozarkic.com/our-services/high-temperature/

[18] J. L. Hall, et al., *Final Report of the Venus Science and Technology Definition Team Venus Flagship Mission Study*, Apr. 2009 https://vfm.jpl.nasa.gov

[19] E. Kolawa, et al., *Extreme Environment Technologies for Future Space Science Missions*, Sep. 2007 http://www.vfm.jpl.nasa.gov/files/EE-Report_FINAL.pdf

[20] T. Kremic et al., *Long-life in-situ solar system explorer (LLISSE) probe concept and enabling high temperature electronics*, 48th Lunar Planetary Sci. Conf, Mar. 2017, https://www.hou.usra.edu/meetings/lpsc2017/pdf/2986.pdf

[21] T. Kremic et al., *SAEVe: A concept study for a long duration small sat class Venus lander*, 49th Lunar Planetary Sci. Conf, Mar. 2018, https://www.hou.usra.edu/meetings/lpsc2018/pdf/2744.pdf

[22] Glenn Extreme Environments Rig (GEER), https://www1.grc.nasa.gov/space/geer/

## Acronyms

ASIC: Application Specific Integrated Circuit
BJT: Bipolar Junction Transistor
GE: General Electric
GND: Ground
HTCC: High Temperature Co-fired Ceramic
IC: Integrated Circuit
IrIS: Iridium Interfacial Stack
JFET: Junction Field Effect Transistor
JFET-R: Junction Field Effect Transistor & Resistor
LET: Linear Energy Transfer
LLISSE: Long-Lived (or Long-Life) In-Situ Solar System Explorer
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
NASA: National Aeronautics and Space Administration
PDK: Process Development Kit
SAEVe: Seismic and Atmospheric Exploration of Venus
SiC: Silicon Carbide
SOI: Silicon On Insulator
T: Temperature
TID: Total Ionizing Dose
$V_T$: JFET Threshold Voltage

# The Rise of Power SiC and GaN Market and The Impact of COVID-19

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**Keywords: EV/HEV, Wide bandgap semiconductor, Gan, SiC, main inverter, fast charger**

**Abstract**

**Despite the COVID-19 outbreak, the power Silicon Carbide (SiC) and GaN market continue their ascension. The high growth of the EV/HEV market impacted significantly the wide SiC industry, numerous carmakers continue qualifying SiC devices in main inverters, on-board chargers (OBC) and DC/DC converters. While GaN has found its killer application in consumer fast charging. This paper provides an overview of SiC and GaN device technology, including Yole Développement's understanding of the market's current dynamics and future evolution of wide band gap materials compared to mainstream Silicon power electronics market.**

## INTRODUCTION

While the COVID-19 has had a swift and severe effect on several manufacturing industries including automotive and consumer, SiC and GaN fabrication shrugs off pandemic and continue to grow. For example, Tesla have had a shutdown in the beginning of 2020, however its sales of electric cars accelerated by the end of the year and hit a new record despite difficult first half.

The main inverter market is still driving the SiC based electric and hybrid electric vehicles (EV/HEV), with more than $300B of EV/HEV investments announced by different OEMs [1], clearly confirming the automotive industry's commitment to governmental CO2 reduction targets.

New players from different technology areas (material and equipment suppliers, power electronic device manufacturer, system integrators, car makers…) are entering EV/HEV business. New divisions or joint ventures fully dedicated to EV/HEVs are being established by many companies. The strong technology requirements and at the same time tough product qualification challenges call for development of new power electronic technologies. The high volume demand for EV/HEV attracts many players to be first to develop and implement such new solutions.

EV/HEV charging, energy storage and other markets related to the EV/HEV follow the trends in the EV/HEV industry: increasing EV battery pack voltage (400V/800V) leading to demand for 1,200 V rated power electronic devices. The companies involved in related applications have to continuously adapt their products while often benefiting of the technology development done for EV/HEVs.

In the consumer market, the ever-evolving power-hungry smartphones are increasing their battery capabilities to accommodate their multi-functionalities. Thus, pressuring the smartphone industry to find solutions to reduce the charging time, which became a crucial parameter for OEMs and an important differentiator for the choice of the flagship. Chargers are preferably low on cost, efficient, and small. This approach is favorable for the use of GaN HEMT where

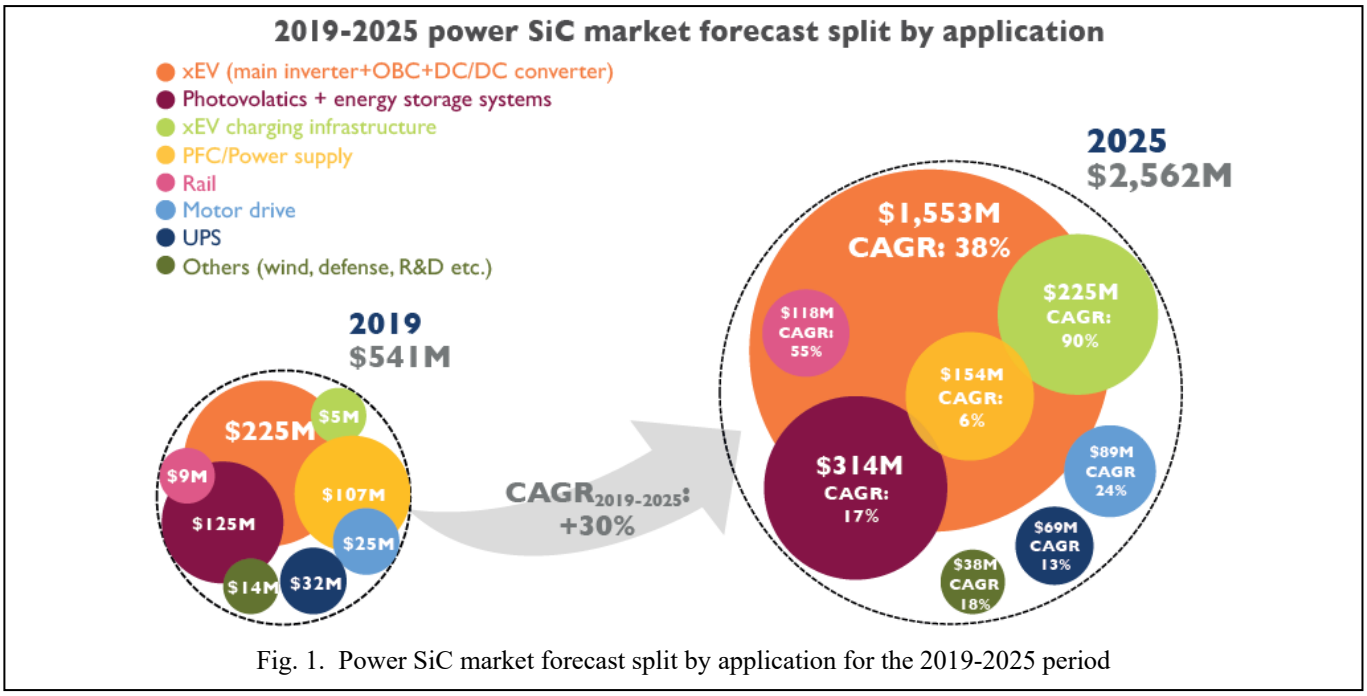


Fig. 1. Power SiC market forecast split by application for the 2019-2025 period

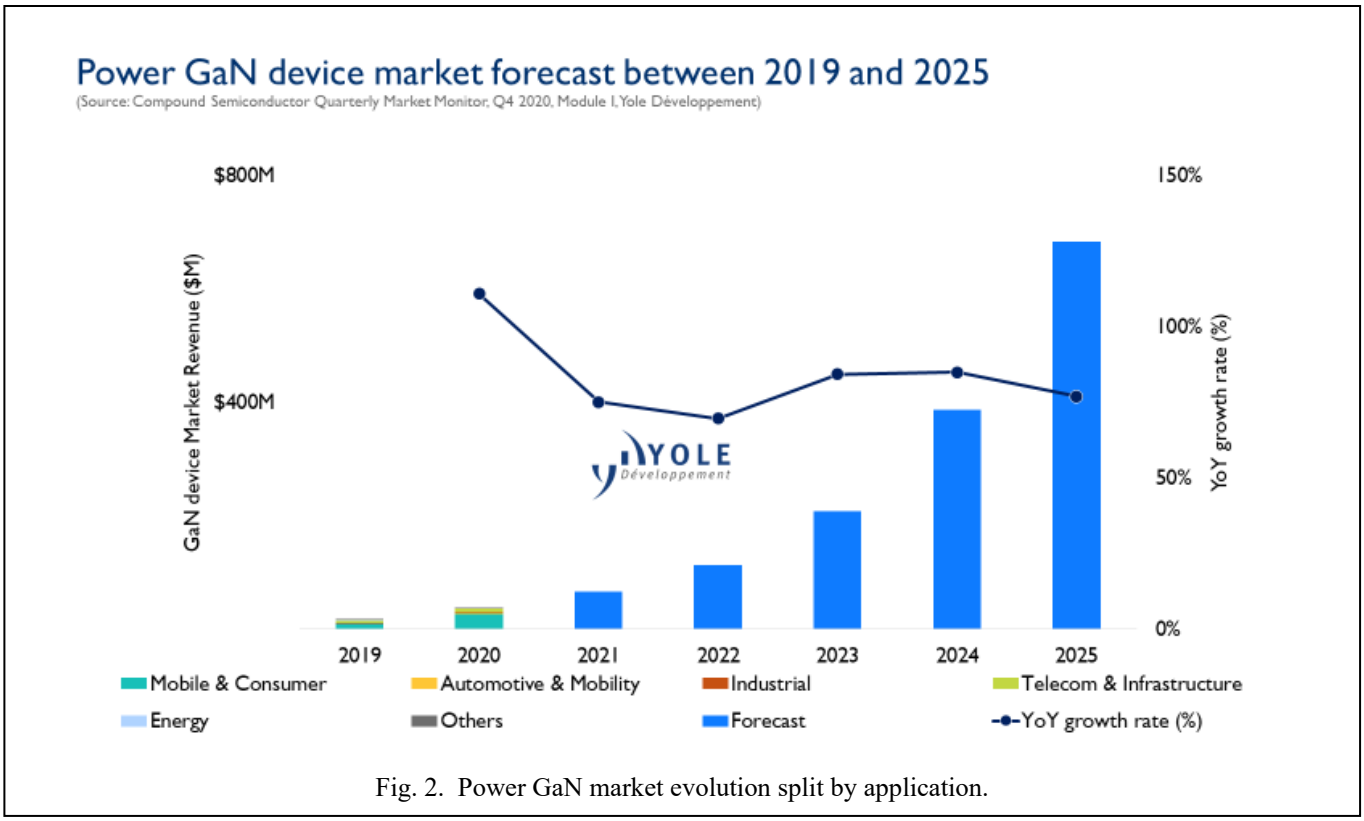


Fig. 2. Power GaN market evolution split by application.

traditional silicon semiconductor is limited to switching frequencies of a few hundred kilohertz, whereas GaN goes beyond the megahertz range. Combining its high frequency capacity and its high-power density, GaN-based product entered the fast charger application with augmented power devices in a compact design.

Regarding the compound semiconductor industry, vehicle electrification and phone fast charging bring new market opportunities for wide band gap materials such as SiC and GaN.

## MARKET OPPORTUNITIES FOR SIC

The 2018 - 2019 SiC power device market is notable for Tesla's adoption of SiC in its main inverter. Recently, several carmakers have multiplied announcements for SiC solution design wins. In 2020, BYD has also adopted SiC-based main inverter solutions for its premium models. Other carmakers, such as Audi, Volkswagen, and Hyundai, are expected to adopt SiC in their next-generation models. Moreover, 800V battery vehicles represent a significant market opportunity for SiC owing to its interesting performance/cost ratio compared to silicon IGBTs. Players like STMicroelectronics, Infineon, Rohm, Onsemi and GE have already 1200V AEC qualified SiC MOSFETs and are ready to serve this market.

The xEV market is the primary market driver for Si power devices, and it is the source of excitement for SiC - which is not surprising at all.

Forecasts range from the conservative, at several hundred million dollars, to optimistic, such as the $3 billion estimate from STMicroelectronics. But they all agree that the SiC market is poised for healthy growth driven by the automotive segment.

Based on our discussions with different players, Yole sees a prospering SiC power device market. In fact, we expect the SiC power semiconductor market's value to approach $2.5B by 2025, with a compound annual growth rate (CAGR) of 30% for 2019 – 2025 (See Fig. 1) [2].

The automotive market is undoubtedly the foremost driver, and as such will hold around 60% of total device market share in 2025.

In 2018, the increase of wafer demand as well as the transition from 4" to 6" resulted in wafer shortages. Consequently, securing wafer supply has become the priority for device manufacturers. Several companies invested heavily, and others signed long-term supply agreements. In parallel, the US-China trade tensions, accelerated the domestic supply chain development in China, with more than $2 billion invested in SiC covering wafer, epiwafer and device.

Along with EV applications, SiC is of great interest to the charging infrastructure market, which is growing significantly. Indeed, high power chargers can benefit from SiC's higher efficiency and higher frequency by offering more business. By acquiring Ascatron and Innovion and licensing GE's SiC module technology, II-VI has internalized

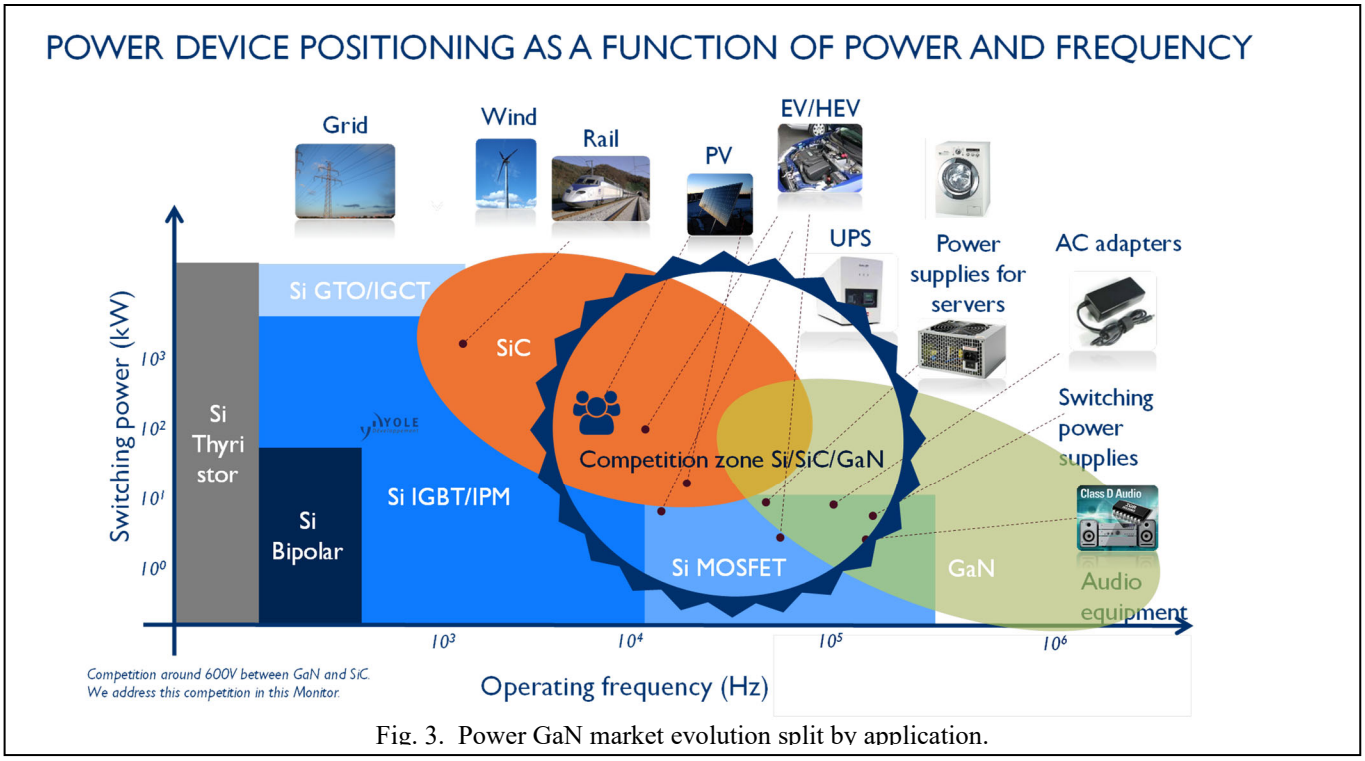


Fig. 3. Power GaN market evolution split by application.

the epi and device manufacturing steps in order to secure new business in the growing module market.

The SiC market is very dynamic, with lots of investments as well as partnerships to accelerate the time to market. Regarding the module business, in the 2019-2020 period, Cree partnered with StarPower, ABB, ZF and Delphi for SiC-based power train systems for electric cars and e-buses. ROHM teamed up with Vitesco and Leadrive Technologies to work on SiC powertrain solutions. Automotive Tier 1 player Bosch is also internally developing SiC modules.

## Market Opportunities for GaN

For the GaN power market, the adoption of GaN HEMTs for Oppo's in-box fast charger at the end of 2019 boosted the penetration of this wide bandgap material. Indeed, several OEMs such as Oppo, Vivo, Realme and Meizu rushed to adopt GaN-based inbox fast charger for their flagship released in early 2020. Also, other players such as Samsung and Xiaomi have opted for GaN accessory chargers.

Another high-volume market opportunity can be found in automotive applications, where several OEMs are interested in GaN HEMT devices and currently testing and qualifying the technology. GaN is of great interest in 48/12V DC-DC converters in mild-hybrid electric vehicles and bi-directional on-board charging applications in electric-vehicles. Various Tier 1s, e.g. Valeo and Continental are already using and qualifying GaN product. Players like EPC, Transphorm, GaN Systems, and Texas Instruments have already obtained AEC qualification. Yole expects that GaN power will enter automotive OEM's supply chain and enjoy increasing volumes starting from 2023-2024.

The GaN journey has just started with the end-consumer mass market where it will gain volume production. In a few years, it will expand in the automotive and industrial market. The GaN device market is poised to reach more than $700 million in 2025 (See Fig. 2) [3-4].

## SiC and GaN

SiC and GaN will compete around 600V. For applications with high power demand and high voltages such as rail, wind, and power grid, SiC will be preferred. For applications with small power demand and high frequency benefits like consumer fast chargers, and small power supplies for servers, GaN will be the winner (See Fig. 3) [4].

In automotive applications, the competition is again power dependent. We see an increasing demand for SiC in the inverter with high power. Depending on the evolution of GaN device, the cost erosion, and topology technologies, we might see GaN penetrating the low power inverters (small cars, urban vehicles…) in the long-term. In Off-board chargers SiC will be dominating this market, whereas in onboard chargers, we expect GaN to bring some benefits by increasing the Watts per Kg. For DC/DC applications, in high voltage there will be a co-existence of both technologies, and a slight advantage to GaN for bi-directionality function.

## Conclusions

The industry shook after the pandemic hit most factories from raw materials to device level. However, wide band gap materials SiC and GaN stood and emerged with a positive outcome, they clearly show a strong growth potential in

EV/HEV and consumer market, respectively. Both compound semiconductors have significant added values and challenges for market adoption.

## REFERENCES


[1] Yole Report: Power Electronics for Electric & Hybrid Electric Vehicles 2020
[2] Yole Report: Power SiC Market: Applications, Players, Technology, and Substrates 2020
[3] Yole Report: Power GaN Market: Applications, Players, Technology, and Substrates 2019
[4] Yole's - Compound Semiconductor Monitor Service Q4-2020: Module I: Power SiC and Power GaN


## ACRONYMS

EV/HEV: electric vehicles/ hybrid electric vehicles
BEV: battery electric vehicles
PHEV: plug-in hybrid electric vehicles
CAGR: Compound Annual Growth Rate
IGBT: insulated-gate bipolar transistor
OEM: original equipment manufacturer

# Processing Choices for Achieving Long Term IC Operation at 500° C

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**Keywords: SiC, JFET, Integrated Circuits, High-Temperature, Dielectric, LPCVD**

**Abstract: The prospects for beneficial infusion of integrated circuits (ICs) into previously inaccessible extreme-temperature application environments has increased with recent NASA Glenn demonstrations of 4H-SiC Junction Field Effect Transistor & Resistor (JFET-R) chips functioning for over a year at 500 °C in air ambient [1]. This paper focuses on fabrication process choices believed key to demonstrated 500 °C durability that must be considered when porting this uniquely durable IC capability into commercial foundry manufacturing.**

## INTRODUCTION

Stable and long-term functionality is a requirement for beneficial integrated circuit (IC) electronics deployment into applications. While it has been known for decades that wide band gap semiconductor's ability to operate near 500 °C would enable worthwhile benefits to aerospace, automotive, drilling, and other applications, there has essentially been no such practical deployments due to lack of stable long-term operation at this temperature. To address this critical gap to enable IC electronics capability to these important applications, the NASA Glenn SiC JFET-R process was developed emphasizing "over-design for durability" prioritized over other IC performance metrics (e.g., circuit speed). To date, ICs prototyped using this process are the only chips ever reported to demonstrate more than one year of stable operation at 500 °C [1].

The fundamental technology cross-section developed is shown in an experimentally realized cross-section in Fig. 1. For the SiC JFET-R process flow, the "front end of the line" (FEOL) process defines inherently durable transistors and resistors in commercially procured 4H-SiC homoepilayers [2]. The FEOL involves reactive ion etching SiC epi to define JFET and resistors devices along with three ion implants (two n-type, one p-type, all activated by the same anneal) that respectively facilitate source/drain contacts, lowered JFET resistance, and suppresses parasitic field inversion conduction [1,3,4]. The FEOL processing steps are sufficiently straightforward and widely practiced in the manufacture of conventional-temperature SiC high-power devices that NASA chose to migrate them into commercial SiC foundry for the most recent (COVID-19 delayed) "Version 12" JFET-R IC run [5].

The arguably tougher challenge to achieving prolonged IC operation at 500 °C resides at the "back end of the line" BEOL that implements two levels of metal interconnect followed by wire bonding pads. This paper explores key durability aspects the BEOL interconnect process, including experimental annealing results and core fabrication philosophies that to this day are crucially guiding the processing evolution of this technology.

## BEOL ANNEAL EXPERIMENTS

As described previously, the $SiO_2$ interlayer dielectrics films seen in Fig. 1 are deposited at 720 °C via low-pressure chemical vapor deposition (LPCVD) using tetraethyl orthosilicate (TEOS) precursor, while $TaSi_2$ "Metal 1" and "Metal 2" films are deposited via close-proximity sputtering (21 mm target to substrate space) in order to minimize void formation over topologic features [1,3].

A series of accelerated age testing experiments provided key insights that foundationally guided BEOL process development choices. A series of individual non-functioning chips from an earlier unsuccessful version of the NASA Glenn JFET IC were each subjected to 30 minute anneals in either $N_2$ or $H_2$:$N_2$ 4% forming gas at one of the following temperatures: 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, or 1370 °C. All samples were optical-imaged before and after the anneal and selected samples were then focused ion beam (FIB) cross-sectioned to further document basic material failure points. The four district chip features were in-depth examined as follows: 1) the edge of a wide Metal 2 power bus, 2) the central region of a larger area capacitor, 3) an "IrIS" bond pad [6] capped with 1 µm gold to somewhat mimic the presence of a Au ball wire bond had the chip had been fully packaged [7], and 4) an uncapped IrIS bond pad.

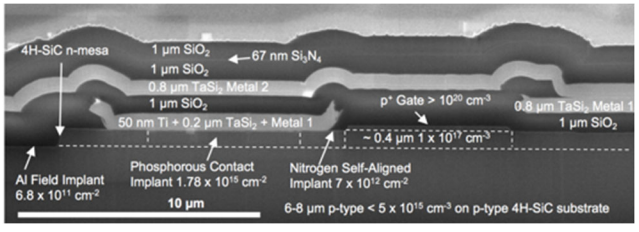


Fig. 1. Scanning electron micrograph cross-section of the source and gate region of an as-fabricated 500 °C durable 4H-SiC JFET with two levels of interconnect from the NASA Glenn Version 10 prototype wafer run [1]

Table I summarizes the major outcomes of this study. Each of the 4 columns of the table corresponds to one of these 4 respective chip features while each row corresponds to the anneal temperature the chip was subjected to. The thicker red lines in the table demarcate the ascertained effective upper temperature limit of the BEOL processing for each respective chip feature studied. As seen in Table I, the bond pads effectively limit the overall chip microstructural durability.

*Bond Pad Feature Temperature Limits:* As supported by the post-anneal cross-section images collected from 500 °C, 700 °C, and 900 °C annealed IrIS bond pads shown in Fig. 2, the first clear BEOL structural temperature limit is found just above 700 °C. For the Fig. 2a image after 500 °C anneal the IrIS stack has segregated into its planed layers of $TaSi_2$ that contacts the underlying SiC, $PtSi_X$, Ir, Pt and a top Au metal. While the Fig. 2b post 700 °C image of bond pad without Au cap reveals a thickened $PtSi_X$ zone that comes closer to SiC interface, the contact remains a smooth and abrupt interface between $TaSi_2$ and SiC. However, the Fig. 2c image of 700 °C anneal IrIS stack with Au cap shows evidence of oxygen accumulation at the Au/Pt interface which could become a bonding failure point if the Au ball bond attached during chip packaging is not thick enough to prevent oxygen penetration. By 900 °C, the Fig. 2d image shows Pt has reached the SiC interface along with evidence of voiding (white arrow).

*Oxide and Metal 2 Temperature Limits:* The second clear BEOL structural temperature limit is found at 1200 °C for the LPCVD TEOS $SiO_2$ and $TaSi_2$. The Fig. 3a, b, and c cross-section images of samples after 1000 °C and 1100 °C anneals all show about the same $TaSi_2$ microstructure and Metal 2 trace shrinkage along the edges of the metal. The largest

TABLE I
EXPERIMENTAL SUMMARY OF ANNEALS ON SELECTED CHIP FEATURES (COLUMNS) AS A FUNCTION OF ANNEALING TEMPERATURE (ROWS)

| Anneal T °C | Power Bus | Capacitor | Au Capped Bond Pad | Uncapped Bond Pad |
|---|---|---|---|---|
| 500 | | | | Nominal |
| 600 | | | | |
| 700 | | | w/Au +oxide | PtSix grows |
| 800 | | | | |
| 900 | | | | Pt reaches SiC |
| 1000 | Nominal | | | |
| 1000 | FMG ~ N2 | Metal 1 vs. 2 | | |
| 1100 | ~1000 | | | |
| 1200 | TaSi2 chg | | | |
| 1300 | 3 layers | | | |
| 1370 | 1 layer | | Au/Pt trees | Pt nano wires |

N2:H2 Foming gas 4%
FIB image (not shown)
FIB image shown
SEM image (not shown)
Optical image (not shown)
upper temperature limit

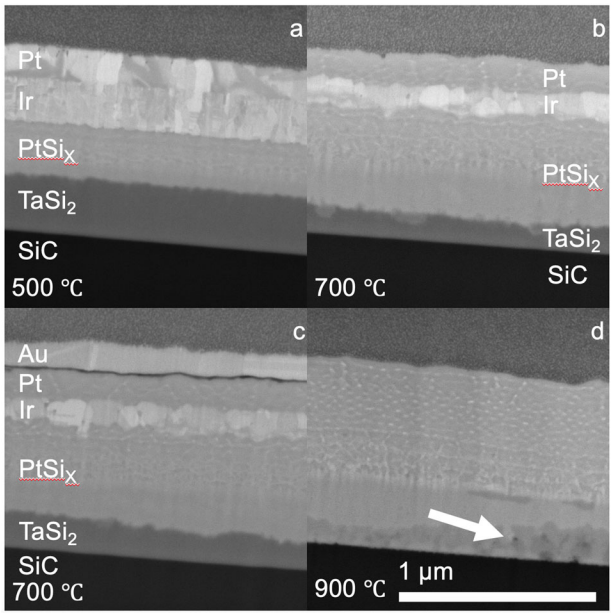


Fig. 2. FESEM images of a FIB cross-section of "IrIS" bond pads, each subjected to single 30 minute anneal in N2 at (a) 500 °C, (b, c) 700 °C, and (d) 900 °C. For the 900 °C anneal Pt has reached the SiC surface and there is onset of void formation as denoted by white arrow.

difference in these images/samples is that samples anneal in FMG exhibits more charging of the dielectric despite the fact that all images were taken under the same field emission scanning electron microscope (FESEM) conditions. For sample subjected to 1200 °C anneal, Figure 3d shows that at 1200 °C the amount of $TaSi_2$ shrinkage increased slightly along with observable change to the $TaSi_2$ microstructure. The top and bottom interfaces of the $TaSi_2$ Metal 2 trace is also roughening. The sample annealed at 1300 °C (Fig. 3e) shows clear relaxation of the dielectric resulting in a large void and substantial restructuring of the $TaSi_2$, yet some of the layered TaSi2 microstructure is still apparent. The Fig. 3f image of the 1370 °C annealed sample reveals a nearly circular relaxation void with evidence of metal redeposition on the interior walls of the void, and there is also no longer layered microstructure evident to the $TaSi_2$.

It is worth noting that no dielectric cracks were observed to form on any of these samples. Dielectric cracks have been observed in subsequent prototype IC generations that added $Si_3N_4$ layers (e.g., Fig. 1) that function as mitigation against mobile ion contamination circuit effects [1,5].

*Comparison of Metal 1 vs. Metal 2:* In order to assist ohmic contact formation to SiC, titanium was deposited as the first layer of the Metal 1 Ti/$TaSi_2$ stack in early generations NASA Glenn SiC JFET-R prototype ICs. Fig. 4 shows a cross-sectional image recorded near the horizontal center of a large-area Metal 1 / TEOS $SiO_2$ / Metal 2 capacitor device following annealing at 1000 °C for 30 minutes in FMG. Note that the Metal 2 $TaSi_2$ layer exhibits more-ordered layer-

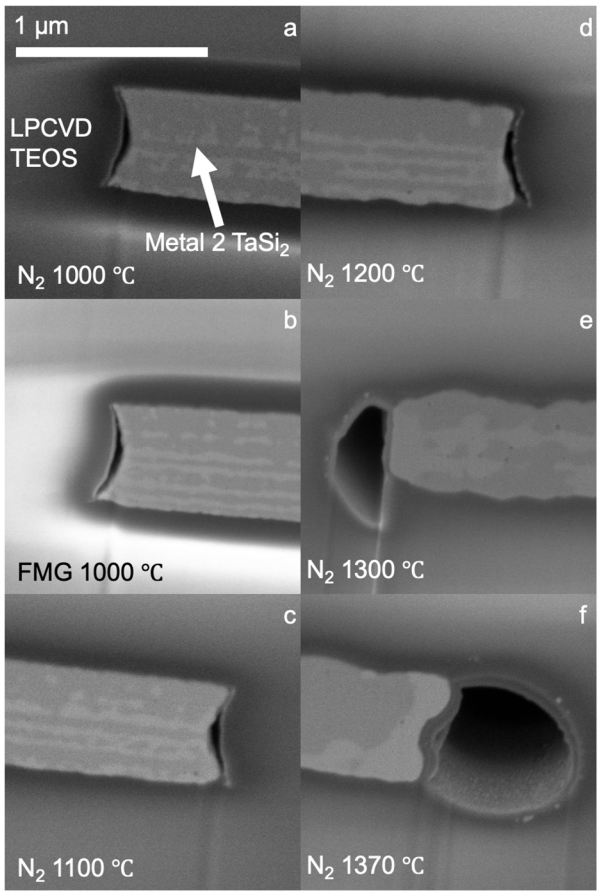


Fig. 3. FESEM images of a FIB cross-section of edges of Metal 2 power bus line feature. All anneals are 30 minutes. (a), (c)-(f), were annealed in $N_2$. (b) was annealed in $N_2$:$H_2$ 4% FMG.

structure than Metal 1, and there is also evidence of voids in the Metal 1 titanium layer. It can also be observed in Fig. 4 that Metal 1 is noticeably thicker than Metal 2.

Void formation is mitigated with titanium deposited only inside etched Via 1 areas where SiC ohmic contact is needed using a plug-metal process described in [1,8].

## BEOL Process Integration Approach

In addition to the fundamental microstructure thermal behaviors described in the preceding section, this section describes important core process integration approaches adopted to maximize BEOL interconnect and bonding pad long-term 500 °C operational durability.

The first is to take full advantage of the physical hardness of SiC as the foundation for anchoring the highest-stress features. In particular, the "IrIS" metal bond pads are over 100 µm in diameter and physically the largest features on each SiC chip, and they also withstand the largest materials mismatch in Coefficient of Thermal Expansion (CTE) [6]. To withstand the CTE mismatch over the inherently larger than 500 °C range of desired operating temperature, the wire bonding pads

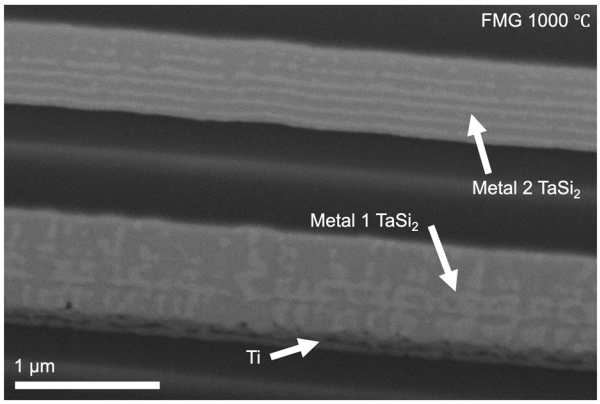


Fig. 4. FESEM images of a FIB cross-section of central region of Metal 1 / TEOS SiO2 / Metal 2 capacitor following 30-minute 1000 °C anneal in $N_2$:$H_2$ 4% FMG.

are strategically anchored directly to the single-crystal SiC, and they are also location-confined to outer periphery regions of each chip. To further limit/confine stress/damage effects, the bond pads are also physically isolated from any direct attachment of Metal 1 and Metal 2 interconnect traces. Heavily doped SiC serves as the electrical "bridge" of signals between "IrIS" bond pads and Metal 1 interconnect traces [9].

Another major durability-enhancing philosophy is to minimize unique processing steps and their associated processing materials. Instead of employing Cu interconnect traces with $TaSi_2$ (or other material) liners as done for many silicon ICs, 1 µm thick $TaSi_2$ is instead employed as the sole material for both levels of interconnecting metal between on-chip transistors and resistors [1,3]. Close-proximity (21 mm target to wafer spacing) sputtering if $TaSi_2$ is carried out via pulsed-DC or High-Power Impulse Magnetron Sputtering (HIPIMS). Other methods of $TaSi_2$ deposition (e.g., CVD) as well as silicon-rich films may also work, so long as uniformly dense film coverage over ~ 1 µm surface topology features (imposed by underlying features such as etched SiC mesas as seen in Fig. 1) is achieved.

The third key philosophy is to deposit all dielectric layers at the same temperature (720 °C) that is also well above the desired 500 °C designed IC operating temperature. This approach ensures that maximum film stresses occur near room temperature instead of high temperature. $SiO_2$ dielectric is deposited at 720 °C using Low Pressure Chemical Vapor Deposition (LPCVD) via TetraEthyl OrthoSilicate (TEOS) precursor. Thin stochiometric $Si_3N_4$ films (again, LPCVD deposited at 720 °C) are sandwiched between $SiO_2$ layers (as seen in Fig. 1) with startlingly profound impact to high temperature durability reported in [10].

A fourth key philosophy is achieved manufacturability critical to technology adoption and infusion. With modest adjustments, the NASA Glenn 500 °C durable SiC JFET-R fabrication process is compatible with semiconductor mass-production tools. Insulator deposition is carried out using standard LPCVD tube furnace hardware with some non-standard procedures. All materials used in the BEOL

processing are compatible with most silicon IC manufactures except for the bond pad metals of iridium, gold, and platinum, which would require separate equipment and accommodations. Advantageously, the bond pad metal and corresponding via-3 features are large simple features and could even be done in a separate facility with a contact aligner.

Further processing optimizations are actively being investigated. One primary focus/challenge of on-going improvement is to retire dielectric cracking as the predominant high-T failure mechanism [1,3,10] while preserving $Si_3N_4$ as an impediment to deleterious oxygen and sodium penetration. A second major focus is to shrink all layout feature sizes in order to substantially upscale chip complexity. Towards this end, stepper-based lithography is planned to supplant contact-aligner based lithography in future SiC JFET-R IC runs [11].

The BEOL described here might also be adapted for use with other transistor approaches including planar implanted SiC JFETs or SiC bipolar junction transistors. However, heteroepitaxial transistor technologies (e.g., III-N heterojunction FETs) will face additional obstacles to 500 °C durability including higher CTE mismatch stress and higher reactivity/diffusivity than inherent to the SiC homoepilayer approach.

## Conclusion

This paper has summarized important processing and materials aspects of achieving prolonged SiC JFET-R ICs capable of more than a year of 500 °C operation. With modest investment in modified equipment and materials, this technology is portable to commercial foundry manufacturing. Such new capability promises to unlock extreme-temperature IC benefits to a variety of important aerospace, automotive, and deep-well drilling applications.

## Acknowledgements

This work was conducted by The NASA John H. Glenn Research Center in Cleveland, OH USA with funding from the NASA Science Mission Directorate under the High Operating Temperature Technology (HOTTech) and Long-Lived In-Situ Solar System Explorer (LLISSE) projects. The authors are grateful to G. Hunter, G. Beheim, M. Krasowski, C. Chang, N. Prokop, L. Greer, D. Lukco, A. Avishai, K. Moses, J. Gonzalez, M. Mrdenovich, J. Flatico, R. Okojie, S. Rajgopal, R. Buttler, A. Miller, F. Lam, D. Spina, A. Izadnegahdar, S. Booth, D. Centeno-Gomez, C. Tolbert, Q. Nguyen, and T. Kremic for their support.

## References

[1] P. Neudeck, et al., *Proc. 2018 IMAPS Int. Conf. High Temperature Electronics*, pp. 71-78. https://ntrs.nasa.gov/citations/20180003391

[2] Wolfspeed, a Cree company, https://www.wolfspeed.com

[3] D. Spry, et al., *Proc. 2016 IMAPS Int. Conf. High Temperature Electronics*, pp. 249-256. https://ntrs.nasa.gov/citations/20160014879

[4] D. Spry et al., *Materials Science Forum*, vol. 828, pp. 1112-1116 (2016). https://ntrs.nasa.gov/citations/20160005309

[5] GE Research, Niskayuna, NY USA, as a subrecipient under OASIS Contract GS00Q140ADU106; Pool 1

[6] D. Spry and D. Lukco, *J. Electronic Materials*, vol. 41, p. 915-920 (2012). https://doi.org/10.1007/s11664-011-1792-9

[7] L. Chen, et al., *Proc. 2016 IMAPS Int. Conf. High Temperature Electronics*, pp. 66-72. https://ntrs.nasa.gov/citations/20160014867

[8] D. Spry and P. Neudeck, U.S. Patent 9,978,686 (2018).

[9] D. Spry et al., U.S. Patent 10,256,202 (2019).

[10] D. Spry, et al., *Materials Science Forum*, vol. 1004, pp. 1148-1155 (2020) 10.4028/www.scientific.net/MSF.1004.1148

[11] P. Neudeck et al., this conference

## Acronyms

BEOL: Back End Of Line
CTE: Coefficient of Thermal Expansion
CVD: Chemical Vapor Deposition
FEOL: Front End Of Line
FESEM: Field Emission Scanning Electron Microscope
FET: Field Effect Transistor
FIB: Focused Ion Beam
FMG: Forming Gas
HIPIMS: High-Power Impulse Magnetron Sputtering
IC: Integrated Circuit
IrIS: Iridium Interfacial Stack
JFET: Junction Field Effect Transistor
JFET-R: Junction Field Effect Transistor & Resistor
LPCVD: Low Pressure Chemical Vapor Deposition
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
NASA: National Aeronautics and Space Administration
SiC: Silicon Carbide
T: Temperature
TEOS: TetraEthyl OrthoSilicate

# Monolithically Integrated GaN Power and RF ICs on 150mm Poly-AlN for Envelope Tracking Power Amplifier Applications

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***Index Terms*——Back barrier (B/B) layer, high thermal conductivity, QST substrate.**

**Abstract**

**This is the first comprehensive study on monolithically integrated GaN power and radio frequency (RF) integrated circuits (ICs) on GaN-on-poly-AlN (QST™) substrates. GaN power and RF ICs integration was feasible due to the reduced parasitics, thermally matched substrate of poly-AlN, high thermal conductivity, high mechanical strength, as well as the optimized GaN layer structure designs. The E/D-mode GaN low-voltage logic device and E-mode power device were realized to implement the soft-switching buck-converter. A 0.25-µm gate length T-shaped gate GaN RF high-electron-mobility transistor was adopted for the high-output power stage. Monolithically integrated GaN power and RF ICs on QST substrates results in a feasible single envelope-tracking power-amplifier chip with high thermal stability.**

## I. Introduction

GaN is widely used in high-frequency and high-power devices. Sapphire and Si are commonly used as substrate materials for GaN. However, the low thermal conductivity those substrate materials limits the heat dissipation in device-level self-heating and may reduce the reliability and longevity of a device. Thus, for many applications, replacement substrates such as SiC or GaN are used to improve device performance; however, the high cost of these two substrates remains problematic.

The poly-AlN substrate has been proven to be a promising technology for GaN power integrated circuits (ICs) due to its high thermal dissipation efficiency and high mechanical strength. However, the combination of GaN with silicon-on-insulator technology for radio frequency (RF) applications was demonstrated recently, and the combination is similar to the combination of GaN with Qromis substrate technology (QST) substrates. The QST substrate consists of a polycrystalline ceramic core (poly-AlN) that is covered by several encapsulation layers on top of which is a $SiO_2$ bonding layer and a single crystalline Si layer, which serves as the nucleation layer for the growth of metal organic chemical vapor deposition (MOCVD) [1]. By using a back-barrier design and Fe[2-3] + C[4-5] buffer doping optimization, we demonstrated that RF GaN on QST for an RF power amplifier has high thermal stability and the output power efficiency and linearity are maintained at high-voltage operation. Based on delay-time analysis, the QST performance at a stable bandwidth was associated with negligible parasitic channel delay between the GaN/Si interfaces. Thus, an all-GaN envelope-tracking power amplifier with buck-converter seems implementable.

## II. Experimental Procedures

The AlGaN/GaN RF high-electron-mobility transistor (HEMT) structure was grown using MOCVD on QST and Si substrates. The epitaxial layers were composed of a thin AlN nucleation layer and an Fe-doped/C-doped GaN buffer layer. A 50-nm $Al_{0.05}Ga_{0.95}N$ back barrier was grown, followed by a 300-nm GaN channel layer. A 0.5-nm-thick AlN spacer layer and a 20-nm-thick $Al_{0.24}Ga_{0.86}N$ barrier layer were deposited. Finally, to reduce AlGaN barrier layer surface oxidation and leakage current, a 2-nm GaN cap layer was deposited through MOCVD. The HEMTs with high thermal dissipation efficiency and high mechanical strength were fabricated on a poly-AlN substrate, as illustrated in Fig. 1.

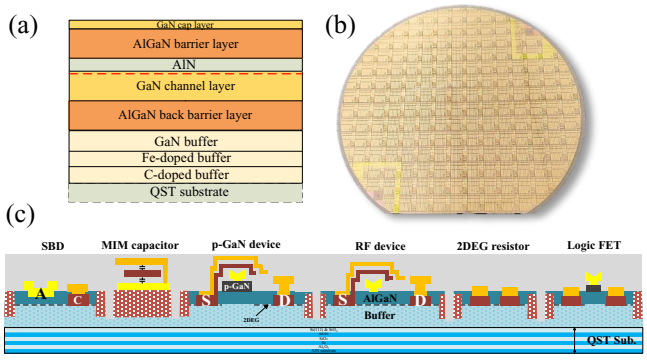


Fig. 1. (a) Structure, (b) photograph, and (c) schematic process cross-sections of the GaN IC on the GaN-on-QST substrate.

Fig. 2(a) presents the schematic cross-sections of devices. Transmission electron microscopy (TEM) image cross-sections of GaN on a QST substrate and of the gate RF HEMT are illustrated in Fig. 2(b) and (c), respectively. The RF HEMTs had a gate length ($L_G$) of 0.25 µm, a gate width ($W_G$) of 50 µm, a gate-source distance ($L_{GS}$) of 0.75 µm, and a gate-drain distance ($L_{GD}$) of 2.25 µm.

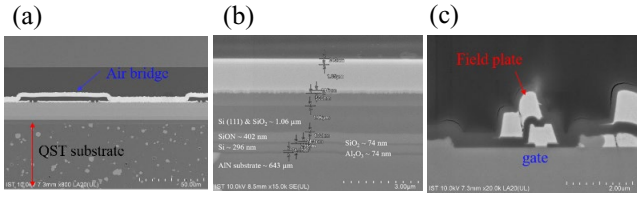


Fig. 2. TEM images of the (a) device cross-section, (b) QST substrate contact, and (c) detailed gate module.

## III. Results and Discussion

To study the effect of a poly-AlN substrate on the performance of the device, we measured the $I_{DS}$–$V_{GS}$, $I_{DS}$–$V_{DS}$, and $I_{GS}$–$V_{GS}$ characteristics of the devices by using Agilent 4142B, as illustrated in Fig. 3. The drain-to-source current ($I_{DS}$) and output transconductance ($g_m$) versus gate-to-source voltage ($V_{GS}$) at $V_{DS}$ was 10 V, with a $V_{GS}$ sweep from −5 to 2 V. The saturation currents of GaN on Si and GaN on QST were 1067 and 906 mA/mm at $V_{GS}$ = 2 V and $V_{DS}$ = 10 V, respectively. As illustrated in Fig. 3 (b), the Si device also had the best $I_{on}/I_{off}$ ratio and subthreshold swing (*S.S.*), which were $1.2 \times 10^5$ and 0.131 V/dec, respectively. The $I_{on}/I_{off}$ ratio and *S.S.* of the QST device were $2.4 \times 10^4$ and 0.341 V/dec, respectively. Fig. 3(c) depicts a comparison of the two devices' the on-resistance ($R_{on}$) values were 3.14 ©·mm ($R_{on_Si}$) and 3.06 ©·mm ($R_{on_QST}$).

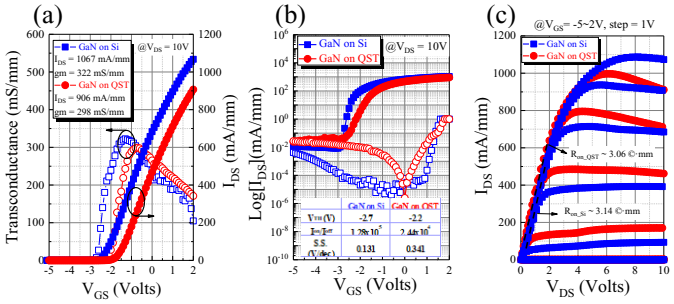


Fig. 3. (a) Transfer characteristics ($I_{DS}$–$V_{GS}$) at $V_{DS}$ = 10 V with a $V_{GS}$ sweep from −5 to 2 V. (b) Curve of the drain (log-scale $I_{DS}$–$V_{GS}$) and gate ($I_{GS}$–$V_{GS}$) of the off-state leakage current. (c) $I_{DS}$–$V_{DS}$ output current at a $V_{GS}$ sweep from −5 to 2 V with a step of 1 V.

To investigate the large-signal linearity performance of the device under high-frequency operation, we conducted two-tone intermodulation distortion measurements, as illustrated in Fig. 4. The operating fundamental frequency was 3.5 GHz, and the tone spacing was 20 MHz at a $V_{DS}$ of 28 V. The output third-order intercept point (OIP3) of GaN on QST and GaN on Si was 28.42 dBm and 27.92 dBm, respectively. A higher OIP3 was registered in the HEMT with GaN on a QST substrate than the HEMT with GaN on the Si substrate. However, the transconductance linearity contributed to the superior two-tone linearity performance of the HEMT with GaN on a QST substrate [6]. Because of its high thermal conductivity and high linearity, a GaN on QST substrate is highly suitable for emerging fifth-generation (5G) applications.

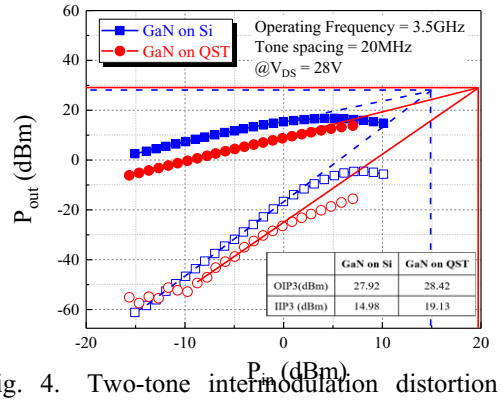


Fig. 4. Two-tone intermodulation distortion linearity measurements with an operating frequency of 3.5 GHz and tone spacing of 20 MHz at a $V_{DS}$ of 28 V.

Temperature is a crucial consideration for device reliability. We measured the surface temperature distribution in both devices. The surface temperature map values in Fig. 5(a) and (b) were obtained from the IR radiation intensity, and they determined the emissivity calibration that was performed for the QST and Si substrate devices within 300 s at a current of 500 mA/mm. As illustrated in Fig. 5(a) and (b), the surface peak temperatures of the Si device ranged from 34.1 °C to 59.8 °C and those of the QST device were from 34.5 °C to 52.1 °C. The results revealed that the QST substrate was less affected by self-heating than the Si device was. Because the thermal conductivity of the GaN on the QST device was higher than that of the Si device, its heat dissipation performance was better than that of the GaN on Si device, with the device operating at an $I_{DS}$ of 500 mA/mm and $V_{DS}$ of 10 V, as illustrated in Fig. 5(c).

To explore the influence of ambient temperature on device characteristics, we performed variable temperature measurements on the two devices. Fig. 5(d) shows an $I_{DS}$–$V_{DS}$ characteristic measured from 300 K to 375 K with a 25 K step. The maximum saturation current at 300 K and 375 K of the Si device was 592 mA/mm and 505 mA/mm, respectively, at a $V_{DS}$ of 20 V. The current of the device was affected by external temperature and dropped close to 15%. The current of the QST device was 441 mA/mm and 391 mA/mm at a $V_{DS}$ of 20 V and dropped close to 12%. The $I_{DS}$ degradation of GaN on QST was smaller than of GaN on Si, at 3.1% when the device was operated in a high-temperature environment (375 K). The results in Fig. 5 indicate that the QST substrate

can be used at relatively high temperatures due to its superior thermal conductivity.

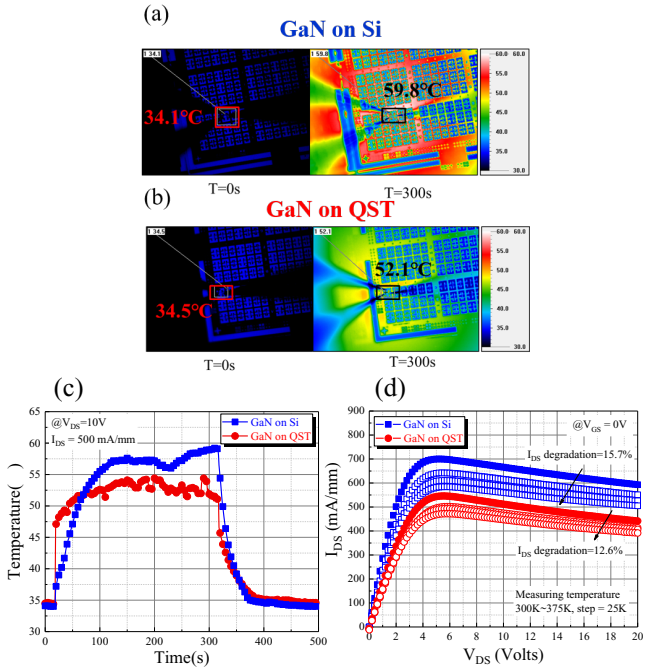


Fig. 5. Analysis of thermal image measurement of (a) GaN on Si and (b) GaN on QST. (c) Analysis of thermal behavior at an $I_{DS}$ of 500 mA/mm, and the (d) different $I_{DS}$–$V_{DS}$ characteristics at various temperatures.

Fig. 6. presents the small-signal measurements of the QST and Si devices conducted using an Agilent network analyzer. The measurement method involved increasing temperature from room temperature (300 K) to 375 K with a step of 25 K. Fig. 6 displays the maximum current gain ($f_T$) and maximum power gain ($f_{max}$) of the Si device at 300 K and 375 K ($f_T/f_{max}$ = 26/54 GHz and $f_T/f_{max}$ = 19.2/37.6 GHz, respectively). The S-parameter changed 1.35/1.43 times under the influence of temperature, with the frequency of the device declining by 6.8/16.4 GHz. The QST device had the following values: $f_T/f_{max}$ = 17.8/39 GHz and $f_T/f_{max}$ = 13.6/29.6 GHz. The S-parameter changed 1.30/1.31 times under the influence of temperature, and the frequency of the device declining by 4.2/9.4 GHz.

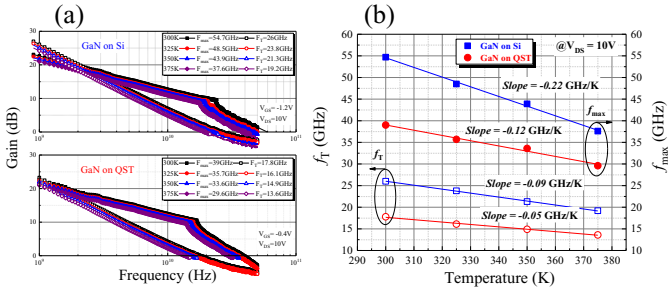


Fig. 6. Small-signal characteristics at different temperatures in GaN on Si and GaN on QST devices. (a) Frequency (Hz). (b) Temperature (K).

Fig. 7(a) and (b) display the transfer ($I_{DS}$–$V_{GS}$) and output characteristics ($I_{DS}$–$V_{DS}$) of the E-mode p-GaN power HEMT. As presented in Fig. 7(a), the $V_{TH}$ and the off-state drain current value were 1.2 V and 4.15E-8 mA/mm, respectively. The device also obtained an improved $I_{on}/I_{off}$ ratio and lower *S.S.*, which were 1.1 × $10^{10}$ and 0.075 V/dec, respectively. Next, Fig. 7(b) indicates that the maximum output current density $I_{max}$ was 451 mA/mm at a gate bias of 6 V, and the lower on-resistance $R_{on}$ was 4.6 ©·mm for the E-mode p-GaN power HEMT. Additionally, the thermal stability was measured from room temperature (25 °C) to 225 °C, with 50 °C steps, as displayed in Fig. 8(a) and (b). The E-mode p-GaN power HEMT that was grown on a QST substrate exhibited good thermal behavior due to the high thermal conductivity of the QST substrate. Fig. 8(a) displays the transfer characteristics at different temperatures; the off-state leakage current and saturation current were less varied. The $V_{TH}$ performance shift was investigated; as displayed in Fig. 8(b), the $V_{TH}$ of the device shifted less than 0.03 V even up to a temperature of 225 °C, which demonstrates this device's superior $V_{TH}$ stability.

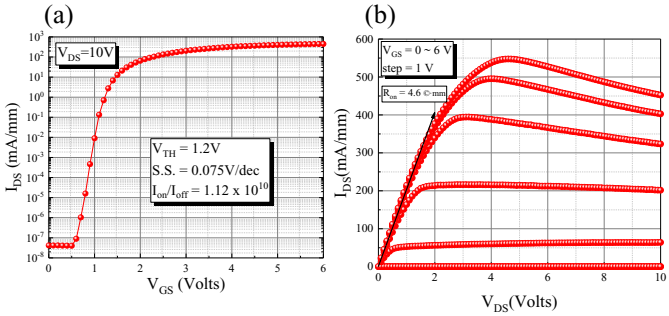


Fig. 7. (a) Transfer and (b) output characteristics of the p-GaN gate power HEMT on the QST substrate. The device exhibited a low $R_{on}$ of 4.6 ©·mm, a $V_{TH}$ of 1.2 V, a low off-state leakage of <$10^{-7}$ mA/mm, and a high $I_{on}/I_{off}$ ratio of 1.1 × $10^{10}$.

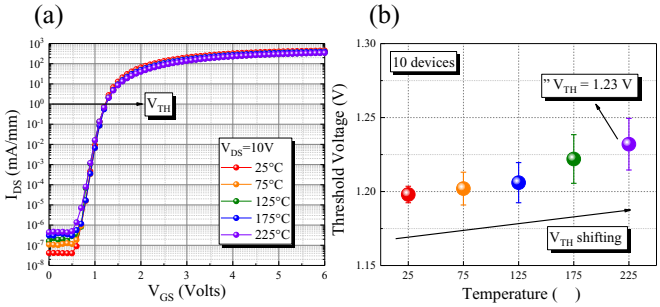


Fig. 8. (a) Transfer and (b) $V_{TH}$ of the p-GaN gate power HEMT on the QST substrate at different temperatures. The device exhibited high thermal stability and a low $V_{TH}$ shift of 0.03 V at 225 °C.

The off-state breakdown voltage and pulse measurement were measured and are depicted in Fig. 9(a) and (b). The device exhibited a high off-state breakdown of 694 V at $V_{GS}$ = 0 V. To analyze the trapping and detrapping effect, the

dynamic $R_{on}$ ratio of the E-mode p-GaN power HEMT was measured using a pulse width of 2 µs and a period of 200 µs. In this work, establishing the following bias conditions was necessary: pulse voltage ($V_{GS}$, $V_{DS}$) and quiescent voltage ($V_{GSQ}$, $V_{DSQ}$). The $V_{DSQ}$ for the device was swept from 0 to 650 V with increments of 50 V. Clearly, the device exhibited a superior dynamic $R_{on}$ ratio, which was 1.25 times at $V_{DSQ}$ = 650 V.

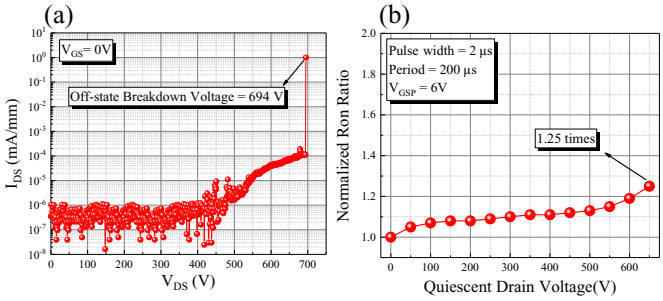


Fig. 9. (a) Off-state breakdown voltage and (b) dynamic $R_{on}$ characteristic of the p-GaN gate power HEMT on the QST substrate. The device exhibited a high off-state breakdown voltage of 694 V and a low dynamic $R_{on}$ ratio of 1.25 times at $V_{DSQ}$ = 600 V.

Fig. 10. presents $V_{in}$–$V_{out}$ transfer characteristics and the switching waveform of the GaN inverter. The inverter was measured at a $V_{DD}$ bias of 5 V and switch from $V_{out}$ = 5 V to 0 V.

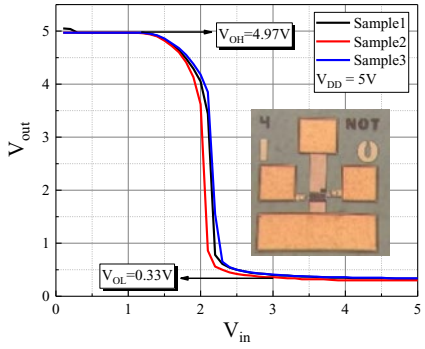


Fig. 10. Characteristics of NOT for three samples.

The inverter had good switching performance when the $V_{OH}$ and $V_{OL}$ were 4.97 V and 0.33 V, respectively, as displayed in Fig. 10. Additionally, the inverter measured the switching waveforms at 100 kHz, 200 kHz, 300 kHz, 400 kHz, and 500 kHz, respectively, as displayed in Fig. 11. The inverter operated at 100 kHz, which maintained the complete square wave. However, the inverter also had less distortion at 500 kHz, which clearly demonstrated the functionality of this circuit.

## IV. Conclusions

The GaN on QST structure can effectively improve the heat dissipation characteristics of a device and reduce the influence of the high temperature generated by the device during operation or in outdoor ambient temperatures. This study applied the GaN on QST structure to high-frequency, high-power, and logic device applications. Effective heat dissipation characteristics make engineered substrates a promising RF platform for 5G micro- or macro-cell base stations.

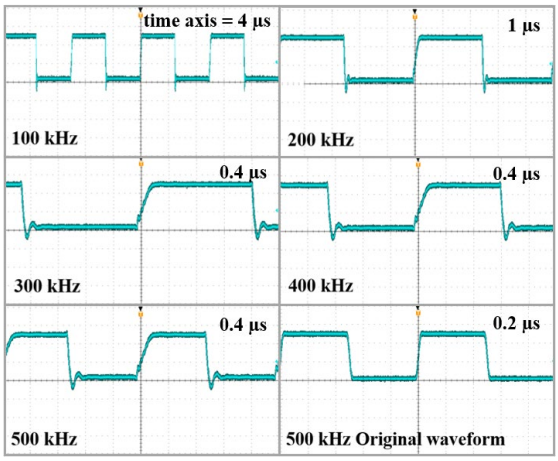


Fig. 11. Switching waveforms at 100 kHz to 500 kHz with a step of 100 kHz.

## References


[1] X. Li, "GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion", IEEE IEDM, 978-1-7281-4032-2, 2019.

[2] Y. Komatsuzaki, "A High Efficiency 3.6-4.0 GHz Envelope-Tracking Power Amplifier Using GaN Soft-Switching Buck-Converter", IEEE/MTT-S International Microwave Symposium, 978-1-5386-5067-7, 2018.

[3] H. Chiu, S. Chen, "AlGaN/GaN Schottky barrier diodes on silicon substrates with various Fe doping concentrations in the buffer layers," Microelectronics Reliability, vol. 83, 2018, pp. 238-241.

[4] J. H. Lee, "High Figure-of-Merit ($V^2_{BR}/R_{ON}$) AlGaN/GaN Power HEMT With Periodically C-Doped GaN Buffer and AlGaN Back Barrier," Journal of the Electron Devices Society, Vol. 6, 2018, pp. 1179-1186.

[5] S. Kumar, P. Gupta, I. Guiney, C. J. Humphreys, S. Raghavan, R. Muralidharan, and D. N. Nath, "Temperature and Bias Dependent Trap Capture Cross Section in AlGaN/GaN HEMT on 6-in Silicon with Carbon-Doped Buffer," IEEE Transactions on Electron devices, Vol. 64, No. 12, December 2017.

[6] S. H. Sohel, A. Xie, E. Beam, H. Xue, J. A. Roussos, T. Razzak, S. Bajaj, Y. Cao, D. J. Meyer, W. Lu, and S. Rajan, "X-Band Power and Linearity Performance of Compositionally Graded AlGaN Channel Transistors," IEEE Electron Device Letters, Vol. 39, No. 12, December 2018.

# SESSION 5:
# DEVICES 1: GAN

# Performance of 0.3 um gate length GaN HEMT by using i-line stepper for high power c-band applications

Sangmin Lee, Byoungchul Jun, Chulsoon Choi, Hyeyoung Jung, Seokgyu Choi, Min Han, Hogeun Lee, Myoungkeun Song, Jihun Kwon, Myungsoo Park, Sungwon Lee, Yongjae Kim, Sewon Hwang, Hangyol Ji, Inseop Kim, Jinman Jin, Kyeongjae Lee and Jun-Hyeok Lee

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**Keywords: GaN, HEMT, i-line stepper, c-band, RF, power amplifier**

**Abstract**

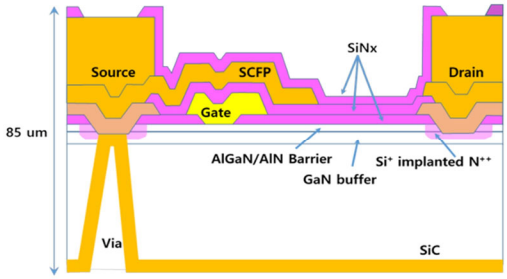
**GaN HEMT devices with 0.3 um gate length has been developed with i-line stepper based process. Device fabrication process includes Si+ ion implant ohmic, Ni based gamma gate, Au electro-plated source connected field plate, through hole SiC via directly connected to the source ohmic. The current gain cut off frequency was measured about 21 GHz and the power density about 8.5 W/mm at 3.5 GHz. Angelov GaN HEMT large signal model has been developed and available in ADS software. A wideband PA at 5.1 – 5.8 GHz has been designed and fabricated with 2 of 350umx20 finger devices. The PA shows 13~15 dB small signal gain, 10~12 dB power gain, >49 dBm peak power, >42% drain efficiency. The measured performance of the PA was well matched to the simulation.**

## INTRODUCTION

Traditionally, c-band frequency range has a number of applications such as satellite communications, satellite TV networks, weather satellite, 802.11a wifi, radio LAN services, data link for UAVs and wideband jammer etc. [1, 2, 3, 4] As 5G mobile service has been deployed in 2020 globally mostly in sub-6 GHz frequency range, the demand of high power, high efficiency, high gain power amplifiers with affordable price in c-band has never been higher before. Though GaN HEMT technology is the most promising solution for this demand, actual devices meet all those requirements are scarcely found in the RF PA market. The devices developed for s-band applications using 0.4 um or 0.5 um gate length shows high power at affordable price but once the frequency is raised to c-band, it suffers low gain and efficiency. On the contrary, 0.25 um gate length devices, developed for x-band, shows excellent gain and efficiency at c-band but the maximum power of a single device is limited, and the manufacturing cost is very high. 0.3 um gate length devices with similar power performance to 0.4 um gate fabricated with a mass producible photo lithography such as i-line stepper seems to be an obvious solution for high power c-band applications. 0.3 um gate was defined by i-line stepper with high resolution photo resist on top of SiNx dielectric layer. The rest of the device structures were similar to the high-power devices with 0.4 um gate process to maintain the power performance.[5]

## RESULTS AND DISCUSSIONS

1) Device design and fabrication process: The epi structure, device design and fabrication process are same as Wavice baseline process of 0.4 um gate technology published elsewhere [5], except the gate length. 0.3 um gate length was achieved using i-line stepper and subsequent pattern treatment and ICP etching of SiNx dielectric layer. Fig 1 shows schematic diagram and SEM picture of the cross section of the device.

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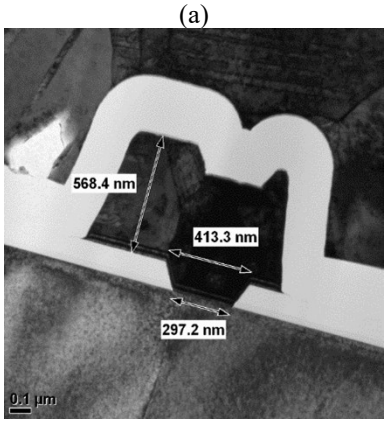


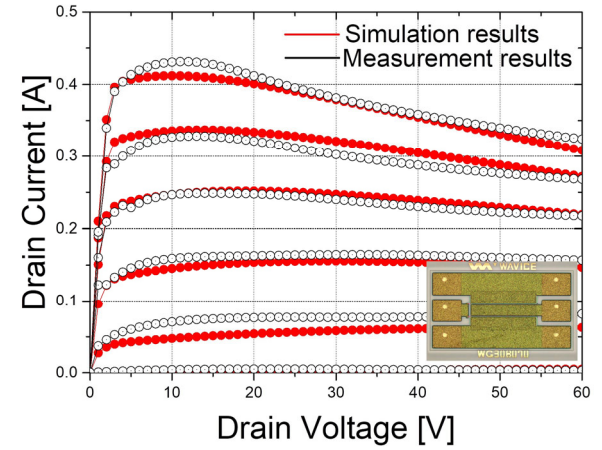

(b)

Fig. 1. (a) a schematic diagram and (b) a SEM cross-section picture of 0.3 um gate length GaN HEMT device

2) Device performance and large signal model: Table 1 shows key DC performance of 0.7 mm gate periphery devices. The ft and fmax were measured as 21 and 39 GHz respectively.

TABLE I
DC performance of 0.3 um gate length devices with 0.7 mm gate periphery.

| Parameter | Test Condition | Unit | Mean |
|---|---|---|---|
| Gm_max | Vd=10V, maximum gm | S/mm | 0.32 |
| Id_Max | Vd=10V, Vg=2V | A/mm | 0.98 |
| Ig10_n8 | Vd=10V, Vg=-8V | uA/mm | 11 |
| Id10_n8 | Vd=10V, Vg=-8V | uA/mm | 12 |
| Vth | Vd=10V, Id=1mA/mm | V | -2.3 |

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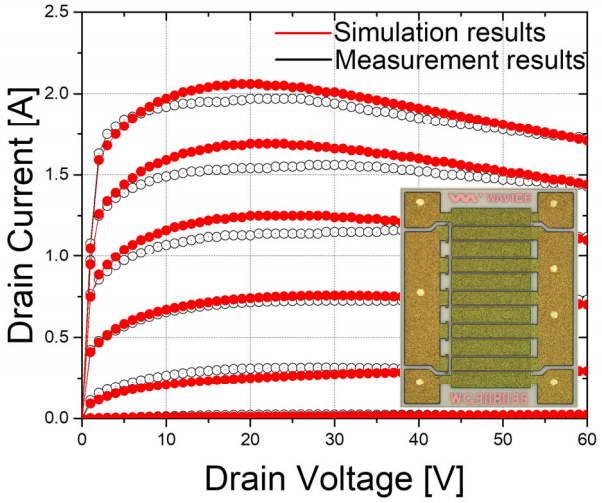
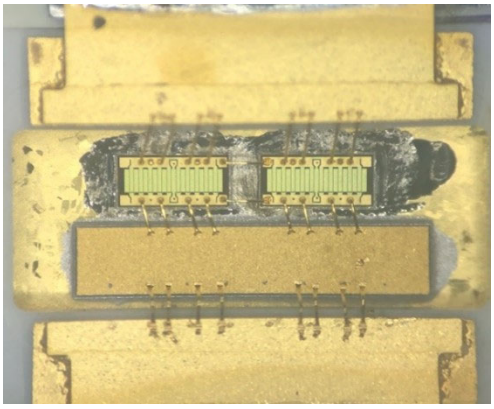



(b)

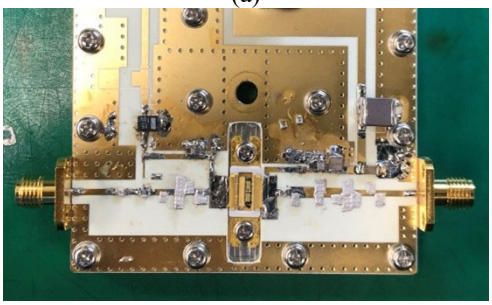
Fig. 2. DC IV characteristics of (a) 0.7 mm and (b) 3.5 mm gate periphery devices. Optical microscope pictures of actual devices are enclosed in the graph.

The DC IV characteristics of 0.7 mm and 3.5 mm gate periphery devices are shown in figure 2. ADS simulated IV curves from Angelov GaN large signal models are well matching to the measured data.

3) Wideband PA: Using the device model described above, a wideband power amplifier has been designed and fabricated. Figure 3 shows the picture of packaged transistor and the evaluation board. 2 of 7 mm gate periphery devices and 6.47 pF SLC were used in a package. GaN HEMT devices were AuSn eutectic bonded and the 2 mil Au wires were ball bonded to the devices. Fig. 3 shows the picture of packaged device and the evaluation board.



(a)



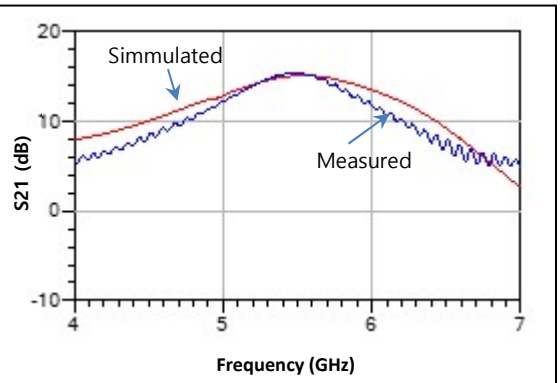
(b)

Fig. 3. Optical microscope picture of (a) a packaged transistor showing 2 of 7 mm gate periphery devices and a SLC and (b) an evaluation board with the packaged transistor

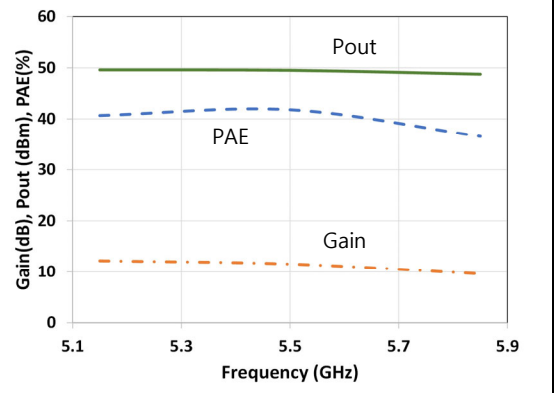
Figure 4 shows small signal gain and the power performance of the PA. The computer simulated and measured S21 gain show 13~15 dB and well match each other for 5.1 – 5.8 GHz. Peak power was measured as 49.6 dBm at 5.5 GHz and the PAE 44.6%. For the frequency range, the output power was >49 dBm, PAE >42% and gain >10 dB.

Figure 5 shows previous works for 1 stage power amplifiers in C-band (4-8 GHz). [6-15] The PA reported in this work shows the 2nd highest power gain.

The highest gain in C-band was reported by Ma et. al., 13.5 dB using 0.25 um gate length and 100 um unit gate width 24 mm total gate periphery. (2 devices with 120 gate fingers) [7] In this report, however, 350 um unit gate width devices were used and thus the total number of gate fingers is only 40. With this technology, it seems probable to realize higher power amplifiers(>300W) with high power gain(>12dB) in a compact footprint.




(a)




(b)

Fig. 4. (a) Small signal gain (S21) by measurement and simulation (b) peak output power (Pout), PAE and power gain as a function of frequency

## CONCLUSIONS

GaN HEMT devices with 0.3 um gate length have been successfully developed by using i-line stepper photo lithography process. The ft of 21 GHz and power density of 8.5 W/mm have been measured. Angelov GaN large signal model has been made and is available in ADS. The wideband PA designed by this model shows high power and high gain performance at 5.1-5.8 GHz. Currently a list of reliability test is in progress and higher power devices have been in development to improve the power and efficiency performance with this technology.

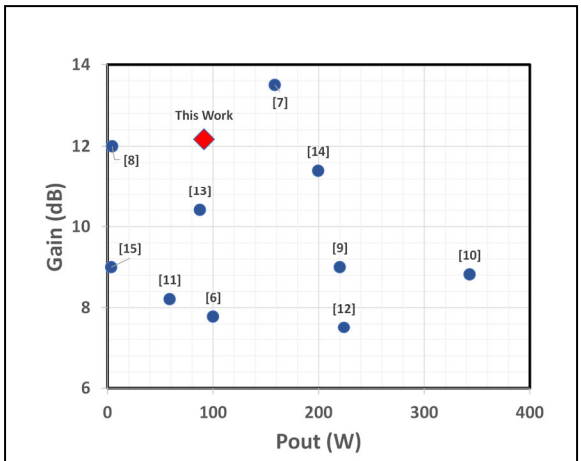



Fig. 5. Previously reported 1 stage PA performances in C-band

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] M. van Heijningen *et al.*, *C-Band Single-Chip Radar Front-End in AlGaN/GaN Technology,* IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 11, pp. 4428-4437, 2017.

[2] Ishida Takao, *GAN HEMT TECHNOLOGIES FOR SPACE AND RADIO APPLICATIONS*, Microwave Journal 54, 8, pp. 56-66, 2011.

[3] Mohamed Fazal, et al., *Design of Secured, High Speed Two Way RF Data Link for Airborne Vehicle Communication*, Microwave Symposium Digest 20013 IEEE MTT-S International Microwave and RF Conference, New Delhi, India, , pp. 1-4, 2013.

[4] Patrick Hindle, *Future RF Market Opportunities for GaN*, Microwave Journal, 55, 6, pp22-42, 2012.

[5] S. Lee, et al., *Qualification of Wavice Baseline GaN HEMT process with 0.4 um gate on 4" SiC wafers*, CS MANTECH Technical Digest,m pp179-182, 2020.

[6] H. Otsuka et. al., *Over 57% Efficiency C-band GaN HEMT High Power Amplifier with Internal Harmonic Manipulation Circuits*, Microwave Symposium Digest 2008 IEEE MTTS International, pp 311-314, 2008.

[7] X. Ma et. al., *A C-Band Internally-Matched High Efficiency GaN Power Amplifier*, CHIN. PHYS. LETT. Vol. 31, No. 10 (2014), pp 108401-1 – 108401-4, 2014.

[8] Rocco Giofre et. al., *A GaN on SiC process with high power density and efficiency*, Proceedings of European Microwave Integrated Circuits Conference (EuMIC), pp 180-183, 2013.

[9] K. Yamanaka et. al., *C-band GaN HEMT Power Amplifier with 220W Output Power*, Microwave Symposium Digest

2007 IEEE MTT-S International, pp 1251-1254, 2007.
[10] H. Shigematsu et. al., *C-band 340-W and X-band 100-W GaN Power Amplifiers with Over 50-% PAE*, Microwave Symposium Digest 2009 IEEE MTTS International, pp 1265-1268, 2009.
[11] K. Iyomasa et. al., *GaN HEMT 60W Output Power Amplifier with Over 50% Efficiency at C-Band 15% Relative Bandwidth Using Combined Short and Open Circuited Stubs*, Microwave Symposium Digest 2007 IEEE MTTS International, pp 1255-1258, 2007.
[12] H. Maehara at. al., *Internally Matched GaN FET at C-band with 220W Output Power and 56% Power Added Efficiency*, Proceedings of Microwave Conference (APMC) 2012 Asia-Pacific, pp 358-360, 2012.
[13] T. Yamasaki et. al., *A 68% Efficiency, C-Band lOOW GaN Power Amplifier for Space Applications*, Microwave Symposium Digest 2010 IEEE MTTS International, pp 1384-1387, 2010.
[14] Cree (Anonymous), *C-Band GaN HEMT Delivers 200 W CW, Microwave Journal*, 58, 1, pp 132-134, 2015.
[15] Felix Rautschke et. al., *Octave bandwidth S- and C-band GaN-HEMT power amplifiers for future 5G communication*, International Journal of Microwave and Wireless Technologies, 10, pp737–743, 2018.

## ACRONYMS

ADS: Advanced Design System (®Keysight)
LAN: Local Area Network
UAV: Unmanned Aerial Vehicle
ICP: Inductively Couple Plasma
SEM: Scanning Electron Microscopy
HEMT: High Electron Mobility Transistor
PA: Power Amplifier
PAE: Power Added Efficiency
SLC: Single Layer Capacitor

# Investigation of Un-doped GaN Cap Layer on RF and Trap Related Characteristics in AlGaN/GaN HEMTs

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**Keywords: GaN, HEMT, GaN cap, interface, trap, C-V, pulsed I-V**

**Abstract**

**In this work, the influence of un-doped GaN cap layer on AlGaN/GaN high electron mobility transistors (HEMTs) has been studied by using DC, pulsed I-V, capacitance-voltage (C-V), and load-pull characterizations. The device without cap layer is found to exhibit smaller dynamic range ($V_{on}$-$V_{th}$) compared to that of the device with cap layer. However, the lower interface trap density in the device without cap layer can lead to higher drain current with different quiescent points, resulting in better RF power and gain at 2.7 GHz.**

## INTRODUCTION

GaN-based high electron mobility transistor (HEMT) is promising for high power and high frequency device applications, owing to its wide bandgap, high saturation electron velocity and low on-resistance. However, GaN-based devices suffer from the existence of traps at passivation/III-V interface, leading to threshold voltage instability [1] and current collapse [2]. Recently, many methods have been reported to improve the interface property, by using different passivation materials and deposition techniques, such as $Al_2O_3$ grown by atomic layer deposition (ALD) [3], SiN deposited by plasma enhanced chemical vapor deposition (PECVD) [4], SiN deposited by low pressure chemical vapor deposition (LPCVD) [5], and nitridation interlayer prior to gate dielectric [6].

In the early stage of GaN HEMT development history, it is believed that GaN cap is helpful to protect the surface and suppress the surface traps [7-9], which could also be caused by immature pre-treatment and improper passivation process. In order to suppress the high electrical field induced defect and inverse piezoelectric effect, GaN cap layer has been widely used in GaN HEMTs [10-11]. However, because of the high voltage operation, the electrically degraded devices always contain the pit-like defects at the gate edge side, which degrade the $I_{dmax}$ [12-13]. The negative polarization charges at the interface of the GaN cap layer and the AlGaN layer cause the increase of the barrier height [14], reducing the gate leakage current and increasing the Schottky turn on voltage. However, the negative polarization charges also suppress the carrier density of the 2-dimensional electron gas (2DEG) and result in an increase of the sheet resistance [15]. The insertion of the GaN cap layer also increase the distance between the gate electrode and the 2DEG channel, hence inevitably compromising the gate controllability.

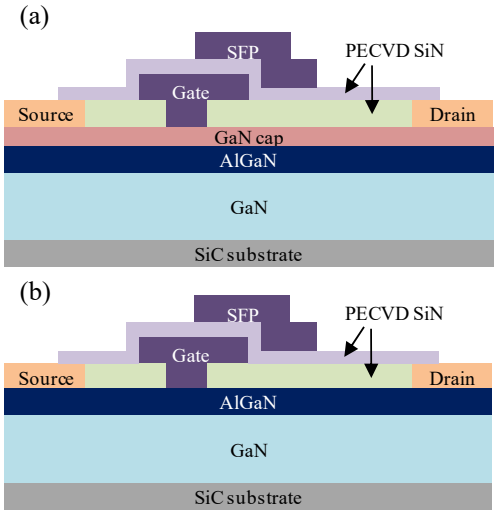


Fig. 1. Schematic of the 0.4-um AlGaN/GaN HEMTs with (a) and without (b) GaN cap layer.

In this paper, we apply C-V measurement, DC, pulsed IV, and RF techniques to investigate the trapping behaviors and the influence of un-doped GaN cap on AlGaN/GaN HEMTs.

## EXPERIMENTAL

The structure of the AlGaN/GaN HEMT in this work is shown in Fig. 1. AlGaN/GaN heterostructure with and without 3-nm GaN cap layer are grown on 4-inch SiC substrate by metal organic chemical vapor deposition (MOCVD). Ohmic metal were formed by electron beam evaporation of Ti/Al/Ti/Au metal stacks, followed by rapid thermal annealing at 855°C for 30 s in N2 ambience. A SiN layer of 80 nm thickness was deposited by PECVD as a first passivation layer. ICP etch was applied for gate opening. Schottky contact was formed by evaporated Ni/Pd/Au . A second SiN layer of 200 nm thickness was deposited by PECVD as interlayer of gate metal and source field plate (SFP).

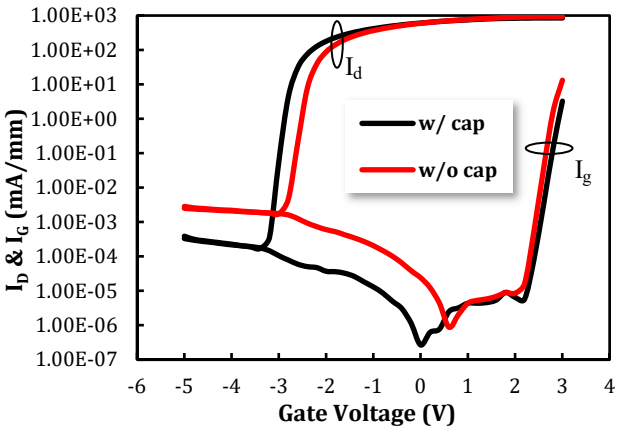


Fig. 2. Transfer characteristics of the AlGaN/GaN HEMTs with and without GaN cap.

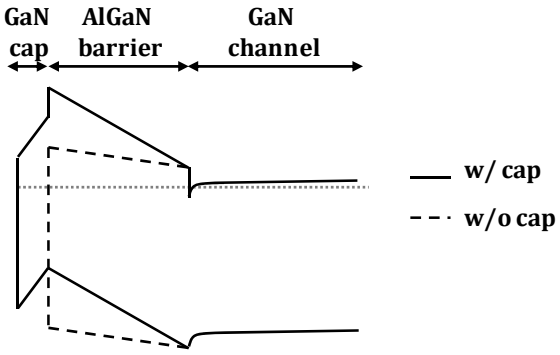


Fig. 3. Schematic illustration of energy-band diagram for AlGaN/GaN HEMTs with GaN cap layer and without GaN cap layer.

## Device Characteristics and Performance

Fig. 2 shows the CW $I_d$-$V_g$ transfer characteristics of the devices with and without GaN cap layer. The device with cap layer shows a level of leakage nearly one order of magnitude lower than that of the device without cap layer. This can be attributed to the barrier height increase caused by the insertion of the GaN cap layer, as illustrated in Fig. 3. The increase of the barrier height also leads to an increase (≈ 0.2 V) of the gate turn-on voltage ($V_{on}$). Because of the existence of the GaN cap layer, the distance between the gate metal and the 2DEG channel increases, also causing a positive shift (≈ 0.38 V) of the threshold voltage ($V_{th}$). That is, the capped device has a more negative $V_{th}$ and a higher $V_{on}$ as compared to those of the un-capped one. Since it is generally believed that larger $|V_{on}-V_{th}|$ (dynamic range) features better RF performance and ruggedness up to much higher compression regions, the capped device is thus expected to exhibit better RF performance.

To confirm that, the devices (operated in class AB at $I_{ds}$ = 12.5 mA/mm, $V_{ds}$ = 50 V) were characterized at 2.7 GHz using a load-pull system, matched for having maximum output power ($P_{out}$). Fig. 4 shows the large-signal measurement results for the capped and un-capped devices. The peak output power density and the gain of the devices with and without cap layer are 11.6, 11.1 W/mm, and 20.0, 20.7 dB, respectively. Apparently, the un-capped device features a significant higher gain and a better compression behavior than those of the capped one. This is not in line with what we expected.

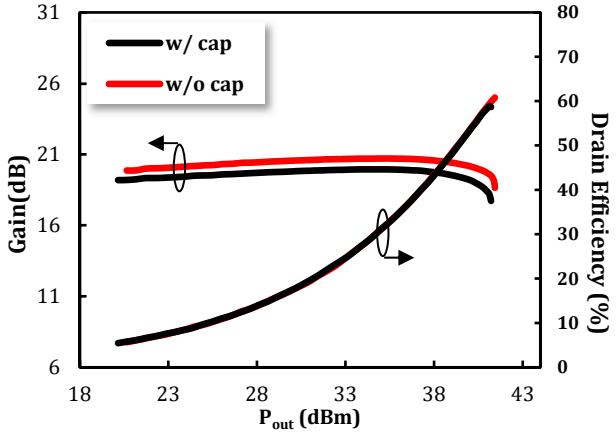


Fig. 4. Gain and Drain Efficiency vs. $P_{out}$ for AlGaN/GaN HEMTs with and without GaN cap.

To understand the cause behind this contradiction, trapping analysis utilizing C-V measurements on MIS diodes

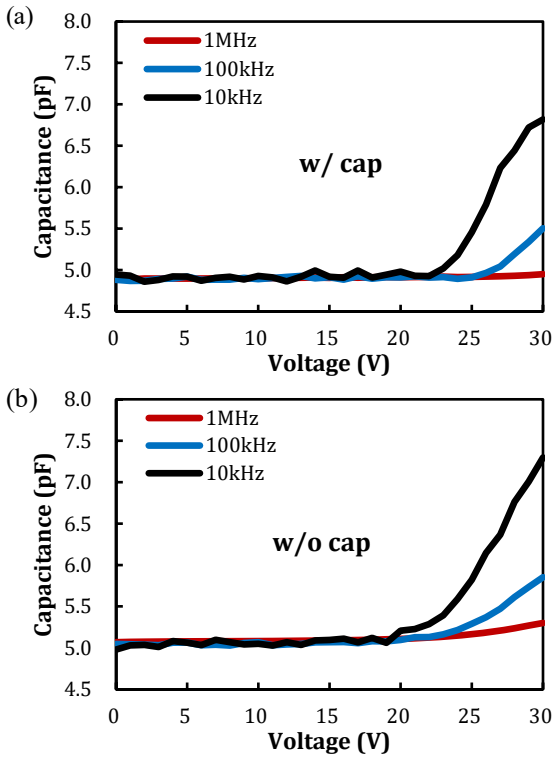


Fig. 5. Frequency dispersion of the C-V characteristics of the MIS diodes with and without GaN cap.

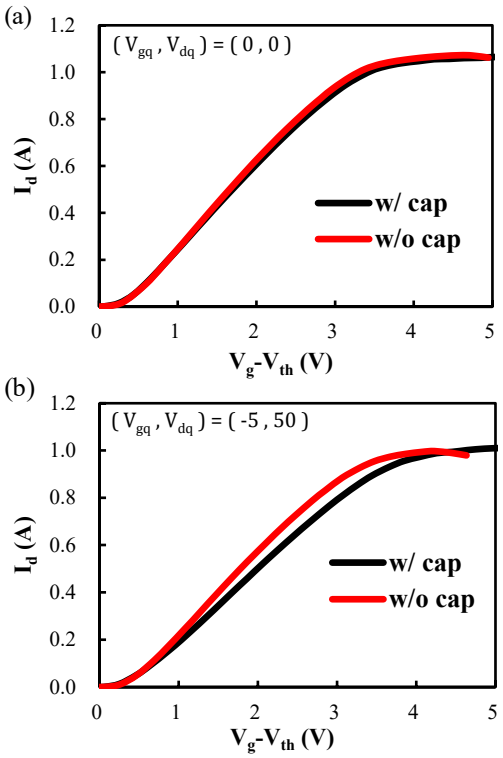


Fig. 6. Id vs. ($V_{gs}$-$V_{th}$) characteristics by the double pulse measurement for AlGaN/GaN HEMTs with and without GaN cap.

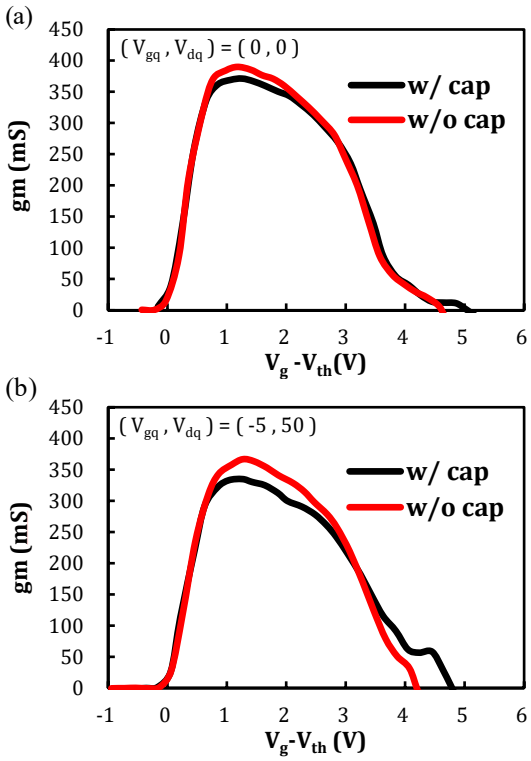


Fig. 7. Gm vs. ($V_{gs}$-$V_{th}$) characteristics by the double pulse measurement for AlGaN/GaN HEMTs with and without GaN cap.

are performed. The density of fixed charges occurred at the passivation/III-N interface can therefore be derived from the frequency dispersion of the measured C-V characteristics [16-18]. Usually, there are two different regions in the measured C-V curves. The first one for negative applied voltage corresponds to the carrier accumulation at the 2DEG channel, and the second one for positive applied voltage accounts for the effects due to the dielectric/III-N interface. Fig. 5 shows the second region of the measured frequency dispersion of the C-V characteristics of the MIS diode structures with and without GaN cap layer. The measured frequencies are 10 kHz, 100 kHz, and 1 MHz, as respectively indicated. The density of interface traps ($D_{it}$) is then calculated by the following equation [19]:

$$D_{it}=\frac{C_{SiN}}{q}\frac{V_2-V_1}{E_2-E_1}=\frac{C_{SiN}}{q}\frac{\Delta V}{\Delta E}$$

where $\Delta V$ is the on-set voltage shift for $f_1$ and $f_2$, $C_{SiN}$ is the capacitance of PECVD-SiN dielectric, q is the magnitude of electronic charge, $\Delta E$ is the difference of the energy levels between which the interface states distributed and given by

$$\Delta E=E_1-E_2=kT\ln(\frac{f_2}{f_1})$$

where k and T (= 300 K) are Boltzmann constant and temperature, respectively. From $E_C$ – 0.35 eV to $E_C$ – 0.30 eV, $D_{it}$ for the MIS diodes with and without GaN cap are estimated to be $3.7\times10^{13}$ and $2.8\times10^{13}$ $cm^{-2}eV^{-1}$, respectively. Clearly, the $D_{it}$ value of the un-capped diode is 30% lower as compared with that of the capped one.

The C-V analysis shows that the capped device has a serious frequency dispersion, which might potentially degrade the RF performance. The transfer curves obtained by the double pulse measurement technique as a function of gate overdrive voltage ($V_g$-$V_{th}$) for different quiescent points are shown in Fig. 6. Two quiescent points are used, i.e., ($V_{gq}$, $V_{dq}$) = (0 V, 0 V) and (-5 V, 50 V) respectively corresponding to the cases in which negligible and significant charge trapping are activated in the device. Pulse width and duty cycle are 1 μs and 1%, respectively. It is found that both types of devices behave similarly for ($V_{gq}$, $V_{dq}$) = (0 V, 0 V), while different $I_d$ degradation behaviors are observed when ($V_{gq}$, $V_{dq}$) = (-5 V, 50 V) is used. The $I_d$ drop for the device without GaN cap layer is significant lower. Fig. 7 shows gm versus overdrive voltage ($V_g$-$V_{th}$) curves measured by the double pulse method. As a result of the slightly loss of the gate controllability due to an increase of the distance between the gate metal and the 2DEG channel, the gm peak of the device without cap layer for ($V_{gq}$, $V_{dq}$) = (0 V, 0 V) is 4.9% higher than that of the one with cap layer. For the same device, the difference of the gm peak between different quiescent points is found to be 9.7% and 5.9% for the devices with and without cap, respectively. This result indicates that a lower level of trapping centers exists in the

SiN/AlGaN interface than that exists in the SiN/GaN interface. Our analysis shows that the observed RF performance for the two types of devices is dominated by the amount of the resulting interface trap density and the corresponding frequency dispersion.

## CONCLUSIONS

We have studied the influence of un-doped GaN cap layer on AlGaN/GaN HEMTs by using various characterization methods. We conclude that the cap layer can significantly degrade the RF performance if the interface properties are not properly tailored.

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## REFERENCES

[1] Peter Lagger, et al., *Comprehensive Study of the Complex Dynamics of Forward Bias-Induced Threshold Voltage Drifts in GaN Based MIS-HEMTs by Stress/Recovery Experiments*, IEEE Transactions on Electron Devices, vol. 61, no. 4, April 2014.

[2] Kengo Kobayashi, et al., *Current collapse suppression in AlGaN/GaN HEMTs by means of slant field plates fabricated by multi-layer SiCN*, Solid-State Electronics vol. 101, pp. 63-69, 2014

[3] Kenya Nishiguchi, et al., *Current linearity and operation stability in Al2O3-gate AlGaN/GaN MOS high electron mobility transistors,* Japanese Journal of Applied Physics vol. 56, no. 10, 2017

[4] W. Yang, J. Yuan, B. Krishnan, A. J. Tzou and W. Yeh, *C-V Measurement under Different Frequencies and Pulse-mode Voltage Stress to Reveal Shallow and Deep Trap Effects of GaN HEMTs*, 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 2018, pp. 103-107.

[5] Hui Sun, et al., *Investigation of the Trap States and $V_{TH}$ Instability in LPCVD $Si_3N_4$/AlGaN/GaN MIS-HEMTs with an In-Situ $Si_3N_4$ Interfacial Layer,* IEEE Transactions on Electron Devices, vol. 66, no. 8, August 2019

[6] Shu Yang, et al., *Mapping of Interface Traps in High-Performance Al2O3/AlGaN/GaN MIS-Heterostructures Using Frequency- and Temperature-Dependent C-V Techniques,* 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 2013, pp. 6.3.1-6.3.4

[7] T.Kikkawa, et al., *Surface-Charge Controlled AlGaN/ GaN-Power HFET without Current Collapse and Gm Dispersion*, IEDM Tech. Dig., 2001, pp. 585–588.

[8] S Arulkumaran, et al., *Studies on the Influences of i-GaN, n-GaN, p-GaN and InGaN Cap Layers in AlGaN/GaN High-Electron-Mobility Transistors*, Japanese Journal of Applied Physics vol. 44, no. 5A, 2005, pp. 2953–2960.

[9] Oleg Mitrofanov, et al, *Impact of Si doping on radio frequency dispersion in unpassivated GaN/AlGaN/GaN high-electron-mobility transistors grown by plasma-assisted molecular-beam epitaxy*, Applied Physics Letters vol. 82, no. 24, June 2003.

[10] Ponky Ivo, et al., *Influence of GaN cap on robustness of AlGaN/GaN HEMTs*, 2009 IEEE International Reliability Physics Symposium, pp. 71-75, April 2009.

[11] Ronghui Hao, et al., *Breakdown Enhancement and Current Collapse Suppression by High-Resistivity GaN Cap Layer in Normally-Off AlGaN/GaN HEMTs*, 2017 IEEE Electron Device Letters, vol. 38, no. 11, November 2017.

[12] J.A. del Alamo, et al., *GaN HEMT reliability*, 2009 Microelec. Rel. 49, pp. 1200–1206, Sep. 2009.

[13] G. Meneghesso, et al., Degradation of AlGaN/GaN HEMT devices: Role of reverse-bias and hot electron stress, Microelectronic Engineering, vol. 109, pp. 257–261, September 2013.

[14] P. Kordos, et al., *Impact of layer structure on performance of unpassivated AlGaN/GaN HEMT*, 2005 Microelec. Journal, vol. 36, pp. 438-441, March 2005.

[15] Joydeep Ghosh, et al., *Charge density and bare surface barrier height in GaN/AlGaN/GaN heterostructures: A modeling and simulation study,* Int J RF Microw Comput Aided Eng. 2018; 28:e21455.

[16] Jie-Jie Zhu, et al., Improved Interface and Transport Properties of AlGaN/GaN MIS-HEMTs With PEALD-Grown AlN Gate Dielectric, IEEE Transactions on Electron Devices, vol. 62, no. 2, February 2015.

[17] W. Yang, J. Yuan, B. Krishnan and P. Shea, *Characterization of Deep and Shallow Traps in GaN HEMT Using Multi-Frequency C-V Measurement and Pulse-Mode Voltage Stress*, in IEEE Transactions on Device and Materials Reliability, vol. 19, no. 2, pp. 350-357, June 2019

[18] S. Yang, S. Liu, Y. Lu, C. Liu and K. J. Chen, "AC-Capacitance Techniques for Interface Trap Analysis in GaN-Based Buried-Channel MIS-HEMTs," in IEEE Transactions on Electron Devices, vol. 62, no. 6, pp. 1870-1878, June 2015.

[19] Y. Hori, et al., *Characterization of interface states in Al2O3/AlGaN/GaN structures for improved performance of high-electron-mobility transistors*, 2013 J. Appl. Phys. vol. 114, no. 4, 244503, December 2013.

# Analysis of GaN-HEMT DC-Characteristic Alterations by Gate Encapsulation Layer

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**Keywords: GaN HEMT, strain engineering, gate encapsulation**

**Abstract**

**In this paper, we investigate changes of DC characteristics in GaN HFETs linked to the intrinsic stress of the 2nd passivation layer (gate encapsulation). In the earlier work of our group, it was shown [1] that the leakage current of transistors is highly sensitive to the gate encapsulation with $SiN_x$. In this study, the device characteristics before and after encapsulation with 200 nm tensile/compressive $SiN_x$ layer were analyzed. We show that a transferred strain underneath the gate contact caused by the intrinsic stress in $SiN_x$ layer not only influences the reported leakage current but also changes threshold voltage ($V_{th}$) and maximum drain current ($I_{DSmax}$) of GaN HFETs. The obtained experimental results are consistent with the performed simulations.**

## Introduction

The influence of a stressed $SiN_x$ passivation layer on GaN HFETs characteristics was reported in [1] and [2]. It is expected from theory that due to the piezoelectric nature of AlGaN/GaN epitaxial layers an external force applied to the gate structure leads to a local reduction/enhancement of the channel electron density and consequently tunes the device characteristic. In this work, the influence of intrinsic stress in the $SiN_x$ passivation layer encapsulating the gate was investigated. For this purpose, we compared the DC characteristics of the same transistors before and after passivation with 200 nm nitride deposited in a PECVD system. Nitride layers with 1.5 GPa difference in intrinsic stress were compared. The investigations were additionally backed by physical device simulations optimized for predicting local strain variations.

## Experimental

In this study, the transistors were fabricated on two identical 4 inch s.i. SiC substrates with MOVPE-grown epitaxial layers. The fabrication process includes the following steps: formation of ohmic contacts, deposition of 150 nm $SiN_x$ as the first passivation layer, device isolation by multi-energy $N^+$ implantation, gates fabrication and DC characterization of the transistors. The first nitride layer was deposited using the same recipe for both test wafers. After the first set of measurements the gates were encapsulated with 200 nm $SiN_x$. For the wafer W1 a tensile recipe with + 0.5 GPa stressed nitride and for the wafer W2 a compressive recipe with about - 1.0 GPa intrinsic stress were used. The highly compressive intrinsic stress of $SiN_x$ was realized by using a low frequency plasma excitation for the PECVD deposition process. Then the same transistors on both wafers have been characterized DC-wise. The electrical measurements were carried out on 2×50-µm transistors with 150 nm gate length, 0.5 µm source-gate and 1.5 µm drain-gate separation.

## Results and Discussion

Fig. 1 shows the mean-value output characteristics of 37 transistors measured before and after gate encapsulation. On wafer W1 with a tensile nitride (+ 0.5 GPa) as the second passivation, $I_{DSmax}$ increased by about 0.15 A/mm, while on wafer W2 with the compressive nitride (- 1.0 GPa) the increase was only by 0.03 A/mm, as compared to the measurements before gate encapsulation. The increase in maximum current on wafer W1 indicates an enhancement of electron density in the 2DEG channel. Fig. 2 shows the wafer statistics of the threshold voltage before and after 2nd passivation layer deposition. The mean $V_{th}$ of wafer W1 shifts by about – 0.35 V, while the shift on the wafer W2 is about - 0.17 V. This confirms a higher electron density underneath the gate contacts in the case of tensile passivation. Further analyses revealed that on wafer W2 the mean value of Schottky barrier height ($\phi_b$) was lowered by about 0.14 eV after passivation. K. Yao et al. [3] has proposed that Schottky contact/AlGaN interface states are responsible for strain-induced gate barrier lowering of the devices under compressive stress and vice versa. This means, the observed threshold voltage shift on the wafers was not entirely created by the direct-piezoelectric effect and $\phi_b$ has compensated the piezoelectric induced $V_{th}$ shift. In Table I the changes of the analyzed DC parameters are summarized. Based on Table I we can attribute at least 0.32 V shift of $V_{th}$ to the 1.5 GPa stress variation in the second passivation layer between wafers W1 and W2. Additionally, the intrinsic stress dissimilarity in the gate encapsulation leads to 2.8 times higher gate leakage on wafer W1 compare to W2. The lowered leakage currents on wafer W2 accompanied by the lowered $\phi_b$ again confirms a reduction of electron density in the case of compressive passivation layer.

As it was mentioned, the measurement results can be explained when the electron density in the vicinity of the gate

contact was enhanced/reduced. This effect is similar to the application of tensile/compressive stress on AlGaN/GaN epitaxial layers. Therefore, we propose that the mechanical force from the gate-encapsulation nitride was transferred through the gate metal stack and the first passivation layer into the area underneath the gate contact. This force depending on its polarity (compressive/tensile) either compresses or expands the semiconductor material at the interfaces, thus decreasing or increasing piezoelectric polarization respectively. This effect results in the observed difference in DC characteristics. The degree of the transferred stress depends on the device dimensions, i.e. thicknesses of the first and second passivation layers, gate length, gate-drain and gate-source distances, as well as on the mechanical properties, i.e. intrinsic stress in the deposited $SiN_x$ and gate-metal-stack stiffness etc.

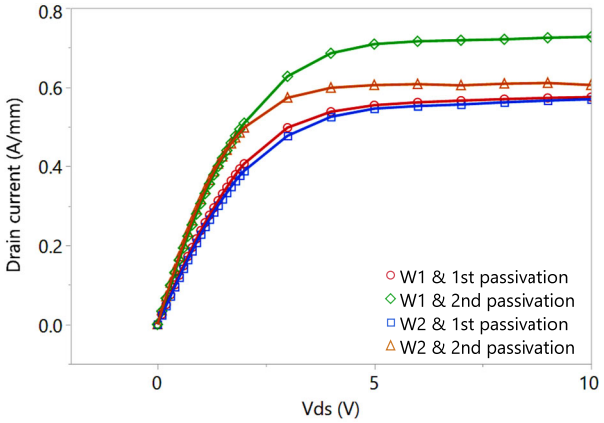


Fig. 1. Mean output characteristics for 37 transistors per wafer measured at $V_{GS}$= 1 V before and after deposition of the second passivation layer.

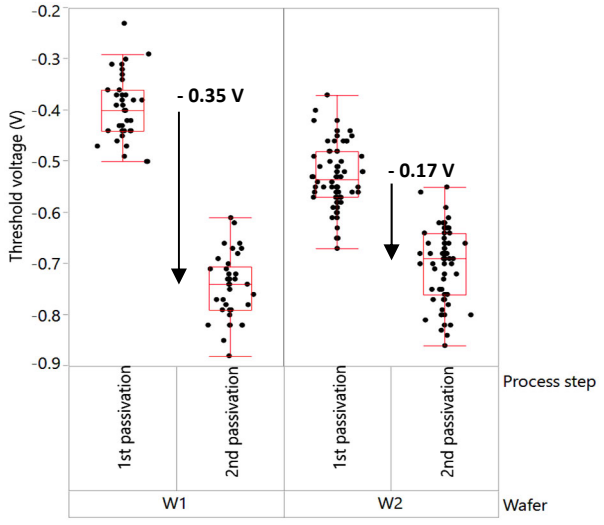


Fig. 2. Box-plot diagram is presenting the transistor threshold voltage ($V_{th}$) measured on wafers W1 and W2 before (1st passivation) and after (2nd passivation layer).

TABLE I
SUMMARY OF DC PARAMETERS SHIFT BETWEEN MEASUREMENTS BEFORE AND AFTER THE 2ND PASSIVATION LAYER

| Parameters | Wafer W1 | Wafer W2 |
|---|---|---|
| $\Delta V_{th}$ (V) | - 0.35 | - 0.17 |
| $\Delta V_{th}$ - $\Delta\phi_b$ (V) | - 0.35 | - 0.03 |
| $\Delta I_{DSmax}$ (A/mm) ($V_{DS}$=10 V) | + 0.15 | + 0.03 |
| Gate leakage | 2.35× | 0.84× |

SIMULATIONS

To verify our experimental results, the devices under study were simulated by Silvaco CAD tools. For this purpose, a model with dimensions representing the fabricated transistors was designed. Two cases for the second passivation in this model were considered. Device A with + 0.5 GPa tensile and device B with – 1.0 GPa compressive stressed $SiN_x$. The intrinsic stress in all other materials/layers was considered to be zero.

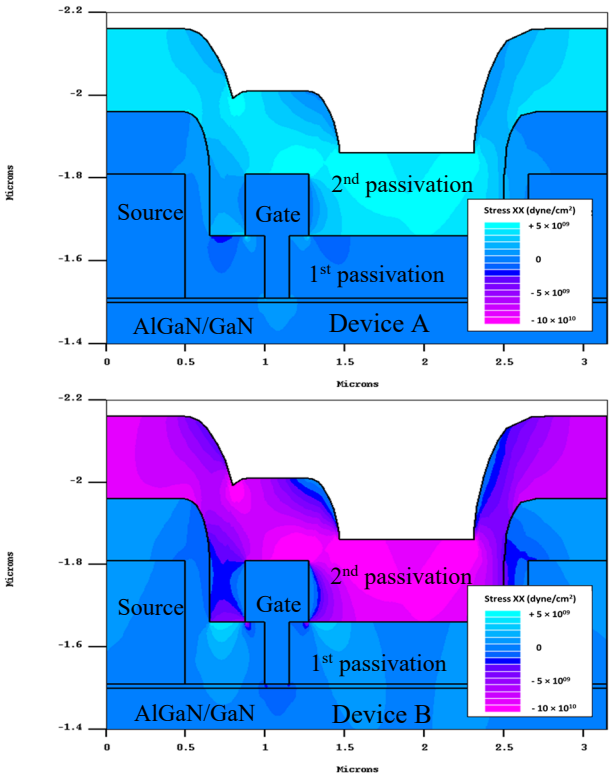


Fig. 3. Mechanical simulation (victory stress module) for devices A and B. The false colors indicate the stress.

A comparison of devices A and B in Fig. 3 shows higher stress in the device A in the area underneath the gate metallization. This is also seen in Fig. 4, which shows normal stress XX (the stress on the X plane which is caused by a force acting in the X direction) profile in AlGaN/$SiN_x$ interface. The graph illustrates that the stress difference between devices A and B increases up to about 6 Gdyne/cm$^2$ (600 MPa) at the gate edges. The stress profile also shows that the transferred tension/compression is higher at the source side of the gate contact where the distance is shorter than on the drain side. Furthermore, we have noticed that besides intrinsic stress in $SiN_x$, the dimensions and mechanical properties of each layer vary the stress profile seen under the gate contact. For instance, it was observed that the gate head overlap over $SiN_x$ and gate metallization stiffness vary the amplitude of stress XX. The simulation results prove the influence of the second passivation on stress profile in AlGaN/GaN epitaxial layer. This consequently has to result in a higher/lower 2DEG electron density for a tensile/compressive $SiN_x$ respectively.

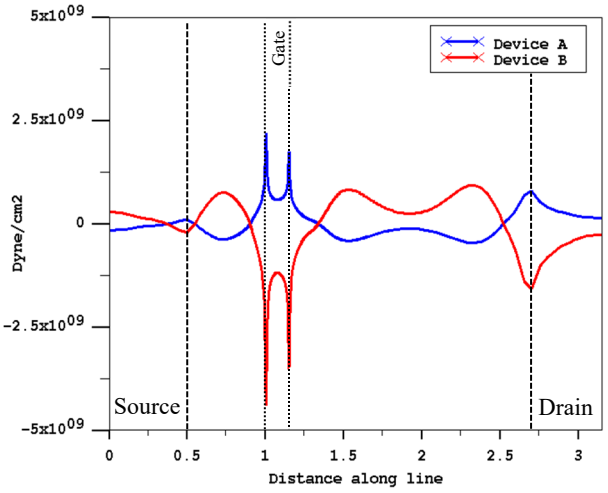


Fig. 4. Stress XX profile in the devices A and B. Cutline is selected along AlGaN/$SiN_x$ interface.

Fig. 5 presents material displacement vectors in the device A, which has a tensile stressed layer as the second passivation. As shown in the figure a tensile nitride, i.e. an expanded material, tends to shrink. This consequently causes the forces which are directed downward (Z orientation) and applying force on the gate metallization. The displacement vectors are opposite to the gate trench opening similar to a case when the first passivation is tensile stressed. Additionally, any compression in Z direction by Poisson ratio leads to further tensile stress in X orientation. These explanations are in consistent with the observed stress XX profile in Fig. 4 for tensile/compressive passivation. The discussed forces lead to expand/contract the area underneath the gate contact which is corresponding to the devices electrical properties.

The simulation of electron density in the devices A and B is presented in Fig. 6. These images show the simulated electron density at $V_{GS}$= - 3 and $V_{DS}$= + 10 V. Comparison of the electron density underneath the gate contact indicates one order of magnitude higher density in device A, which may lead to a noticeable punch-through effect. As a consequence, higher leakage current and negative shift of pinch-off voltage for the device A are expected.

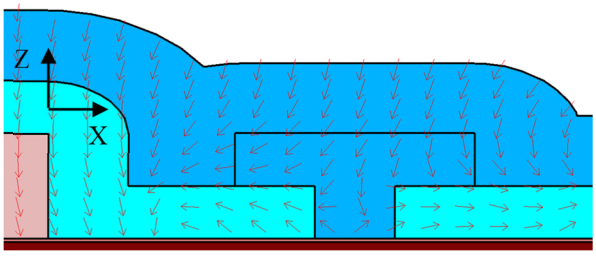


Fig. 5. Mechanical simulation of device A. The arrows are presenting the displacement in X/Z orientations in the first and second passivation layers and gate metal.

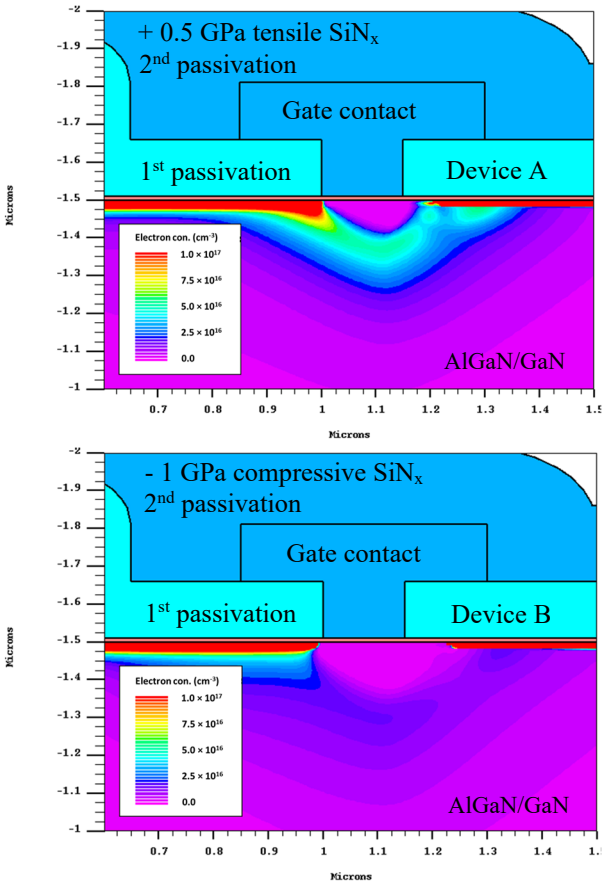


Fig. 6. Electrical simulation results for the devices A and B. Color range presents the electron density in 2DEG and GaN channel.

## Conclusions

The results of our work demonstrate the importance of the intrinsic stress in $SiN_x$ films used for the encapsulation of the gates in the fabrication of GaN HEMTs. We have shown that the mechanical strain alters the DC-characteristics of GaN HFETs after introducing intrinsically stressed nitride for the second passivation layer. This strain leads to a reduction/enhancement of the electron density in the 2DEG in the vicinity of the gate contact. As a result, gate leakage, drain current and threshold voltage were affected. This mechanism has been confirmed by simulation of the fabricated transistors showing the transferred stress to epitaxial layer and its influence on the 2DEG channel. Based on this work the intrinsic stress of the gate encapsulation layer, not necessarily $SiN_x$, can be effectively used for tuning the DC characteristics of GaN HFETs for particular applications. The observed changes in DC characteristics are expected to be even more pronounced for GaN-based transistors with shorter gate lengths.

## Acknowledgements

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## References

[1] S. Chevtchenko et al., *Investigation and Reduction of Leakage Current Associated with Gate Encapsulation by SiNx in AlGaN/GaN HFETs*, International Conference on Compound Semiconductor Manufacturing Technology, CS MANTECH 2011.

[2] K. Osipov et al., *Local 2DEG Density Control in Heterostructures of Piezoelectric Materials and Its Application in GaN HEMT Fabrication Technology*, IEEE Transactions on Electron Devices, vol. 65, no. 8, pp. 3176-3184, 2018. doi: 10.1109/ted.2018.2850010.

[3] K. Yao et al., *Piezoelectricity-Induced Schottky Barrier Height Variations in AlGaN/GaN High Electron Mobility Transistors*, IEEE Electron Device Letters, vol. 36, no. 9, pp. 902-904, 2015, doi: 10.1109/LED.2015.2456178.

## Acronyms

HEMT: High-Electron-Mobility Transistor
HFET: Heterostructure Field Effect Transistor
PECVD: Plasma-Enhanced Chemical Vapor Deposition
2DEG: Two Dimensions Electron Gas

# Improved Gate Reliability Normally-Off p-GaN/AlN/AlGaN/GaN HEMT with AlGaN Cap-Layer

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**Keywords: p-GaN gate HEMT, normally-off, etching stop, TCAD simulation, gate reliability, life time**

**Abstract**

**In this work, the dual junction-high-electron-mobility-transistor (DJ-HEMT) was investigated. The thin AlGaN was grown between the p-GaN gate and gate metal. In the TCAD simulations, the band gap and electric field were shown in this letter, proving the dual junction forming. Moreover, DJ-HEMT shows the high gate voltage swing due to the dual junction at the gate region of device, which enhance gate performance. By contrast with standard p-GaN HEMT (ST-HEMT), DJ-HEMT shows higher $V_{TH}$ of 2V, saturation current of 187mA/mm, $I_{ON}/I_{OFF}$ ratio of 5.1 x $10^8$ and gate swing voltage which is higher than 20V. In addition, DJ-HEMT also shows the lower device leakage current and superior life time measurement due to the thicker and higher barrier of AlGaN cap layer.**

## INTRODUCTION

GaN based power devices are emerging as promising candidates for the next generation power switching application due to their wide band gap, high mobility and high electric breakdown field. Conventional p-GaN gate HEMT can be modeled as two back-to-back diodes at the gate region, a reverse Schottky junction and a forward p-n junction, under the forward bias. However, back-to-back diode make the p-GaN gate HEMT operate more than 10V, but the gate bias allowed for long-term reliable operation is approximately 7~8V due to the degradation of the reverse Schottky diode induced by gate leakage current under the high electric field [1]. According to the result, in power switching application, p-GaN gate HEMT need a large threshold voltage and large gate swing voltage to prevent false turn on in high-frequency power switching and make them match with the gate drive circuit design.

The gate failure of p-GaN HEMT has been attribute at the interface between the gate metal/p-GaN layer and/or the p-n junction at p-GaN/AlGaN/GaN region under the high electric field. Moreover, the time-dependent gate breakdown (TDGB) behavior exhibits a high temperature coefficient, causing the impact ionization and carrier injection under the high electric field [2]. When the high positive bias occurring at long stress, the defects were thermally active created by hot holes. Because of the impact ionization mechanism occurring, hot holes can be generated and then accelerated to the AlGaN barrier. Furthermore, the holes release their energy to the lattice and then create the defects at the AlGaN layer or the interface between the p-GaN/AlGaN layer [3].

Hence, we propose a AlGaN/p-GaN/AlGaN/GaN HEMT to improve the gate performance and suppress the leakage current. The AlGaN cap layer not only as the barrier layer to prevent the carrier injection behavior but also forming a junction with p-GaN layer. Finally, the Schottky diode/ Junction1 (J1)/Junction2 (J2) at gate region was investigated as a new structure in the p-GaN HEMT.

## EXPERIMENTAL PROCEDURES

In this work, the AlGaN/p-GaN/AlN/AlGaN/GaN HEMT was grown on 6-inch Si (111) substrates by MOCVD. For the cross-sectional schematic of the epi structure was shown in Fig. 1(a), a 300 nm thick undoped GaN channel layer was grown on top of 4 μm thick undoped AlGaN/GaN buffer/transition layer. Moreover, there are two AlN layer designed in this structure, one is spacer layer and another one is for etching stop layer. Afterward, a 15 nm thick $Al_{0.23}Ga_{0.77}N$ layer and a 100 nm thick p-type GaN layer were grown. Finally, a 10 nm thick $Al_{0.2}Ga_{0.8}N$ was grown on the p-GaN layer, trying to form a junction there, as shown in the structure by TEM. For the device fabrication, the p-GaN etching of $Cl_2/BCl_3/SF_6$ based inductively coupled plasma and the AlN layer as an etching stop layer. The ohmic contacts were prepared by electron beam evaporation and Ti/Al/Ni/Au (25/120/25/150 nm) were stacked on the device sequentially. Then, both devices were annealed by RTA system at 875 ºC for 30 s in $N_2$ ambient. Finally, a Ni/Au (25/120 nm) gate metal stack is deposited and 100 nm of SiN was passivated.

However, the benefits of such an AlGaN cap layer could be explained by band diagram in Fig. 1(b). When the large positive bias stress at the gate side, the Schottky metal/ p-GaN diode is reversed bias, further extending the depletion region, and the electrons in the channel might be emitted over the AlGaN barrier and injected into the p-GaN Layer. Once the electrons transfer to the p-GaN region, they can be accelerated by a high electrical field in the depletion region, yielding impact ionization. Besides, the hole injection is occurring, and the holes drift in the p-GaN layer towards the p-GaN/AlGaN heterointerface and recombine with the injected electrons. Moreover, the injection holes may be a trap state in AlGaN/GaN heterostructure. Thus, the AlGaN cap layer

stacked on the p-GaN not only be a barrier but also form a depletion region, suppressing the carrier injection behavior.

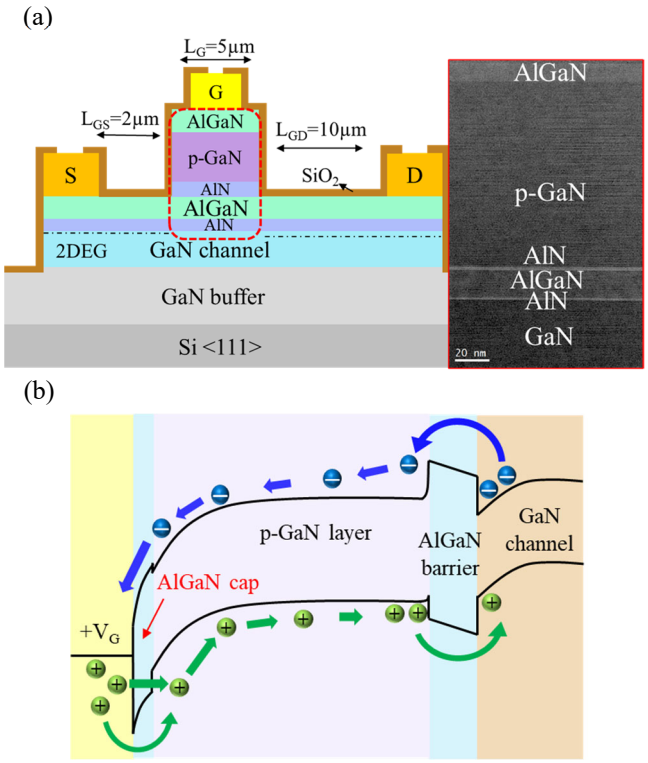


Fig. 1(a) Cross sectional schematic of p-GaN gate HEMT, (b) the band diagram of DJ-HEMT under the large positive gate voltage.

## RESULTS AND DISCUSSION

To prove the dual junction structure, the electric field was simulated by TCAD system, as shown in Fig 2. When the device is under the original state, two electric field distribute at the top side and bottom of p-GaN layer. Therefore, there are two junctions forming at gate region which are Junction1 (J1) and Junction2 (J2). Comparison with Schottky diode of ST-HEMT, the junction1 can suppress the carrier injection, and the thicker and higher barrier height may increase gate operation voltage.

Fig 3(a) and (b) shows the log-scale transfer ($I_{DS}$-$V_{GS}$) and output ($I_{DS}$-$V_{DS}$) characteristics of DJ-HEMT and ST-HEMT. As shown in Fig3(a), the off-state current for the DJ-HEMT and ST-HEMT were $3\times10^{-7}$ and $2.2\times10^{-6}$ mA/mm, respectively, at $V_{GS}$ = 0 V. Additionally, the threshold voltage ($V_{TH}$) value for the DJ-HEMT and ST-HEMT were 2 V and 0.6 V, respectively. The corresponding maximum drain current density ($I_{Dmax}$) values were 116 and 187 mA/mm, respectively.

To analyze the effect of the J1, $I_{GS}$-$V_{GS}$ measurement was shown in Fig4(a). DJ-HEMT exhibits the large gate operation voltage, and the lower gate leakage current under the forward bias. In this work, the gate turn on voltage ($V_{GS_ON}$) was defined at $I_{GS}$=1mA/mm, which are 8.2V and larger than 20V of ST-HEMT and DJ-HEMT, respectively. Moreover, when the $V_{GS}$ operate at off state and/or small bias, DJ-HEMT showing the lower leakage current, the J1 prevent the hot electrons emitted from channel to gate side. Besides, this figure also shows two solid fitting lines and they intersect at $V_{GS}$=16V. It indicates the hole injection behavior is occurring and increase the gate leakage current [4]. As the results, the AlGaN cap like a barrier which suppress the hole injection behavior efficiently. In Fig4(b), the Off-state breakdown voltage of two devices were measured by Agilent B1505, and the DJ-HEMT shows the higher Off-state breakdown voltage owing to lower leakage current.

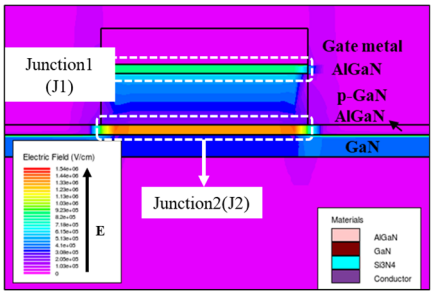


Fig. 2 Distribution of electric field of gate region by TCAD simulation.

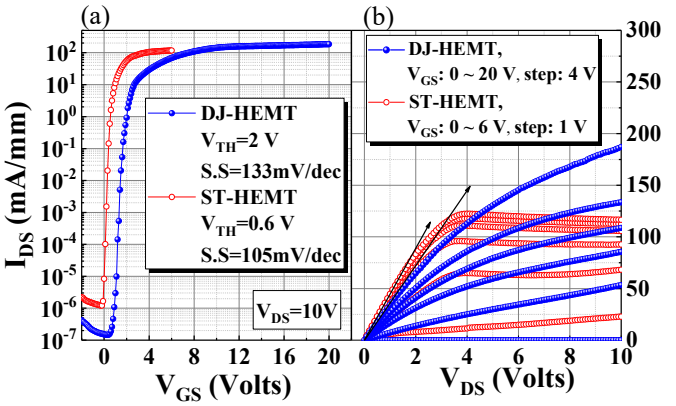


Fig. 3. DC characteristics of DJ-HEMT and ST-HEMT with $L_{GS}/L_G/L_{GD}/W_G$ = 2/5/10/100 μm. (a) Transfer characteristic. (b) Output characteristic.

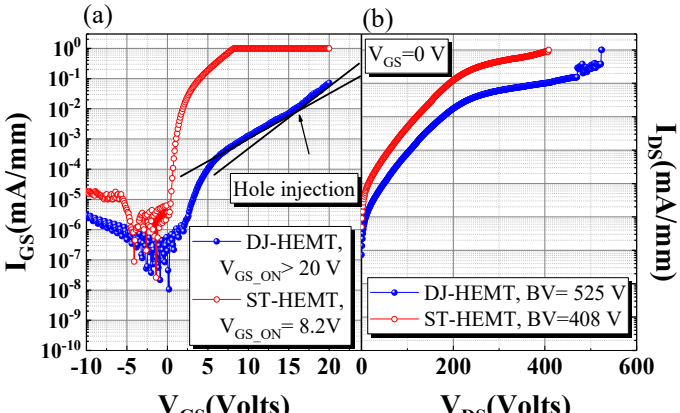


Fig. 4. (a) $I_{GS}$-$V_{GS}$ characteristic and (b) Off-state breakdown voltage measurement of DJ- and ST- HEMTs.

The aim in this work is to enhance the gate performance, so we use TDGB measurement, Weibull distribution and failure of life time to assess the gate reliability DJ-HEMT, which are shown in Fig5(a), (b), (c). In this measurement, the gate failure value is defined at $I_{GS}$=1mA/mm, and there is no bias applied on drain side. As the result, the gate was applied under three different voltages (17V, 18V, 19V). The gate current was in the lower order at the initial state due to the accumulated negative charges under the gate, so the gate leakage current was suppressed. Then, the gate leakage current becomes noisy due to the percolation path has formed. However, the gate dielectric hard breakdown occurs, which shows a sudden increase of the gate leakage current afterwards which was based on the reference of the percolation path formation [5]. After that, the Weibull distribution was plotted by calculating and the failure rate of 63.2% can be calculated of 10.8V and the slope are tight distribution and less variability. However, Fig5(d) shows the comparison of gate breakdown voltage and gate leakage current at $V_{GS}$=6V. Finally, DJ-HEMT exhibits the better gate performance and compared with each group [6-11].

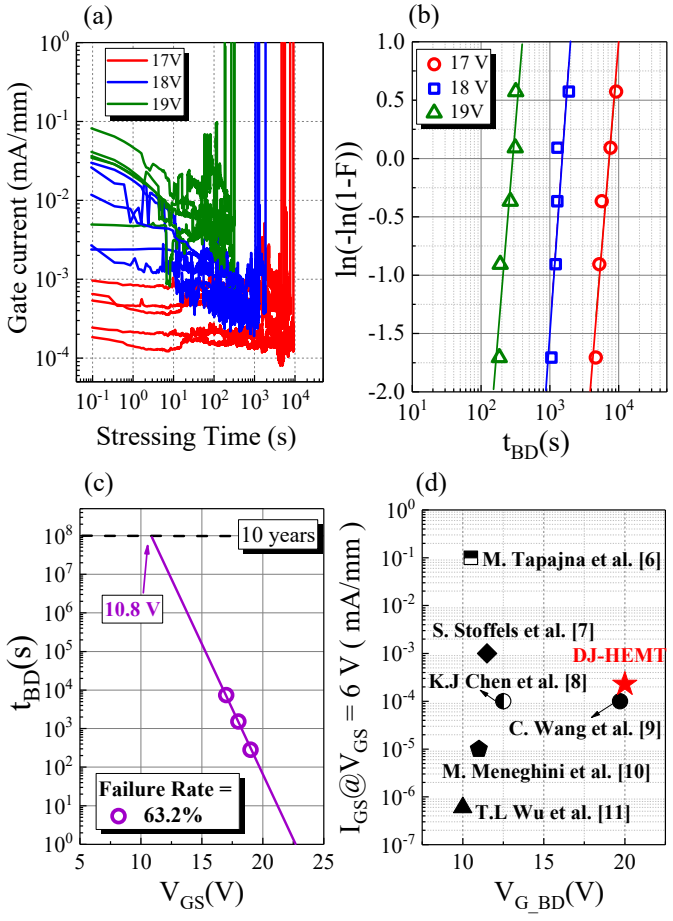


Fig. 5. (a) TDDB measurement, (b) Weibull plot of the time-to-breakdown distributions. (c) lifetime prediction with failure rate of 63.2% of DJ-HEMT. (d) Comparison with other team of the gate breakdown voltage and leakage current.

## CONCLUSIONS

A normally-off p-GaN HEMT with AlGaN cap was investigated in this work. The hot electron and hole injection are suppressed by Junction1 and AlGaN cap, respectively. The device exhibits better DC characteristic, Off-state breakdown voltage, and gate reliability owing to the dual junction gate which reduced the leakage and enlarge forward gate breakdown voltage, paving the way to higher reliable GaN power devices.

## REFERENCES


[1] Isabella Rossetto, Matteo Meneghini, Oliver Hilt, Eldad Bahat-Treidel, Carlo De Santi, Stefano Dalcanale, Joachim Wuerfl, Enrico Zanoni, and Gaudenzio Meneghesso, "Time dependent failure of GaN-on-Si power HEMTs with p-GaN gate", IEEE Trans. Electron Devices, vol. 63, no. 6, pp. 2334–2339, June 2016

[2] Li Zhang, Zheyang Zheng, Song Yang, Wenjie Song, Jiabei He, and Kevin J. Chen, "p-GaN Gate HEMT With Surface Reinforcement for Enhanced Gate Reliability", IEEE Electron Device Letters, Vol. 42, No. 1, January 2021

[3] Andrea Natale Tallarico, Steve Stoffels, Niels Posthuma, Stefaan Decoutere, Enrico Sangiorgi, Claudio Fiegna, "Threshold Voltage Instability in GaN HEMTs With p-Type Gate: Mg Doping Compensation", IEEE Electron Device Letters, Vol. 40, No. 4, April 2019

[4] Xi Tang, Baikui Li, Hamid Amini Moghadam, Philip Tanner, Jisheng Han, Sima Dimitrijev, "Mechanism of Threshold Voltage Shift in p-GaN Gate AlGaN/GaN Transistors", IEEE Electron Device Letters, Vol. 39, No. 8, August 2018

[5] Robin Degraeve, Ben Kaczer, Guido Groeseneken, "Degradation and breakdown in thin oxide layers: mechanisms, models and reliability prediction", Microelectronics Reliability 39 1445-1460, May 1999

[6] Milan Tapajna, Oliver Hilt, Eldad Bahat Treidel, Joachim Würfl, Jan Kuzmik, "Gate Reliability Investigation in Normally-Off p-Type-GaN Cap/AlGaN/GaN HEMTs Under Forward Bias Stress", IEEE Electron Device Letters, vol. 37, no. 4, April 2016

[7] Steve Stoffels, Niels Posthuma, Stefaan Decoutere, "Perimeter Driven Transport in the p-GaN Gate as a Limiting Factor for Gate Reliability", n Proc. IEEE Int. Rel. Phys. Symp. (IRPS), March 2019

[8] Jiabei He, Jin Wei, Song Yang, Yuru Wang, Kailun Zhong, Kevin J. Chen, "Frequency- and Temperature-Dependent Gate Reliability of Schottky-Type p-GaN Gate HEMTs", IEEE Transactions on Electron Devices, Vol. 66, No. 8, August 2019

[9] Chengcai Wang, Mengyuan Hua, Junting Chen, Song Yang, Zheyang Zheng, Jin Wei, Li Zhang, Kevin J. Chen, "E-Mode p-n Junction/AlGaN/GaN (PNJ) HEMTs", IEEE Electron Device Letters, Vol. 41, No. 4, April 2020

[10] Arno Stockman, Fabrizio Masin, Matteo Meneghini, Enrico Zanoni, Gaudenzio Meneghesso, Benoit Bakeroot,

Peter Moens, “Gate Conduction Mechanisms and Lifetime Modeling of p-Gate AlGaN/GaN High-Electron-Mobility Transistors”, IEEE Transactions on Electron Devices, Vol. 65, No. 12, December 2018
[11] Tian-Li Wu, Denis Marcon, Shuzhen You, Niels Posthuma, Benoit Bakeroot, Steve Stoffels, Marleen Van Hove, Guido Groeseneken, Stefaan Decoutere, “Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaN/GaN High-Electron Mobility Transistors”, IEEE Electron Devices Letters, Vol. 36, No. 10, October 2015

# Temperature Dependent Measurement of GaN Impact Ionization Coefficients

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**Keywords: GaN, breakdown, avalanche, impact ionization, temperature dependence**

**Abstract**

**Impact ionization imposes a fundamental limitation for devices in both RF power as well as power conversion and control applications. Especially for high-power devices, understanding of the temperature dependence of impact ionization is critical for device design. We report the measurement of impact ionization coefficients for both electrons and holes in GaN, including the effects of temperature. The extracted coefficients are found to be consistent with device breakdown measurements for a wide range of carrier concentration, device structures, and material growth techniques.**

## Introduction

GaN and other III-N materials are of obvious importance for terrestrial RF power applications, and are emerging as candidates for space RF as well as power conversion and control applications. As a result, developing an improved understanding of the fundamental physical limits of the technology is of increasing importance. A fundamental physical limit to the high-field handling performance of devices in GaN is impact ionization. We report measurement of the impact ionization properties of GaN, including the impact of elevated temperatures on impact ionization. These coefficients also enable the projection of the fundamental limitations of GaN-based devices; we find that our coefficients agree well with measured breakdown voltages for devices over a wide range of device design and material growth techniques.

## Device Design and Characterization

The experimental approach to measurement of impact ionization taken here is the use of the photomultiplication method, using the structures illustrated in Fig. 1. The structure in Fig. 1(a) includes a buried pseudomorphic InGaN layer to absorb the incident light, allowing pure hole injection into the drift layer when illuminated with 390 nm light. As illustrated in the band diagram in Fig. 1(a), the 390 nm wavelength illumination generates electron-hole pairs only in the InGaN layer, and the holes are subsequently injected into the drift layer. In contrast, the structure in Fig. 1(b) is used for electron injection. In this case, 193 nm wavelength light is used to generate electron-hole pairs near the surface of the p-GaN anode; the electrons diffuse to the drift layer resulting in pure electron injection into the drift layer. By measuring the reverse-biased current-voltage characteristics both in the dark and under illumination at different temperatures, the carrier multiplication can be determined and the resulting impact ionization coefficients can be extracted vs. temperature. For the devices reported here, the fabrication flow was similar to that reported in [1], including the use of an N(14) implant based edge termination. Device measurements were performed on-wafer in a shielded variable-temperature probe station.

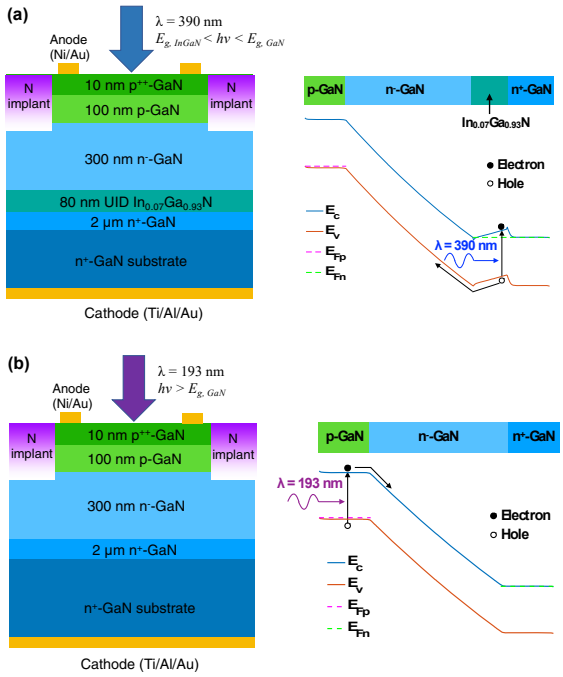


Fig. 1. Cross sections and illustrative band diagrams of device structures used for impact ionization coefficient measurement; (a) structure and band diagram for hole injection, (b) structure and band diagram for electron injection.

Figure 2 shows typical reverse-bias dark and illuminated measurements for both structures from which the extractions were performed. The devices show a positive temperature coefficient of breakdown, as expected for impact-ionization limited performance. The "shoulder" seen in the photocurrent response in Fig. 2(a) is caused by the polarization-induced barrier at the InGaN/GaN heterointerface, and influences only the low-field behavior of the device away from the onset of impact ionization.

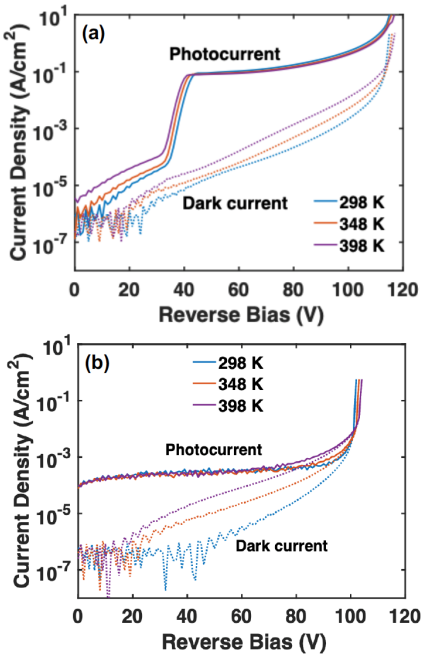


Fig. 2. Measured reverse-bias dark and illuminated I-V curves for: (a) hole injection using the structure in Fig. 1(a) with 390 nm illumination, and (b) electron injection using the structure in Fig. 1(b) with 193 nm illumination.

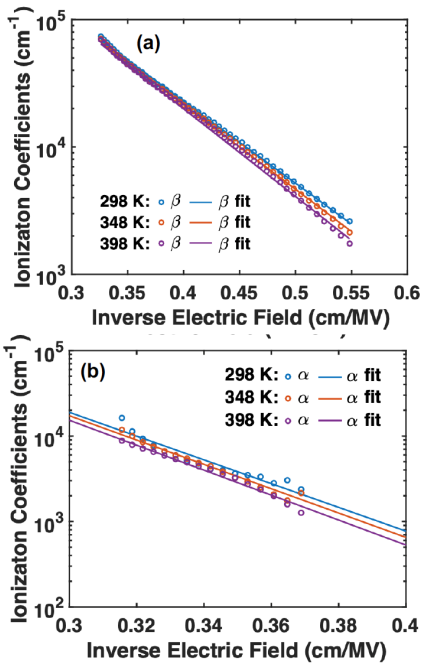


Fig. 3. Measured impact ionization coefficients for: (a) holes, β, and (b) electrons, α. Fits to the Okuto-Crowell model are also shown.

## IMPACT IONIZATION COEFFICIENTS

From the measured characteristics in Fig. 2, the impact ionization characteristics can be extracted. For holes, the data in Fig. 2(a) can be used directly [2] under the assumptions that the field is uniform in the drift layer, that no electrons are injected, and that the impact ionization for holes is larger than that of electrons [3]. For the case of electrons, feedback between the electron and hole generation must be considered; we use the approach outlined in [4]; additional details on the extraction methodology can be found in [5].

The resulting temperature-dependent impact ionization coefficients for holes and electrons are shown in Fig. 3(a) and (b), respectively. Also shown in Fig. 3 are least-squares fits to the Okuto-Crowell model for temperature-dependent impact ionization [6]. In the Okuto-Crowell model, the impact ionization coefficients take the form of the Chynoweth model for impact ionization (equation (1) below) [7], but with temperature-dependent parameters *a(T)* and *b(T)* of the form shown in equations (2) and (3) [6]:

$$\alpha, \beta(E,T) = a(T)\exp\left(-\frac{b(T)}{E}\right) \quad (1)$$

$$a(T) = a_o(1 + c(T - T_o)) \quad (2)$$

$$b(T) = b_o(1 + d(T - T_o)) \quad (3)$$

Table 1 summarizes the coefficients obtained and the form of the model. Consistent with previous reports, the impact ionization coefficients for holes exceeds that of electrons (β/α = 5.3 at 3.3 MV/cm), in line with prior measurements and theoretical expectations [3, 8]. It is also noteworthy that the impact ionization coefficients are weak functions of temperature. This is promising for achieving device performance at high temperatures or self-heating conditions without significant off-state voltage derating.

As a check for consistency between measurement and the extracted parameters, the coefficients in Table 1 were used to simulate the hole and electron multiplication factors as a function of electric field for the device structures in Fig. 1; a comparison between the simulated and measured multiplication factors is provided in Fig. 4. As can be seen, excellent agreement is obtained over the full electric field range evaluated for both electrons and holes.

A critical issue for material parameter extractions like these is their predictive abilities for structures other than those used in the extraction process. Since the temperature coefficient of breakdown is controlled by impact ionization, this provides one means to assess the fidelity of the measured

Table 1. Impact Ionization Model and Extracted Parameters for GaN

**Model:** $\alpha, \beta(E,T) = a(T)\exp\left(-\frac{b(T)}{E}\right)$; $a(T) = a_o(1 + c(T - T_o))$; $b(T) = b_o(1 + d(T - T_o))$; E is electric field (V/cm), T is temperature (K).

| Parameter | Electrons (α) | Holes (β) |
|---|---|---|
| $a_o$ | 2.77x10$^8$ cm$^{-1}$ | 8.53x10$^6$ cm$^{-1}$ |
| $b_o$ | 3.20x10$^7$ V/cm | 1.48x10$^7$ V/cm |
| c | 3.09x10$^{-3}$ K$^{-1}$ | 3.23x10$^{-3}$ K$^{-1}$ |
| d | 5.03x10$^{-4}$ K$^{-1}$ | 7.02x10$^{-4}$ K$^{-1}$ |
| $T_0$ | 298 K | 298 K |

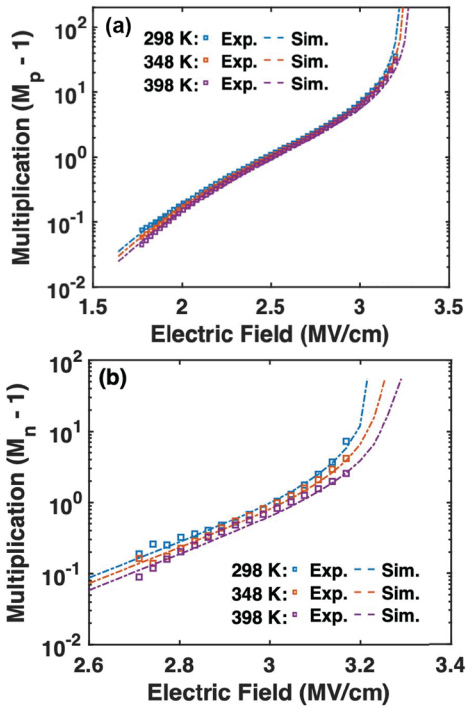


Fig. 4. Measured and simulated carrier multiplication factors for (a) holes and (b) electrons.

coefficients to experiment. The temperature dependence of breakdown in avalanche-limited devices is given by $BV(T) = BV_{298K}(1 + k\Delta T)$, where k is the temperature coefficient [9]. Figure 5 shows the temperature coefficient of breakdown extracted as a function of drift layer doping expected using the measured data reported here, as well as comparisons to measured avalanche-limited devices reported in the literature. As can be seen, good agreement between the measured temperature dependence of breakdown voltage and drift layer doping is observed.

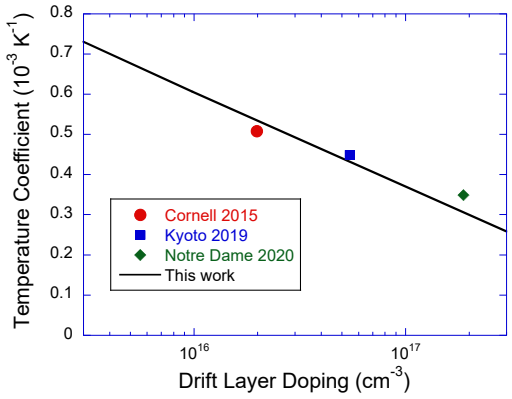


Fig. 5. Drift-layer doping density dependence of the temperature coefficient of breakdown from the reported coefficients (solid line) compared to literature reports for avalanche-limited devices [10-12].

To further assess the generality of the impact ionization coefficients reported here, Fig. 6 shows a comparison of the breakdown voltage vs. drift layer doping for a range of devices (FETs and diodes) reported in literature from a number of groups around the world [5, 13-32], as well as the avalanche-limited theoretical breakdown voltage based on the measured coefficients reported here. As can be seen, the model accurately bounds the experimental results from many groups, despite variations in material growth techniques, device structures, fabrication approaches, breakdown voltage, and carrier concentrations. This suggests the model and coefficients may be broadly applicable to GaN devices generally.

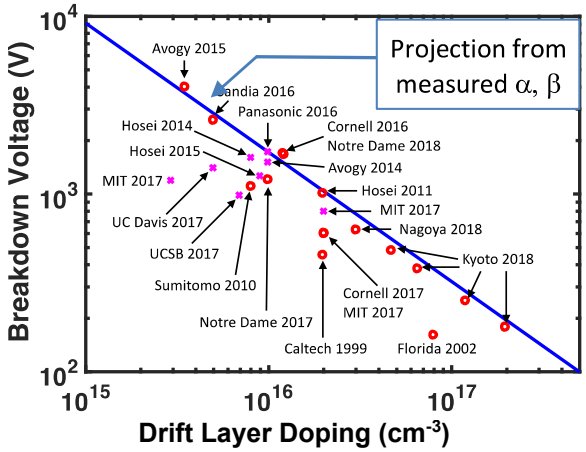


Fig. 6. Comparison of projected breakdown from impact ionization to measured breakdown in literature [5, 13-32].

## Conclusions

The impact ionization coefficients for GaN as a function of temperature have been measured experimentally and compared to device performance. This will facilitate optimization of future RF and power device designs.

## Acknowledgements

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## References

[1] J. Wang et al., Appl. Phys. Lett., **113**, 0234502, 2018.
[2] H. Niwa et al., IEEE Trans. Electron Dev., **62**, 3326, 2015.
[3] L. Cao et al., Appl. Phys. Lett., **112**, 0262103, 2018.
[4] C. Lee et al., Phys. Rev., **134**, A761, 1964.
[5] L. Cao et al., IEEE Trans. Electron Dev., **68**, 2021.
[6] Y. Okuto and C. Crowell, Solid-State Electron., **18**, 161, 1975.
[7] A. G. Chynoweth, Phys. Rev., **109**, 1537, 1958.
[8] I. Oguzman et al., J. Appl. Phys., **81**, 7827, 1997.

[9] I. Kizilyalli et al., IEEE Trans. Electron Dev., **62**, 414, 2015.
[10] L. Cao, PhD dissertation, Univ. of Notre Dame, 2020.
[11] T. Maeda et al., IEEE Electron Dev. Lett., **40**, 941, 2019.
[12] Z. Hu et al., Appl. Phys. Lett., **107**, 243501, 2015.
[13] T. Oka et al., Appl. Phys. Exp., **8**, 054101, 2015.
[14] T. Maeda et al., Proc. IEDM, 30.1, 2018.
[15] Z. Bandic et al., Appl. Phys. Lett., **74** 1266, 1999.
[16] J. Johnson et al., IEEE Trans. Electron Dev., **49**, 32, 2002.
[17] Y. Saitoh et al., Appl. Phys. Exp., **3**, 081001, 2010.
[18] W. Li et al., IEEE Trans. Electron Dev., **64**, 1635, 2017.
[19] Y. Zhang et al., IEEE Electron Dev. Lett., **38**, 1097, 2017.
[20] K. Nomoto et al., Phys. Stat. Solidi A, **208**, 1535, 2011.
[21] Y. Zhang et al., Proc. IEDM, 10.2, 2016.
[22] K. Nomoto et al., IEEE Electron Dev. Lett., **37**, 161, 2016.
[23] O. Atkas and I. C. Kizilyalli, IEEE Electron Dev. Lett., **36**, 890, 2015.
[24] J. Dickerson et al., IEEE Trans. Electron Dev., **63**, 419, 2016.
[25] S. Usami et al., Appl. Phys. Lett., **112**, 182106, 2018.
[26] T. Oka et al., Appl. Phys. Exp., **7**, 021002, 2014.
[27] H. Nie et al., IEEE Electron Dev. Lett., **35**, 939, 2014.
[28] D. Shibata et al., Proc. IEDM, 10.1, 2016.
[29] M. Sun et al., IEEE Electron Dev. Lett., **38**, 509, 2017.
[30] C. Gupta et al., IEEE Electron Dev. Lett., **38**, 353, 2017.
[31] D. Ji et al., Proc. IEDM, 9.4, 2017.
[32] J. Wang et al., Appl. Phys. Lett., **113**, 023502, 2018.

# High Thermal Dissipation of Normally off p-GaN Gate AlGaN/GaN HEMTs on 6-inch N-doped Low Resistivity SiC Substrate

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**Keywords: p-GaN gate HEMT, normally off, low resistance SiC substrate, temperature**

**Abstract**

**Efficient heat removal through the substrate is required in high-power operation of AlGaN/GaN high-electron-mobility transistors (HEMTs). Thus, an SiC substrate was used due to its popularity. This article reports the electrical characteristics of normally off p-GaN gate AlGaN/GaN high-electron-mobility transistors (HEMTs) on low resistivity SiC substrate compared with the traditional Si substrate. The p-GaN HEMTs on SiC substrate possess several advantages, including electrical characteristic and good qualities of epitaxial crystals, especially on temperature performance. Additionally, the price of low resistivity SiC substrate is three times lower than the ordinary SiC substrate.**

## INTRODUCTION

Gallium nitride high-electron-mobility transistors (HEMTs) have attracted increasing attention in the field of high-frequency and high-power device applications due to their high breakdown field, high mobility, and good thermal properties. However, they are naturally normally on devices. For high-power applications, off devices are normally desirable for system reliability [1]. Thus, several researches have been proposed to realize the normally off operation characteristics of the AlGaN/GaN HEMTs such as fluorine base plasma treatment [2], [3], ultrathin barrier (UTB) [4], and gate-recessed structures [5], [6].

Recently, GaN HEMTs with a p-GaN gate stack (p-GaN gate HEMTs) have been suggested as one of the candidates, in which a p-GaN layer on top of the AlGaN barrier depletes the 2D electron gas carriers in the channel [7]–[9]. The normally off p-GaN gate AlGaN /GaN high-electron-mobility transistor (HEMT) on a SiC substrate is expected to be a good choice for high-power switching components due to its high thermal conductivity, low resistivity, and high-voltage capability. Another advantage of using SiC substrate is its less lattice mismatch of ~3% for GaN (that of Si is ~17%). Owing to the high material properties of gallian nitride and SiC substrate, these devices are expected to operate in high temperature environments [10].

Here we analyzed the DC, breakdown, pulsed, and thermal measurement performances of AlGaN/GaN HEMTs with p-GaN gate between low resistivity SiC and ordinary Si substrates. Finally, the heat removal through the SiC substrate had the most outstanding performance.

## EXPERIMENTAL PROCEDURES

In this work, the structure of p-GaN gate/AlGaN/GaN HEMT was grown on a 6-inch SiC substrate by MOCVD, as shown in Fig.1 (a). The fabrication process starts with device isolation by an Ar implantation. The 5-µm-long p-GaN gate island was removed by $Cl_2/BCl_3/SF_6$ dry etching and the etching depth stopped by the 1nm AlN etching stop layer. After dry etching, the source and drain ohmic contacts were prepared using the electron beam evaporation of a multilayered Ti/Al/Ni/Au (25 nm/120 nm/25 nm/150 nm) sequence, patterned by a lift-off process, and annealed by a 30-s rapid thermal annealing (RTA) at 875°C in $N_2$ ambient. Finally, a Ti/Au (25/150 nm) gate metal stack was deposited, and 100 nm of SiN was passivated by plasma enhanced chemical vapor deposition (PECVD).

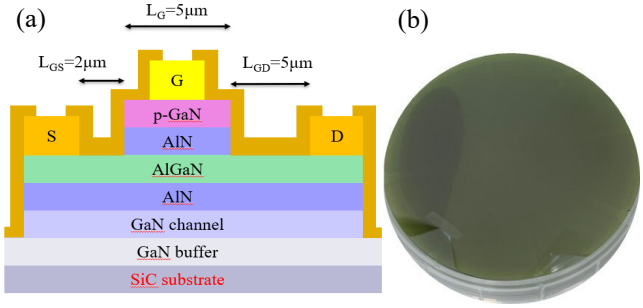


Fig.1. (a)Structure of p-GaN gate HEMT on low resistance substrate. (b) Low resistance SiC outward appearance.

## RESULTS AND DISCUSSION

Figure 2 (a) and (b) shows the log-scale transfer ($I_{DS}$-$V_{GS}$) and output ($I_{DS}$-$V_{DS}$) characteristics of GaN on low resistivity SiC substrate HEMT (LRSiC-HEMT) and Si substrate HEMT (Si-HEMT). As shown in Fig.2 (a), the off-state current for the LRSiC-HEMT and Si-HEMT were $1.37\times10^{-5}$ and $5.2\times10^{-5}$ mA/mm at $V_{GS}$ = 0 V, the $I_{on}/I_{off}$ ratio were 1.5x $10^8$ and 1.85x$10^6$, and delivered the normally off operation with a positive $V_{TH}$ of 3.2V and 1.8V defined at $I_D$ = 1 mA/mm, respectively. In Fig. 2 (b), corresponding maximum drain current density ($I_{Dmax}$) values were

131mA/mm and 108mV/mm at gate-to-source voltage ($V_{GS}$) = 8V and drain-to-source voltage ($V_{DS}$) = 10V. The $I_{Dmax}$ value of the LRSiC-HEMT was 28% higher than that of the Si-HEMT. Additionally, the LRSiC-HEMT also exhibits a lower on resistance ($R_{ON}$) of 16Ω·mm.

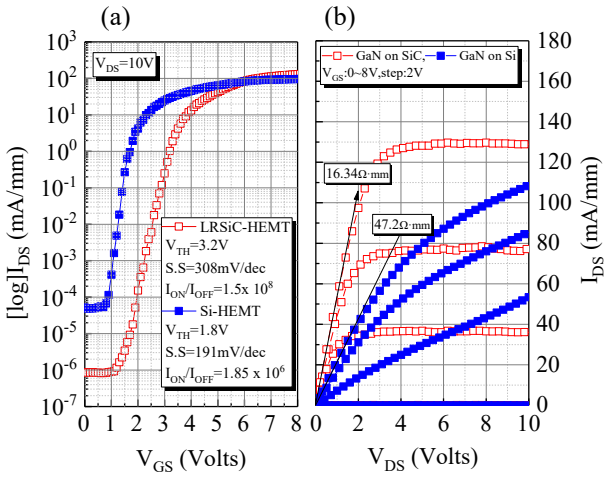


Fig. 2. I–V characteristics of LRSiC-HEMT and Si-HEMT with $L_{GS}/L_G/L_{GD}/W_G$ = 2/5/5/100 µm. (a) Transfer $I_{DS}$-$V_{GS}$ characteristic. (b) Output $I_{DS}$-$V_{DS}$ characteristic.

The breakdown voltage, BV, of the devices is determined with the drain leakage–current reaching 1 mA/mm. As shown in Fig. 3, the off-state breakdown voltages and vertical breakdown voltages of LRSiC-HEMT and Si-HEMT were 325V, 310V, 413V, and 319V, respectively. Vertical breakdown voltage measurements were performed on both wafers by substrate grounded and ohmic contact pattern swept from 0V up to breakdown voltage, and the size of the ohmic pattern is about 100µm x 100µm. Although the epitaxy technology using low resistivity SiC substrate wasn't such stable, performance on device and substrate's breakdown voltages were still better than the traditional Si substrate.

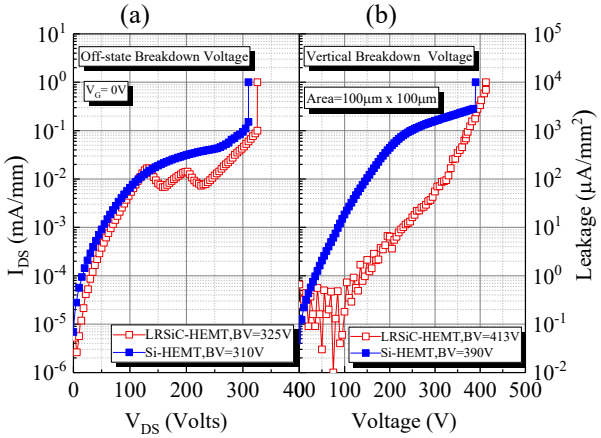


Fig. 3. (a) Off-state breakdown voltage and (b) vertical breakdown voltage measurement.

Having confirmed the importance of the surface temperature distribution measurements, the temperature–time curve was shown in Fig.4 by using an infrared(IR) thermographic system with micro-Raman spectroscopy. On account of having much higher thermal conductivity, SiC could achieve an outstanding performance on heat dissipation. For the set of device measurements, $V_{DS}$ was held constant at 10 V, while $I_{DS}$ was kept at 100 mA/mm for 60 s, then waiting for the device cool down about 50 s. As expected, the center of the gate area reached to the highest temperature. As shown in Fig.4, following with the time, the temperature gradient appears to increase. The temperature of LRSiC-HEMT was heated up to 34.4°C and cooled down to 30°C rapidly. On the contrary, Si-HEMT accumulated much more heat to reach 37.5°C and removed it slowly.

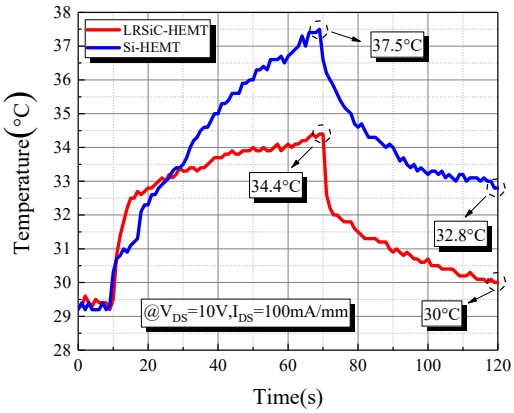


Fig. 4. Temperature following with time, device operating for 60 s and cooling down for 50 s.

To investigate the thermal stability of LRSiC-HEMT, transfer characteristics were measured from room temperature (25°C) to 175°C with a 50°C step (Fig.5 (a)). The device shows a good thermal stability with the $V_{TH}$ shifting less than 0.4V up to 175°C (Fig.5 (b)). $R_{ON}$ increases by about 3.3 times, due to stronger phonon scattering at higher temperature.[11]

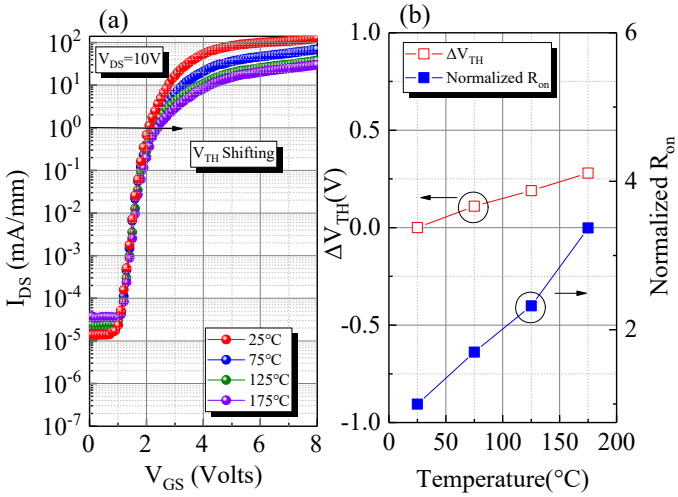


Fig. 5. (a) Transfer characteristics of LRSiC-HEMT from 25°C to 175°C (b) T-dependence of $V_{TH}$ and $R_{ON}$.

To analyze the trapping/detrapping effect, the pulsed I–V characteristic and the dynamic $R_{on}$ ratio of the LRSiC-HEMT were measured using a pulse width of 2 μs and period of 200 μs. The carriers will be trapped in buffer layer or near the surface which is in the AlGaN layer or passivation interface during the pulse measurement. Therefore, it will reduce the carrier density and make the resistance higher [12]. In this work, the $V_{DSQ}$ for LRSiC-HEMT was swept from 0 to 80V with the step of 20V in Fig. 6. Clearly, the current collapse and the dynamic $R_{ON}$ ratio of the Si-HEMT are both worse than LRSiC-HEMT. Additionally, under relatively high stress lead to I-V slope decrease because of the defect trap density in buffer layer and surface. In Fig7, the dynamic $R_{ON}$ ratio are 6.8 times and 2.5 times at $V_{DSQ}$=80V, respectively.

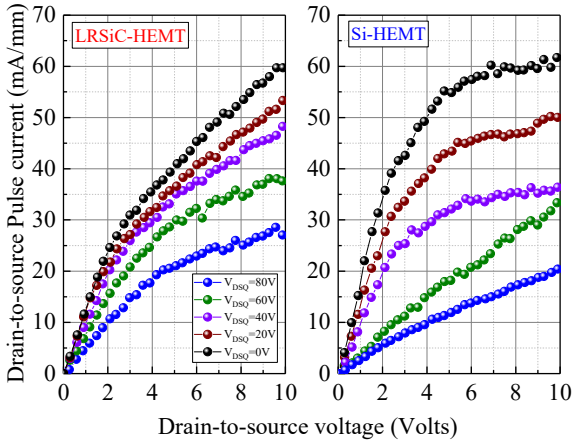


Fig. 6. Pulsed $I_{DS}$–$V_{DS}$ characteristics from quiescent gate bias ($V_{GSQ}$) point of 0 V with 2 μs pulse width and 200 μs pulse period. The quiescent drain bias ($V_{DSQ}$) was then swept from 0 to 80 V (in 20 V increments).

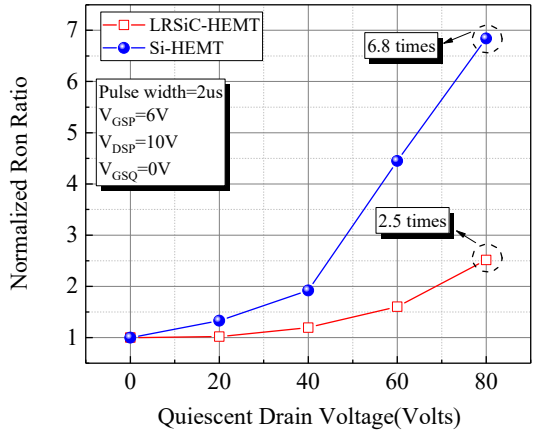


Fig. 7. Dynamic $R_{on}$ ratio of the LRSiC-HEMT and Si-HEMT.

Table.1. Reference price and resistivity of low resistivity SiC substrate and high resistivity SiC substrate.

| | Reference price | Resistivity(Ω·cm) |
|---|---|---|
| **LRSiC(6 inch)** | USD1000 | 0.015~0.025 |
| **HRSiC(6 inch)** | USD3000 | >1E5 |

## CONCLUSIONS

In this work, normally off AlGaN/GaN high-electron-mobility transistors (HEMTs) with p-GaN gate on low resistivity SiC substrate (LRSiC-HEMT) was developed. Comparing to the Si-HEMT, LRSiC-HEMT obtained many advantages, such as higher output current, higher off-state and vertical breakdown voltages, lower dynamic Ron ratio, especially thermal performance. In addition, the price of low resistivity SiC substrate is much lower than ordinary SiC substrate. Therefore, it's promising to be an excellent choice to solve the heat problem for power devices.

## REFERENCES


[1] M. Asif Khan, Q. Chen, C. J. Sun, J. W. Yang, M. Blasingame, M. S. Shur, and H. Park, "Enhancement and depletion mode GaN/AlGaN heterostructure field effect transistors," Appl. Phys. Lett., vol. 68, no. 4, pp. 514–516, Jan. 1996.

[2] W. Chen, K.-Y. Wong, and K. J. Chen, "Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-onSi switch-mode power supply converters," in Proc. IEEE IEDM, Dec. 2008, pp. 1–4.

[3] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "Highperformance enhancement-mode AlGaN/GaN HEMTs using fluoridebased plasma treatment," IEEE Electron Device Lett., vol. 26, no. 7, pp. 435–437, Jul. 2005, doi: 10.1109/LED.2005.851122.

[4] Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, "Enhancementmode AlGaN/AlN/GaN high electron mobility transistor with low ON-state resistance and high breakdown voltage," Jpn. J. Appl. Phys., vol. 45, nos. 42–45, Nov. 2006, Art. no. L1168.

[5] T. Oka and T. Nozawa, "AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications," IEEE Electron Device Lett., vol. 29, no. 7, pp. 668–670, Jul. 2008, doi: 10.1109/LED.2008.2000607.

[6] K.-W. Kim et al., "Effects of TMAH treatment on device performance of normally off Al2O3/GaN MOSFET," IEEE Electron Device Lett., vol. 32, no. 10, pp. 1376–1378, Oct. 2011, doi: 10.1109/LED.2011.2163293.

[7] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, "Gate injection transistor (GIT) normally-off AlGaN/GaN power transistor using conductivity modulation," IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 3393–3399, Dec. 2007.

[8] M. Meneghini, C. de Santi, T. Ueda, T. Tanaka, D. Ueda, E. Zanoni, and G. Meneghesso, "Time- and field-dependent trapping in GaN-based enhancement-mode transistors with p-gate," IEEE Electron Device Lett., vol. 33, no. 3, pp. 375–377, Mar. 2012.
[9] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and J. Wurfl, "Normallyoff AlGaN/GaN HFET with p-type GaN gate and AlGaN buffer," in Proc. ISPSD, 2010, pp. 347–350.
[10]Clément Fleury, High temperature performances of normally-off p-GaN gate AlGaN/GaN HEMTs on SiC and Si substrates for power applications, Microelectronics Reliability Volume 55, Issues 9–10, August–September 2015, Pages 1687-1691
[11]Chengcai Wang, E-Mode p-n Junction/AlGaN/GaN (PNJ) HEMTs, IEEE ELECTRON DEVICE LETTERS, VOL. 41, NO. 4, APRIL 2020
[12]I. Hwang, J. Kim, S. Chong, H.S. Choi, S.K. Hwang, j. Oh, J.K. Shin, U. In Chung, "Impact of channel hot electrons on current collapse in AlGaN/GaN HEMTs.", IEEE Electron. Device Lett. 34 (12) (Dec. 2013) 1494–1496, https://doi.org/10.1109/ LED.2013.2286173. H.-C. Chiu et al.

# SESSION 6:
# PROCESS AND CONTROL

# GaN Through-substrate Via Process for GaN-on-GaN HEMT Power Amplifiers

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**Keywords: GaN-on-GaN, HEMT, Through-substrate via, Power amplifier**

**Abstract**

**A GaN through-substrate via (TSV) process for GaN-on-GaN HEMT power amplifiers (PAs) is described. In order to apply GaN-TSV to GaN-on-GaN HEMT PA, a thick Ni etch stop structure and a metal removal process on the dicing line were developed. Finally, GaN-TSV was applied to a GaN-on-GaN HEMT PA. The reliable connection between the etch stop and GaN-TSV was observed with a cross-sectional SEM. In CW operation, a maximum output power of 47.4 dBm (54.6 W), a maximum PAE of 63.3%, and a gain of 14.7 dB were obtained. This indicates that GaN-on-GaN HEMT PA has suitable heat dissipation properties.**

## INTRODUCTION

Gallium nitride (GaN) substrates are very attractive for high-frequency and high-power GaN high electron mobility transistors (GaN HEMTs) because of their potential to grow high-quality GaN epitaxial layers due to the extremely low dislocation density ($10^4$–$10^6$ $cm^{-2}$). We demonstrated remarkable suppression of current collapse of GaN-on-GaN HEMTs and excellent power characteristics [1]. Furthermore, a recorded power-added efficiency (PAE) of over 80% at ISM-band was obtained [2]. However, GaN substrates exhibit thermal conductivity (230 W/mK) lower than that of the widely used silicon carbide (SiC) substrates (420 W/mK) [3]. Hence, we optimized the thermal management of GaN-on-GaN using thermal simulation and found that the temperature rise was minimum at a substrate thickness of 100 μm. From these results, we developed methods for backside processing of GaN-on-GaN, such as backgrinding, CMP and dicing [4]. In addition, we developed a high-rate ICP etching for GaN through-substrate vias (TSVs) to reduce the source inductance of GaN-on-GaN HEMT power amplifiers (PAs). GaN via-holes with a depth of 91 μm were successfully fabricated with a high etch rate of 1.5 μm/min and a high etch selectivity of 35 [5]. To suppress pillar formation, increasing the wafer temperature by controlling the helium pressure for cooling was effective.

In this study, we developed a GaN-TSV process for GaN-on-GaN HEMT PAs. A 50 W-class GaN-on-GaN HEMT PA with GaN-TSVs was demonstrated. In addition, we will discuss the heat dissipation of GaN-on-GaN HEMT PAs using thermal simulation.

## EXPERIMENTAL PROCEDURE

We used semi-insulating 2-in. GaN (0001) substrates with a dislocation density of less than $5 \times 10^6$ $cm^{-2}$ (SCIOCS product), which were grown using the void-assisted separation (VAS) method with hydride vapor phase epitaxy (HVPE). GaN-HEMT epitaxial layers were grown by metalorganic vapor phase epitaxy (MOVPE) and front-side processing was performed [1, 2].

The backside process basically follows the SiC via process flow that we had developed [6, 7]. After fabricating the front-side device, thermoplastic adhesion was used to bond the wafer to a 4-in. supporting carrier. After that, the backside (N-polar side) of the GaN substrate was ground, and then CMP was performed [4]. The GaN substrate was thinned to 100 μm. An electroplated Ni metal mask with openings of 70 μm in diameter on the backside of the GaN substrate was fabricated. ICP etching was performed in a mixture of $Cl_2$ and $BCl_3$ [5]. Au electroplating was performed after seed metal sputtering. Finally, the dismounted wafer was cleaned and then diced using a stealth dicing process.

The sample was evaluated with SEM and an optical microscope. The power characteristics of the PAs were evaluated by large-signal measurement. In addition, thermal simulation was carried out to understand heat dissipation of GaN-on-GaN HEMT PAs.

## GAN THROUGH-SUBSTRATE VIA PROCESS

Fig.1 shows a cross-sectional SEM image of a typical 91-μm deep GaN via-hole that was fabricated with an etch rate of 1.5 μm/min. The etching profile of the GaN via-hole has two different inclined sidewalls because of the etch back process of a Ni metal mask, which is closely related to the GaN/Ni etch selectivity [8]. The etching selectivity of GaN to Ni metal mask was 35, which was smaller than that of SiC etching (~100) [6]. Therefore, as shown in Fig. 2, it is necessary to increase the thickness of the conventional Ni etch stop. Ni with a thickness of at least 0.3 μm is required in view of the uniformity of the grinding and ICP etching of

the GaN substrate and the over-etching (10 µm). Therefore, a 0.5 µm-thick Ni etch stop structure was fabricated by electroplating. As a result, as shown in Fig. 2, the punch-through of the etch stop was not observed in the SEM observation after the GaN via etching.

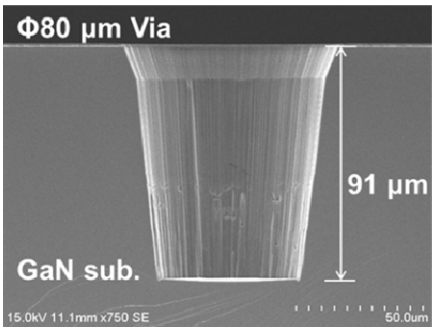


**Fig. 1** Cross-sectional SEM image of a typical 91-µm deep GaN via-hole [5].

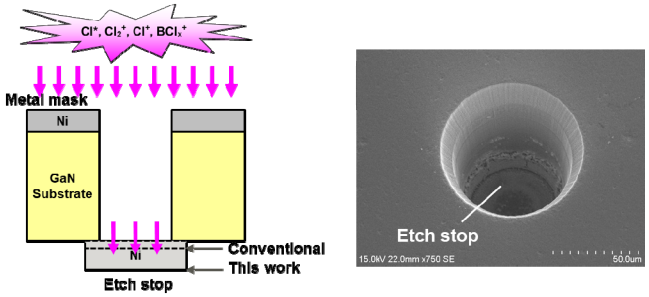


**Fig. 2** Cross-sectional schematic of etch stop structure in GaN substrate via etching and SEM image of etch stop.

Stealth dicing, which involves damaging the crystal with lasers, and then expanding the crystal to separate the chips, is very effective for dicing the GaN substrate [4]. However, to separate the chips, the metal on the dicing line must be removed. Therefore, we developed a metal removal process on the dicing line that uses wet etching. Fig. 3 shows the flow of the metal removal process on the dicing line and the optical micrograph of each process. Here, a process in which Au plating is not performed on the dicing line was performed [7]. First, patterning to open the dicing line was performed to expose the surface of the seed metal (2) for Au plating on the dicing line. Next, the seed metal (2) was etched to stop etching on the Ni surface. Finally, Ni and the seed metal (1) were sequentially etched until the GaN surface was exposed, and then the resist was removed.

Fig. 4 is a photograph of a processed wafer after peeling from supporting carrier and a schematic of the dicing layout. The dicing line is indicated by light blue lines. 5-mm square chips and long chips with different widths and a length of 5 mm were involved. Fig. 5 is a chip photograph after stealth dicing. By removing the metal on the dicing line, chips of different widths facing each other were precisely divided.

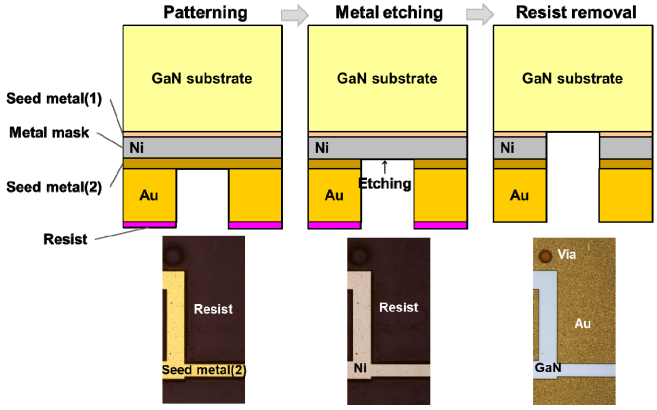


**Fig. 3** Metal removal process flow on the dicing line and optical micrograph of each process.

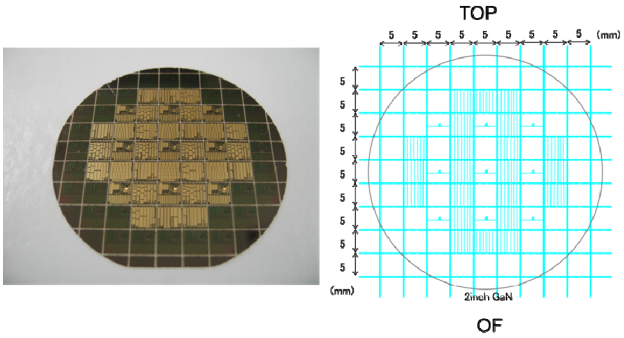


**Fig. 4** Photograph of a processed wafer after peeling from supporting carrier and a schematic of the dicing layout.

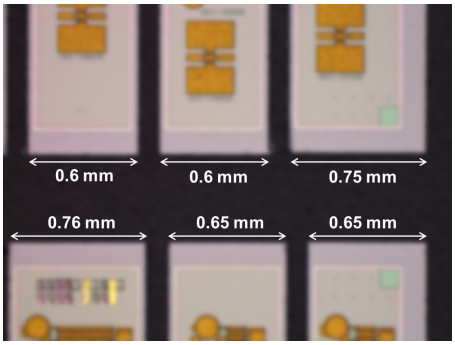


**Fig. 5** Chip photograph after stealth dicing.

Fig. 6 indicates the backside photograph of GaN-on-GaN HEMT PA chip (a), and GaN-TSV SEM image (b). A plurality of GaN-TSVs, which are Au plated from the back surface of the chip to the bottom surface of the etch stop, can

be seen. Fig. 7 shows the cross-sectional SEM image of GaN-TSV of GaN-on-GaN HEMT PA. A reliable connection between the etch stop and Au plating was also observed.

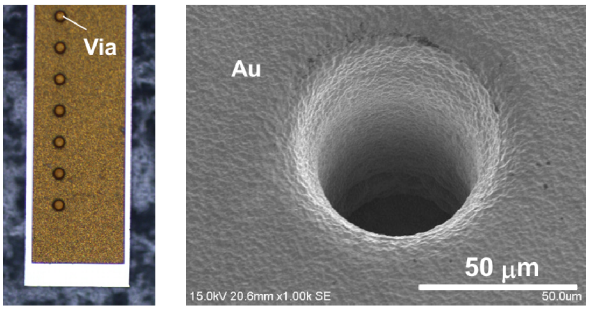


**Fig. 6** Backside photograph of GaN-on-GaN HEMT PA chip (a) and GaN-TSV SEM image (b).

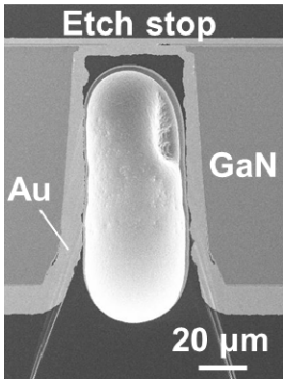


**Fig. 7** Cross-sectional SEM image of GaN-TSV of GaN-on-GaN HEMT PA.

## 50 W-CLASS GAN-ON-GAN HEMT POWER AMPLIFIER

GaN-TSVs were applied to GaN-on-GaN HEMTs having 20-nm AlGaN barriers with an Al composition of 26% [2]. Fig. 8 shows a GaN-on-GaN HEMT PA chip mounted on an evaluation board. The evaluation board performs harmonic treatment using an input matching circuit and an output matching circuit. The GaN-on-GaN HEMT PA chip has 36 gate fingers, with a gate length of 0.5 μm and a unit gate width of 300 μm, and has a gap of 30 μm between the gates. The total gate periphery was 10.8 mm. The input matching circuit and the gate electrode pad, and the output matching circuit and the drain electrode pad are respectively connected using wire bonding. The source electrode pads were connected to the ground on the back of the chip by GaN-TSVs.

Fig. 9 shows the high-frequency power characteristics of GaN-on-GaN HEMT PA with GaN-TSVs at 2.6 GHz. GaN-TSVs connected the source and the ground without failure, enabling high-power operation without oscillation. In pulse measurement at a pulse width of 10 μsec and the duty of 1%, a maximum output power ($P_{out}$) of 48.1 dBm (64.3 W), a maximum PAE of 71.1%, and a gain of 15.7 dB were obtained. On the other hand, in CW operation, a $P_{out}$ of 47.4 dBm (54.6 W), a maximum PAE of 63.3%, and a gain of 14.7 dB were obtained. The decrease in power and PAE during CW operation is due to the self-heating of the device. Fig. 10 shows a simulated comparison of the transient response characteristics of the maximum channel temperature of GaN-on-GaN HEMT PA between CW and pulse operations. As a result, the maximum channel temperature difference between CW operation and pulse operation is as large as 90 °C. However, enabling CW operation suggests that GaN-on-GaN HEMT PA has suitable heat dissipation properties.

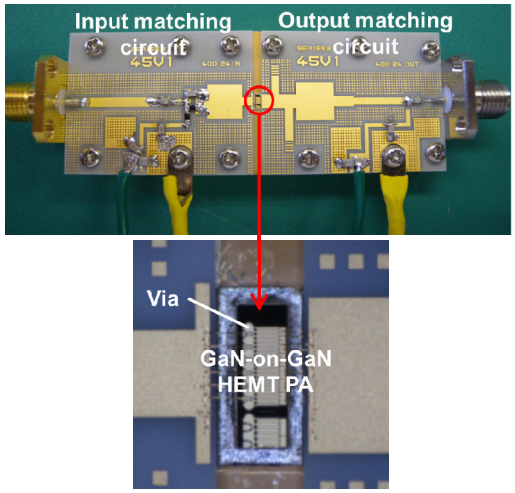


**Fig. 8** Photograph of 50 W-class GaN-on-GaN HEMT PA with matching circuits.

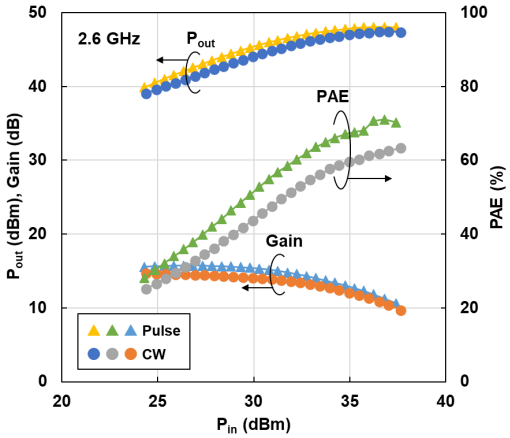


**Fig. 9** Power characteristics of GaN-on-GaN HEMT PA in pulse (closed triangles) and CW (closed circles) operations.

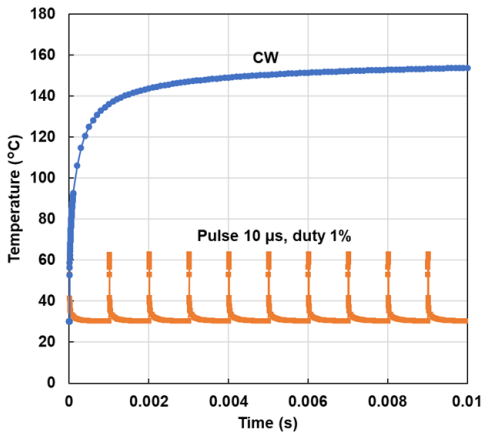


**Fig. 10** Simulated comparison of transient response characteristics of maximum channel temperature between pulse and CW operations.

## Conclusions

The authors studied the GaN-TSV process for GaN-on-GaN HEMT PAs, including using a thick Ni etch stop structure and a metal removal process on the dicing line. In GaN-on-GaN HEMT PAs, a reliable connection between the etch stop and GaN-TSV was observed using a cross-sectional SEM. The GaN-on-GaN HEMT PA exhibited excellent high-frequency power characteristics with a maximum $P_{out}$ of 47.4 dBm and a maximum PAE of 63.3% in CW operation, suggesting that it has appropriate heat dissipation characteristics.

## Acknowledgments

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## References

[1] Y. Kumazaki et al., *Remarkable Current Collapse Suppression in GaN HEMTs on Free-standing GaN Substrates*, 2019 BCICTS Conf., 10b.2.

[2] Y. Kumazaki et al., *An over 80% Power-Added-Efficiency GaN HEMT on free-standing GaN substrate*, Appl. Phys. Express 14, 016502 (2021).

[3] C. Mion et al., *Accurate dependence of gallium nitride thermal conductivity on dislocation density*, Appl. Phys. Lett. 89, 092123 (2006).

[4] N. Okamoto et al., *Backside Processing of RF GaN-on-GaN HEMTs Considering Thermal Management*, 2019 CS MANTECH Conf., 10.5.

[5] N. Okamoto et al., *High-rate ICP Etching for GaN Through-substrate Via of GaN-on-GaN HEMTs*, 2020 CS MANTECH Conf., 8.1.

[6] N. Okamoto et al., *SiC Backside Via-hole Process for GaN HEMT MMICs Using High Etch Rate ICP Etching*, 2009 CS MANTECH Conf., 7.1.

[7] N. Okamoto et al., *Backside Process Considerations for Fabricating Millimeter-Wave GaN HEMT MMICs*, 2010 CS MANTECH Conf., 15.1.

[8] N. Okamoto et al., *Deep GaN through-substrate via etching using $Cl_2/BCl_3$ inductively coupled plasma*, J. Vac. Sci. Technol. A 38, 063003 (2020).

## Acronyms

CMP: Chemical-mechanical polishing
HVPE: Hydride vapor phase epitaxy
ICP: Inductively coupled plasma
ISM: Industrial-scientific-medical
MOVPE: Metalorganic vapor phase epitaxy
PAE: Power-added efficiency
SEM: Scanning electron microscope
TSV: Through-substrate vias
VAS: Void-assisted separation

# Endpoint Detection Using OES in Via SiC / GaN Fabrication

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**Keywords: OES (Optical Emission Spectroscopy), High Density Plasma, SF6, O2, Ar , Endpoint**.

**Abstract**

**GaN-on-SiC technology backside processes is challenging due to SiC etching and process integration. SiC via etch processing is typically done in ICP-RIE tools using Ni or ITO mask with SF6/ O2 /Ar gas mixture to achieve higher etch rate. Typically, the SiC via etch process is done in 75 - 100 um SiC thickness. The OES end point detection being used in GaAs and Si technologies improves via yield and increases process capacity. SiC etching is based on time dependence trying to stop on the GaN layer. The OES technique usually depends on the ability of monitoring byproducts of the etch process to achieve endpoint. The main critical parameter is signal / noise ratio and it is related to hardware, minimum open area to be etched and etching algorithm. This work demonstrates etching SiC with high repeatability and precision stopping on the GaN layer, using optical emission spectroscopy (OES) endpoint detection.**

## 1. INTRODUCTION

Optical emission spectroscopy (OES) is a common method used in semiconductor technology during plasma etching processing for Endpoint detection (EPD). The method is based on measuring and tracking intensity changes in optical emission signals of the reactive species in the plasma over a period of time during the etch process. Typically, OES broadband wavelength is in the range of 200-1100 nm.

EPD methods using OES focus on identifying a single wavelength that corresponds to a chemical species in the plasma. When the etched layer is removed by the etching process, the concentration of reaction products from the etched layer is reduced and the intensity of specific wavelength will be reduced accordantly [1, 2, 3].

Typical Si / $SiO_2$ etch process uses fluorine gas mixture of $CF_4/O_2$, $SF_6/O_2$ but other combination like $C_2F_6/O_2$ could be found. In addition, Ar or $N_2$ can be added for mixture dilution or plasma stabilization. Typically, when OES is used for EPD detection the following wavelengths are being monitored: SiF (440.2 nm), $SiO_2$ (248.6nm), Si (505.6 nm), CO (482.5 nm). In this study, we have developed an EPD method for SiC etching based on following parameters: fraction of Ni mask open area and OES set up.

## 2. EXPERIMENTAL & RESULTS

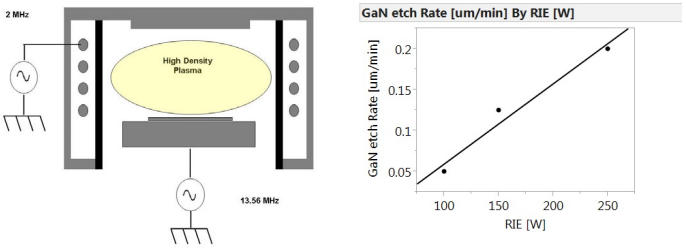



Fig.1. a) Plasma Therm ICP-RIE b) GaN etch rate vs RIE power

The SiC etch process done on a Plasma Therm ICP-RIE tool with upper 2 MHz power generator for plasma generation and bottom 13.56 MHz power generator to control DC bias voltage and OES detector. (Fig.1. (a)). The etch process is a twostep process, both steps using $SF_6$ /$O_2$/Ar gas mixture but the first process step uses higher RIE power to increase the physical mechanism of the etch process. The second process step reduces the RIE power in order to achieve better control and uniformity to stop on the GaN layer. The RIE power was pre-calibrated. Finally, it was set to 150 W. GaN etch rate vs. RIE power are shown in Fig. 1. (b)

In order to set OES wavelength to be monitored during the process, a seed layer was sputtered and ~ 4um Au electroplating was applied on the front side of 3" Si and SiC wafers, and each wafer was mounted on 4" perforated sapphire carrier.

All wafers were grinded to 50 um thickness and processed for full SiC etching using second etch process step parameters. During the last 10 min of the etching process the OES detector was switched on. In order to choose the wavelength with the higher signal difference between end to start, the wavelengths between 200-1100 nm were recorded. The signal of SiF (440.2 nm wavelength) was chosen for process monitoring, which is one the etching products that has and good signal difference. Shown in Fig.2

When SiF (440.2 nm wavelength) peak was significantly reduced, the process was manually stopped. Visual inspection of bare Si and SiC wafers revealed 100% etch. The above results showed good potential for making endpoint detection using SiF(440.2 nm) signal.

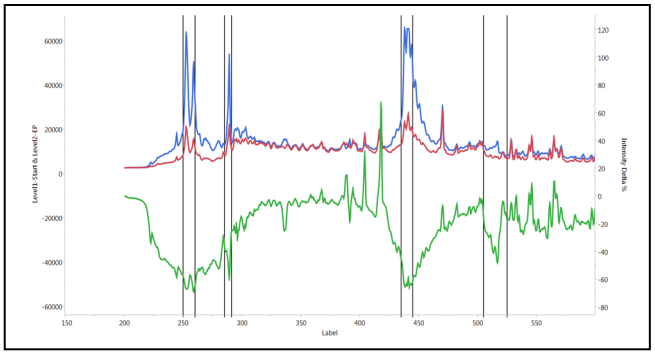


Fig.2. Bare SiC OES wavelength monitoring. **Blue** – Starting point signal, **Red** – end point signal, **Green** – delta (EPD – Start)

### 3. OES SIGNAL / NOISE CALIBRATION

In order to obtain high signal to noise ratio for EPD, the OES signals (200-1100 nm) were recorded for 3 different wafers: Si without mask (100% open area), SiC 100% open area & SiC with 2% opening area of Ni mask. All wafers had the same etching process parameters: ICP and RIE power, pressure, gas flow etc. While observing the difference of OES signature between 100% open area of Si (Blue) and SiC (Red), one can see intensity reduction of ~50% in the range of 200-330 nm wavelength, and ~33% in the range of 400-600 nm wavelength, shown in Fig 3.

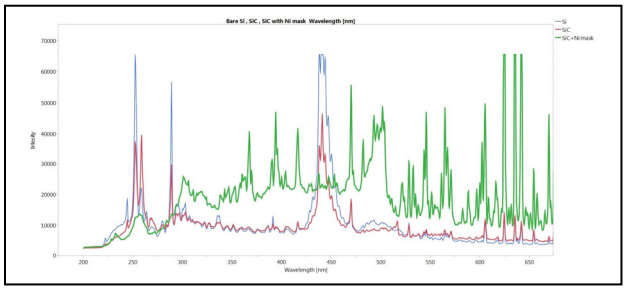


Fig.3. **Blue** – Start signal of OES on Si wafer, **Red** – Start signal of OES on SiC wafer, **Green** - Start signal of OES on SiC wafer with 2% open area.

This result probably was caused by the nature of byproducts related to crystal material differences (Si vs SiC). But when comparing 100% open area of SiC (Red) to 2% open area of SiC (Green), one can see signal reduction of ~ 75% in the range of 200-330 nm and 100% in the range of 400-600 nm, making endpoint detection using SiF(440.2 nm) impossible. On the other hand, tests with 20 % opening area of Ni mask were able to achieve good EPD, shown in Fig.4. Typical via open area is less than 1%, so in order to achieve good EPD it was clear that we have to increase signal to noise ratio. New hardware was installed and a new algorithm was developed for better sensitivity, those solutions helped to overcome the problem and make the EPD applicable.

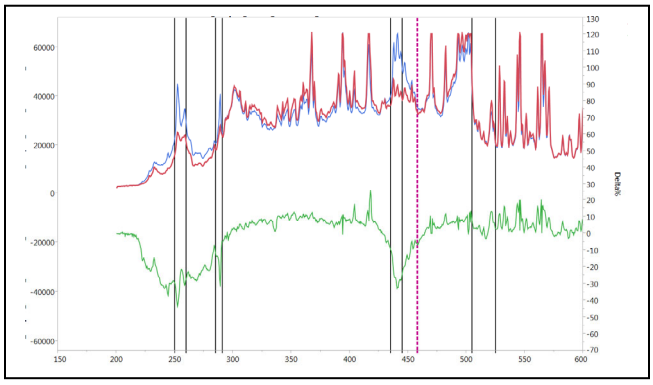


Fig 4. OES on SiC wafer with 20% open area, **Blue** – Starting point signal, **Red** - end point signal, **Green** – delta (EPD – Start).

### 4. RESULTS of NEW EPD PROCESS

100 mm SiC wafers with full front metallization were mounted on perforated sapphire, wafers then grinded to 100 um thickness and Ni masks (~10 um) with different open areas (down to 0.5% mask open area) were tested.

$SF_6$ / O2 gas mixture was used during the etching process and SiF (440.2 nm) was monitored, shown in Fig.5 and Fig.6. All wafers were passed visual inspection (VI) and showed 100% yield of stopping on the GaN layer, shown in Fig7.

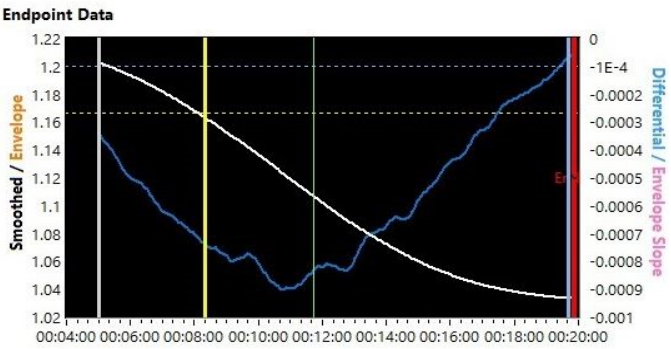



Fig.5 OES of 2.4 % open area during the etching process. **White** signal of new monitor function (f), Blue – df/dt

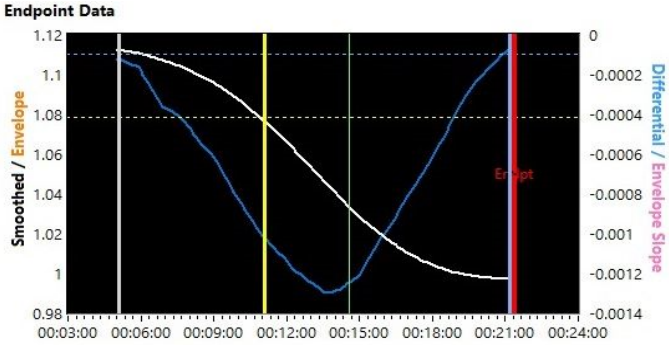
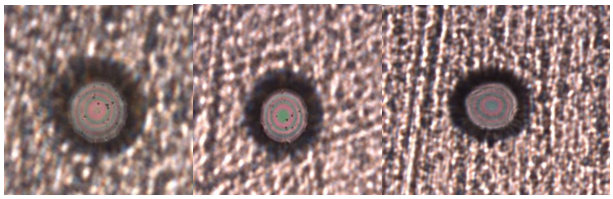



Fig.6 OES of 0.5 % open area during the process.
**White** signal of new monitor function (f), Blue – df/dt



a) Top b) Center c) Bottom

Fig. 7. EPD on 0.5 % opening, VI test across the wafer showing 100% yield stopping on the GaN layer.

## 5. CONCLUSION

In this study, we have showed the reduction of OES signals when Ni mask was applied on SiC wafer. New hardware was installed and a new algorithm was developed for better sensitivity. We successfully demonstrated that EPD using OES for a SiC via process can be achieved for Ni mask open area down to 0.5%.


## ACKNOWLEDGEMENTS

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## REFERENCES


[1] Kyounghoon Han, En Sup Yoon, Jaewon Lee, Heeyeop Chae, Kwang Hoon Han, and Kun Joo Park, "Real-Time End-Point Detection Using Modified Principal Component Analysis for Small Open Area SiO2 Plasma Etching"

[2] Ja Myung Gu, Paragkumar A. Thadesar, Ashish Dembala, Sang Jeen Hong, Muhannad S.Bakir, and Gary S. May, "Endpoint Detection Using Optical Emission Spectroscopy in TSV Fabrication"

[3] John G. Shabushnig, Paul R. Demko, and Richard N. Savage, "Application of Optical Emission Spectroscopy to Semiconductor Processing"

[4] Anthony Barker, Kevin Riddell, Huma Ashraf, Dave Thomas, Chia-Hao Chen, Yi-Feng Wei, I-Te Cho, and Walter Wohlmuth, "Advances in Back-side Via Etching of SiC for GaN Device Applications"

[5] Chia-Hao Chen, Yu-Wei Chang, Ming-Hung Weng, Ricky Chang, Shih-Hui Huang, Fraser Wang, Yi-Feng Wei, Stanley Hsieh, I-Te Cho, and Walter Wohlmuth, "Method for Forming Through Wafer Vias in GaN on SiC Devices and Circuits"

[6] Naoya Okamoto, Toshihiro Ohki, Satoshi Masuda, Masahito Kanamura, Yusuke Inoue, Kozo Makiyama, Kenji Imanishi, Hisao Shigematsu, Toshihide Kikkawa, Kazukiyo Joshin, and Naoki Hara, "SiC Backside Via-hole Process for GaN HEMT MMICs Using High Etch Rate ICP Etching".


## ACRONYMS

OES: Optical emission spectroscopy
EP: End Point
EPD: End Point Detection
SiC: Silicon Carbide

# Implementation of End Point Detection for Compound Semiconductor Wafer Thinning Applications and Investigation of Gallium Arsenide Etch Rates and Surface Roughness

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**Keywords: wet etching, gallium arsenide, etch stop layer, wafer thinning, bulk substrate removal, surface roughness, etch rates**

**Abstract**

**Accurate and precise control of wafer thickness is key to thermal management, packaging, and electrical performance. Recent trends for vertical cavity surface emitting laser (VCSEL), micro-light emitting diodes (µLED) and augmented reality (AR) applications show the need for greater process control. Two processes that drive development for these applications are wet etching a gallium arsenide substrate to a pre-determined thickness and completely removing the substrate. In this paper, the impact of etchant temperature on etch rate and surface roughness will be investigated for the first process. Completely removing the gallium arsenide (GaAs) substrate and stopping on an indium gallium phosphide (InGaP) etch stop layer using end point detection (EPD) will be demonstrated for the second process.**

## INTRODUCTION

Backside thinning a GaAs substrate from a starting thickness of 675 µm to a final thickness between 150 and 200 µm, without damaging the active side of the wafer, is a common approach to manufacture VCSEL devices. Deviations in the final substrate thickness can result in thermal, electrical, and packaging variabilities.[2] Thinning is typically achieved by mounting the device wafer to a carrier and grinding/polishing the backside until the desired final thickness is achieved. The grinding operation is typically followed by a wet etch to relieve residual stress in the wafer generated from the grinding process. An alternative approach to grinding/polishing is to thin the wafer to the desired thickness by wet etching[1]. This approach eliminates the mounting and grinding steps, resulting in a simpler process flow. The first goal of this paper was to demonstrate the impact of etchant temperature on GaAs etch rates and surface roughness.

A common alternative to targeting a final substrate thickness is wet etching to an etch stop layer. An etch stop layer with high selectivity to the GaAs wet etchant allows for the fast bulk removal of the substrate, protects the underlying epitaxial device layer and can be removed in a subsequent step. In a potential µLED process flow, transfer of the functional epi layers to an IC containing wafer can be achieved by wafer-to-wafer bonding and bulk GaAs substrate removal using this process.[3] Detection of this etch stop layer, indicating complete GaAs substrate removal, can be achieved using white light reflectometry end point detection and will be the second goal of this paper.

Single wafer wet etch tools provide advantages for these processes and several factors should be considered when selecting a tool. Compared to traditional wet benches or beaker level processing, single-wafer process equipment provides higher etch uniformities, more precise etch rates, and improved wafer-to-wafer consistency. Single-wafer process equipment also provides added benefits such as wafer-level end point detection, a feature not common on batch tools, which enables higher throughput and greater process control, further improving manufacturability. Here, a Veeco Instruments – Precision Surface Processing WaferEtch® 3302 single wafer etching system was used for all experimentation.

## EXPERIMENTAL SETUP

### *Chemistry*

A mixture of phosphoric acid ($H_3PO_4$, 85%), hydrogen peroxide ($H_2O_2$, 30%), and deionized water was used for the etchant. All chemicals were supplied by J.T. Baker and were of semiconductor/electronics grade.

### *Wafer type and film deposition*

Six inch diameter, n-type, semi-insulating, double side polished, 675 µm thick gallium arsenide substrates with crystal orientation (100) were used as the primary substrate for etch rate and surface roughness studies. These wafers were misoriented 2-degrees towards [110]. For the second application, a 300 nm thick layer of InGaP was used which was deposited at a rate of 38 nm/min onto the frontside of a GaAs (100) wafer, which was misoriented 15-degrees towards [111]. Here, a Veeco Lumina® MOCVD reactor was employed for the deposition using a 7 x 6" configuration carrier. The growth temperature was at 680°C and the pressure was at 42 torr using trimethylindium (TMIn), trimethylgallium (TMGa), trimethylaluminum (TMAl), $PH_3$ and $AsH_3$ as precursors. A 7 micron thick layer of gallium arsenide was then deposited on top of the InGaP at 100 nm/min to mimic a bulk layer. Using this approach avoided the bonding process and achieved the same end point detection result.

*Tool and recipe setup*

The temperature was controlled with a single heat exchanger to +/- 0.2°C and a constant flow rate of 1000 mL/min was maintained. The generic process flow for these experiments can be found in Table 1.

**Table 1**. Process flow for GaAs substrate etching.

| Step | Process | Time | Chemical | Speed (rpm) |
|---|---|---|---|---|
| 1 | Wet etch | 60 seconds | Acid mixture | 600 |
| 2 | Rinse | 20 seconds | DI water | 200 |
| 3 | Dry | 45 seconds | N/A | 1500 |

*Metrology*

Measuring the wafer thickness was performed on a Sentronics StraDex f24-300 sensor. The sensor performs the measurement by directing a laser at the substrate, upon which reflected light is detected from the top surface and refracted light is detected from the bottom surface. Film thickness can then be calculated from the interference pattern and the refractive index of the material. This sensor has a measuring wavelength of 1300 nm and a spot size of 24 µm. Gallium arsenide has an index of refraction of 3.66 at 1300 nm. Twenty-nine measurements were taken every 5 mm from -70 mm to 70 mm across the wafer diameter. These measurements were performed before and after etching. Radial measurements are more common in single wafer processing due to the rotational symmetry of spin processes.

*Uniformity*

Setup wafers were etched prior to this study to optimize the arm scanning profile in the wafer etch system, which directly impacts the etch uniformity. A linear arm scan (constant velocity at each arm scanning location) results in uniformities of approximately 10-15%, depending on the etchant, etchant temperature, and substrate. Hyperbolic motion allows the arm dispensing the etchant to change velocities while scanning across the wafer to ensure equal dwell time at each radial location. Without this feature, the etchant is dispensed for longer amounts of time at radii closer to the center of the wafer. Figure 1 is a graph showing the hyperbolic motion with the arm speeds used in this study to achieve an average uniformity of 2.6% non-uniformity at 50°C.

| Arm Position (mm) | Scan Velocity (mm/sec) |
|---|---|
| 4 | 125 |
| 12 | 123 |
| 20 | 119 |
| 28 | 113 |
| 36 | 105 |
| 43 | 96 |
| 51 | 86 |
| 59 | 74 |
| 67 | 62 |
| 75 | 50 |

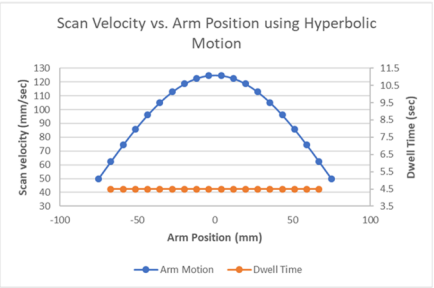


**Figure 1**. Hyperbolic motion of GaAs wet etching.

These values remained constant throughout the study to directly observe the impact of etchant temperature on etch rate and surface roughness. The arm scan is symmetrical with the same speeds used at the negative radial positions. For wafers with significant incoming thickness issues from previous processing steps, a custom arm scanning profile can be created in the software to further improve the uniformity.

*Surface Roughness*

A KLA Tencor P16+ stylus profile was used to acquire the surface roughness measurements. The profilometer setup used a 2.0 µm stylus radius, 400 µm scan length, 20 Hz sampling rate, 5 µm/sec scan speed, 2.00 mg applied force 60° stylus angle and 25 µm long wavelength cutoff. Five surface roughness scans were taken along the wafer radius every 14 mm and averaged together. The surface roughness was also investigated with a Bruker Dimension FastScan AFM, which yielded comparable numbers. Surface topography images provided below were captured with the AFM. Arithmetic average (Ra) was the roughness value used.

RESULTS

*Etch Rates*

Below is a sample dataset from experiments done to investigate the etch rate at 35°C for a one minute process (Table 2). The pre-etch wafer thickness and post-etch wafer thickness measurements are given at each diameter location. The difference between the two is the amount etched at that location. Each etch rate tests were repeated five times and the average delta across all 145 points determined the etch rate.

**Table 2**. Sample dataset of wafer thicknesses before and after etching at 35°C.

| Diameter location (µm) | Pre Etch (µm) | Post Etch (µm) | Delta (µm) |
|---|---|---|---|
| -70000 | 608.902 | 594.104 | 14.798 |
| -65000 | 609.546 | 594.905 | 14.641 |
| -60000 | 609.895 | 595.409 | 14.486 |
| -55000 | 610.121 | 595.810 | 14.311 |
| -50000 | 610.225 | 595.967 | 14.258 |
| -45000 | 610.591 | 596.210 | 14.381 |
| -40000 | 610.713 | 596.297 | 14.416 |
| -35000 | 610.696 | 596.263 | 14.433 |
| -30000 | 610.696 | 596.019 | 14.677 |
| -25000 | 610.382 | 595.792 | 14.590 |
| -20000 | 609.947 | 595.305 | 14.642 |
| -15000 | 609.668 | 594.817 | 14.851 |
| -10000 | 609.512 | 594.556 | 14.956 |
| -5000 | 611.131 | 596.733 | 14.398 |

| Diameter location (µm) | Pre Etch (µm) | Post Etch (µm) | Delta (µm) |
|---|---|---|---|
| 0 | 610.861 | 596.385 | 14.477 |
| 5000 | 610.591 | 596.036 | 14.555 |
| 10000 | 609.355 | 594.591 | 14.764 |
| 15000 | 609.703 | 594.887 | 14.816 |
| 20000 | 610.086 | 595.462 | 14.624 |
| 25000 | 610.400 | 595.862 | 14.538 |
| 30000 | 610.592 | 596.141 | 14.451 |
| 35000 | 610.783 | 596.419 | 14.364 |
| 40000 | 610.800 | 596.471 | 14.329 |
| 45000 | 610.643 | 596.367 | 14.276 |
| 50000 | 610.434 | 596.071 | 14.363 |
| 55000 | 610.173 | 595.775 | 14.398 |
| 60000 | 609.912 | 595.375 | 14.537 |
| 65000 | 609.494 | 594.887 | 14.607 |
| 70000 | 609.233 | 594.556 | 14.677 |

As with most wet etchants, there is an exponential increase in etch rate with etchant temperature and that trend holds true with this study (Figure 2).

An average etch rate of 6.37 µm/min was obtained with an etchant temperature of 20°C, 14.56 µm/min with 35°C etchant and 27.73 µm/min with 50°C etchant. Fitting these values to an exponential regression gave the equation below and a $R^2$ value of 0.9949, indicating an accurate fit and trend.

$$y = 2.463e^{0.049x}$$

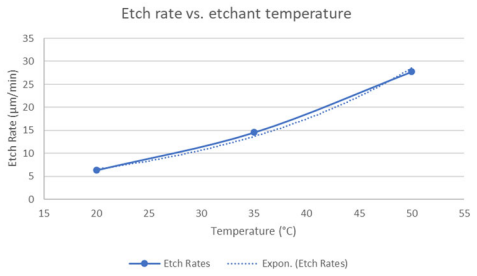


**Figure 2**. GaAs average etch rates at 20°C, 35°C, and 50°C etchant temperatures.

*Etch Uniformity*

Etch uniformities are also of great importance, especially when considering the selectivities of the etch stop layer etch rate to the bulk wafer thickness etch rate. Uniformities were calculated for each of the five runs at each etchant temperature and are given below (Table 3).

**Table 3**. Etch uniformities at 20°C, 35°C, and 50°C etchant.

| Temperature | 20°C | 35°C | 50°C |
|---|---|---|---|
| **Run 1** | 3.56% | 2.76% | 2.80% |
| **Run 2** | 2.30% | 2.40% | 2.82% |
| **Run 3** | 2.80% | 1.83% | 2.44% |
| **Run 4** | 2.47% | 1.76% | 2.59% |
| **Run 5** | 2.37% | 1.76% | 2.25% |

*Surface Roughness*

The average roughness from the five radial surface roughness scans taken on the stylus profilometer are given below (Table 4). There is a clear trend of increasing roughness with increasing etchant temperature.

**Table 4**. Surface roughness values before and after etching using a stylus profilometer.

| Etchant Temp. (°C) | Before Etch Roughness (nm) | After Etch Roughness (nm) |
|---|---|---|
| 20°C | 1.108 | 2.619 |
| 35°C | 0.962 | 4.043 |
| 50°C | 1.008 | 8.987 |

Three scans were taken along the radius of the same wafers using an AFM and the average roughness values are given below (Table 5). Direct comparison of 1-D and 2-D surface roughness measurements are not possible, but the trends of increasing surface roughness with increasing etchant temperature was confirmed

**Table 5**. Surface roughness values before and after etching using an AFM.

| Etchant Temp. (°C) | Before Etch Roughness (nm) | After Etch Roughness (nm) |
|---|---|---|
| 20°C | 1.22 | 2.69 |
| 35°C | 1.23 | 7.37 |
| 50°C | 1.25 | 14.89 |

AFM topography images show the initial pre-etched, low roughness surface (Figure 3, left) and an image from the 20°C etched wafer (Figure 3, right).

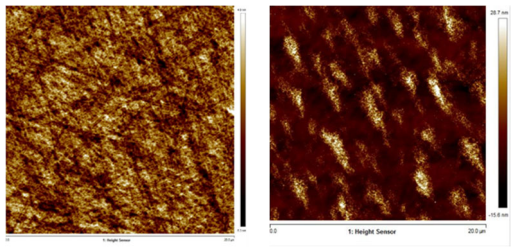

**Figure 3**. GaAs etch rates at 20°C, 35°C, and 50°C etchant temperatures.

In addition to the stylus profilometer and AFM roughness measurements, the topology of the post-etch surface was inspected in a SEM (Figure 4).

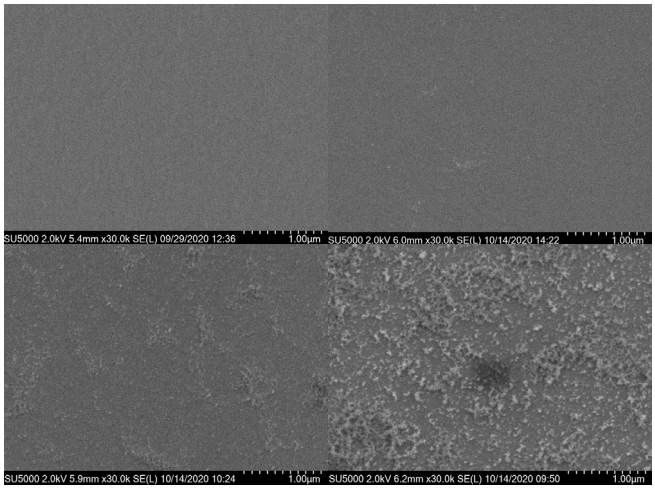

**Figure 4**. SEM image of GaAs surface etched at 20°C (top right), 35°C (bottom left), 50°C (bottom right) and a control without etching (top left).

The top left image of Figure 4 shows an unetched wafer with no discernable topology. The other three images show that the roughness is not uniform after etching, indicating some areas could yield low roughness values even though surrounding areas could be rough and vice versa.

The profilometer surface roughnesses were then plotted against etchant temperature so a comparison could be made to etch rate (Figure 5). Applying a linear regression fit to the data produced a $R^2$ value of 0.907. Modifying the fit to a 2nd order polynomial gave a fit of 1, but more data is needed to verify this fit.

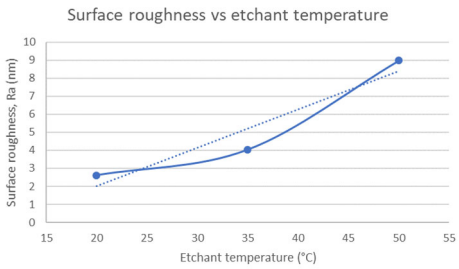


**Figure 5**. Surface roughness values at 20°C, 35°C, and 50°C etchant temperatures.

The surface roughness observed is attributed to the formation of a film, rather than porosity of the wafer surface, based on the morphology observed in the SEM images. This film was theorized to be a gallium oxide or arsenic oxide. One of the 50°C samples, with significant surface roughening due to the film, was exposed to phosphoric acid as a solution to remove the film. Surface roughness values were obtained after exposure to phosphoric acid and the values are given below (Table 6). These five measurements were taken radially on the same wafer, which was etched at 50°C. The post phosphoric acid treatment surface roughness values are much closer to the before etch roughness measurements.

**Table 6**. Surface roughness values before etching, after etching, and after phosphroic acid treatment.

| Radial Measurement # | 1 | 2 | 3 | 4 | 5 | Average |
|---|---|---|---|---|---|---|
| Pre wet-etch | 1.046 | 1.011 | 0.986 | 0.995 | 1.001 | 1.008 |
| Post wet-etch | 3.132 | 10.605 | 7.796 | 7.964 | 15.440 | 8.987 |
| Post phosphoric exposure | 1.902 | 1.791 | 1.809 | 2.383 | 2.362 | 2.049 |

*End Point Detection*

All the above is pertinent to the first goal of this paper where a certain wafer thickness is desired. When the entire GaAs substrate is to be removed, the end point detection of an InGaP etch stop layer can be utilized to ensure consistent wafer-to-wafer processing. The EPD system on the WaferEtch® 3302 system continually monitors the RGB (red, green blue) and HSV (hue, saturation, value) color spaces while the wafer is being etched. Once the software detects a significant change in any of these channels, the wafer is immediately quenched with deionized water to stop the etch process.

In this particular process of bulk etching a GaAs wafer and stopping on a layer of InGaP, the hue channel (yellow line, Figure 6) demonstrated the most significant end point signal. A hue value of approximately 60 bits is obtained from sample numbers 1 to 8 while the wafer is being etched. As soon as the GaAs layer is etched through, the hue channel increases to approximately 210 bits indicating the etch is complete.

The other channels (red, green, blue, saturation, and value) did not show a significant end point signal in this particular application but are known to work well in other applications such as copper under bump metallization (UBM) etching. The advantages of using an EPD system is that it can account for wafer thickness variations from the manufacturer and can be used as an indicator of when the etchant needs to be replenished or replaced.

**Figure 6**. End point detection of InGaP etch stop layer.

## CONCLUSIONS

The characterization of surface roughness and etch rates as a function of etchant temperature was successfully demonstrated on gallium arsenide wafers using a phosphoric acid/hydrogen peroxide mixture. A maximum gallium arsenide etch rate of 27.73 µm/min was achieved at a temperature of 50°C. A custom arm scan profile was used to achieve etch uniformities of 3% and lower at 20°C, 35°C, and 50°C. The surface roughness (Ra) increased to a maximum of 15.440 nm after exposure to 50°C etchant but this was attributed to the formation of a film on the surface. It was shown that exposure to phosphoric acid can remove this film and the surface roughness decreases back to a value more comparable to the starting roughness value.

End point detection of an InGaP etch stop layer was demonstrated when bulk etching a GaAs substrate. This setup enabled consistent removal of the GaAs wafer without etching through the InGaP etch stop layer and potentially damaging the epitaxial layers. Other applications such as substrate stress relief and alternative material etching (GaN, AlGaAs, InP, InGaAsP, etc.) are possible but outside the scope of this paper. Future studies will investigate the oxide formation in more detail.

## REFERENCES

[1] Seurin, Jean-Francois & Khalfin, et. al. (2013). High-power red VCSEL arrays. Proceedings of SPIE - The International Society for Optical Engineering. 8639.

[2] Choi, J.H. & Wang, L. & Bi, Hai & Chen, Ray. (2006). Effects of Thermal-Via Structures on Thin-Film VCSELs for Fully Embedded Board-Level Optical Interconnection System. IEEE Journal of. 12. 1060 - 1065.

[3] Zhang, L., Ou, F., Chong, W. C., Chen, Y., & Li, Q. (2018). Wafer-scale monolithic hybrid integration of Si-based IC and III-V epi-layers. Journal of the Society for Information Display, 26(3), 137–145.

# A Systematic Approach for Determining Overlay Spec Limits in Photolithography

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**Keywords: Overlay Measurement, Misalignment, Spec Limits, Stepper**

**Abstract**

**A systematic way to determine the photomask overlay spec limits by using a new overlay measurement structure is discussed in this paper. The results show that this novel artifact enabled us to automatically obtain reliable and accurate overlay measurements, monitor in-line overlay, conduct stepper alignment corrections, and establish the relationship between the misalignment and parametric test parameters. By implementing the stepper alignment corrections, the overlay control can be further improved by 30%, which ensures enough margin for high volume production.**

## INTRODUCTION

With increasing demands to improve the performance of HBT and pHEMT technologies and reduction in the die size for cost savings, critical dimension (CD) and overlay control in the photolithography module become more and more important. Errors in the overlay of different lithography layers can directly cause issues such as: photo rework, extra processing steps and cycle time, parametric test failures, yield loss, device performance implications, reliability concerns, and wafer scrap. However, the alignment vernier widely used has become less useful. That is because the accuracy and repeatability of reading the alignment vernier manually is quite poor. As a result, continuous improvement in overlay measurement and control is required.

In this paper, the impacts of the misalignment were analyzed. A new overlay measurement structure has been defined and implemented. An effective way to determine the overlay spec limits is discussed. The results showed the new overlay artifact provided a robust solution to improve the stepper alignment performance and made an improvement in overlay margin sustainable during high volume production.

## BACKGROUND

In general, there are five major steps in photolithography. First is substrate preparation, then photoresist spin coat and soft bake, alignment and exposure of wafers on the stepper, after which comes post-exposure bake and development [(1)]. The last and critical step is post-develop-inspection, where it is determined whether the previous steps have been performed correctly and detects if the photo process yields correct critical dimensions (CDs) and good overlay. Figure 1a. shows a cross-section of a good device with perfect Via CD and overlay between layers Emitter and Via, and a bad device with oversize CD and misalignment is shown in Figure 1b. The oversize Via and misalignment resulted in the Via falling off the emitter metal, which caused die sort (DS) yield loss and reliability failures. At photo inspection step, if we can detect this kind of issue and rework the affected wafers, the yield loss can be avoided.

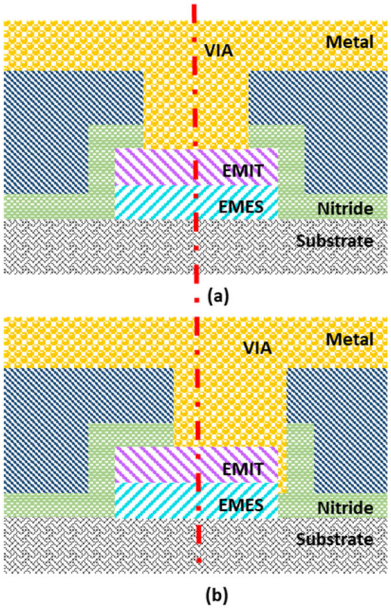


Fig. 1a. A good device with perfect CD and overlay. 1b. A bad device with oversize CD and misalignment.

Here is an example showing how the alignment affects the die sort yield (see Figure 2). The major DS yield detractor was leakage failing high. The overlay errors had dramatic impacts on the die sort test. The DS yield loss due to the misalignment on this wafer was close to 30%.

In order to better control the photo process, in addition to the critical dimensions, a successful overlay control is an essential requirement for the final performance of the devices and a critical step for maintaining a high level of yield in a wafer fab. The key point for the overlay control is to obtain accurate and precise measurement for overlay. Next, the

effective measurement of overlay errors and setting of practical limits will be discussed.

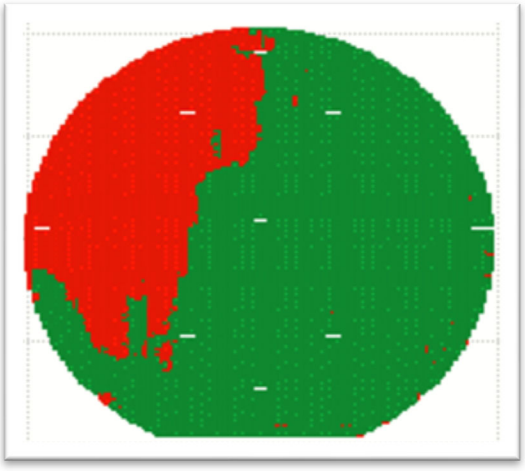

Fig. 2. Die sort yield loss (red) due to misalignment.

## Description of CD and Overlay Structure

In the past, the overlay error was checked by visually reading the alignment vernier. However, numerous factors impact the manual vernier reading. Examples include microscope focus, magnification, and the person performing the measurement. It is difficult to get repeatable and accurate measurements by reading the alignment vernier. To eliminate these inconsistencies in measurement, a new metrology structure has been developed and used for automatic CD and overlay measurement by using IVS metrology system made by Inspectrology. A typical module of the new metrology row contains 1) Label, 2) CD mark, 3) Focus Mark, and 4) Overlay mark. This in-line monitoring structure for CD measurement has been implemented and proved that the measurement deviation between the standard CD artifact and the real device can be dramatically minimized [(2)]. How to obtain reliable and accurate overlay error measurements will be discussed in the subsequent sections.

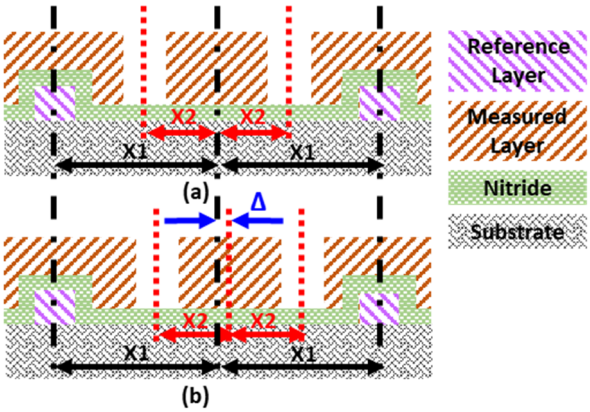


Fig. 3a. Measured and reference layers have perfect alignment. 3b. Measured and reference layers has misalignment Δ.

A standard overlay mark is shown in Figure 3. The top cross-section in Figure 3a. shows the reference layer (RL) and measured layer (ML) has perfect alignment. X1 and X2 are half the distance between the center lines of the reference features and the center lines of the measured features, respectively. The center lines of the two layers coincide. Figure 3b. shows there is a misalignment between the two layers. The center line of the measured layer has a translation error delta (Δ) in x-direction, which is called the overlay error or misalignment. The overlay error is then calculated by determining the value of the difference between the coordinates of the center line of the RL to the ML.

## Results and Discussions

To pursue device performance enhancement and additional die per wafer, the feature sizes on the chip keep shrinking to decrease the capacitance, increase the gain and Fmax, and reduce the die size. At the same time, the layout design rule (LDR) between key layers is becoming more compact, such as Base-Emitter spacing, overlap between the Via and the underlying conductor, etc. This imparts huge challenges to photolithography. Next, how to implement the new overlay measurements, which enables the development of a robust process to systematically evaluate the new LDR and also determine the alignment spec limits which will improve the overlay control, will be explained.

The alignment margin experiments have been designed and performed on ASML steppers by using a mask with a new LDR and the overlay marks added. All-field overlay measurements with 5 locations (center and 4 corners) within a printfield were conducted on all wafers on the IVS metrology system. The rest of the process was unchanged. The overlay errors, PCM and Die sort data have been reviewed and analyzed.

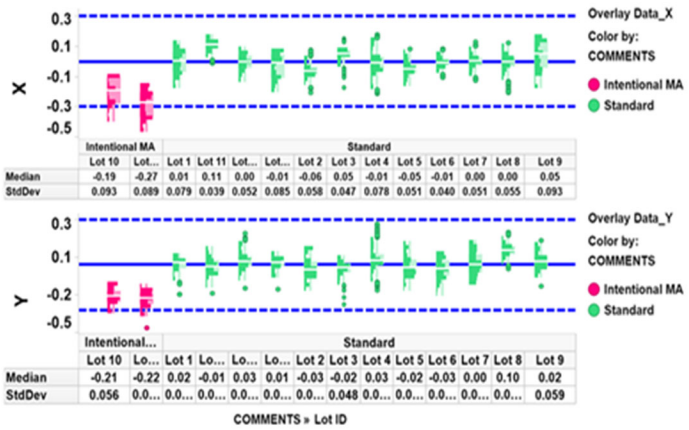


Fig. 4. An example of the overlay trend chart in X and Y directions on different lots.

An example of the overlay trend chart in X and Y directions on different lots is shown in Figure 4. Lots with the intentional

misalignment are shown in red. It was proven that the overlay errors could be found by using the new measurement approach. Therefore, the misalignment of the production lots can be well monitored.

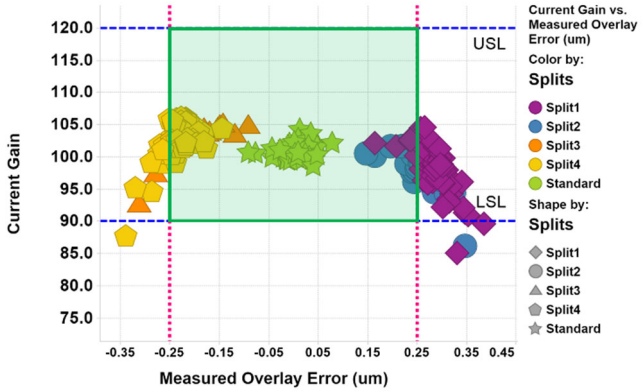


Fig. 5. The relationship between the measured overlay error and the current gain

After combining the overlay, PCM and DS data, the results show a relationship between the overlay errors and electrical test parameters. This relationship between the measured overlay error in X-axis and the current gain in Y-axis has been summarized in Figure 5. The upper spec limits (USL) and lower spec limits (LSL) for the current gain are 120 and 90 respectively. The range of alignment is from -0.35µm to +0.35µm. It can be seen clearly from Figure 5 that when the overlay error is within -0.25µm to 0.25 µm, the current gain is stable. However, it starts to roll off once the absolute value of overlay error is greater than 0.25µm. Based on the plot shown in Figure 5 and considering the current gain stability, data outside the green box should be avoided, and the misalignment must be controlled within ±0.25µm. Therefore, to meet the requirements of the new LDR, the USL and LSL for alignment should be +0.25µm and -0.25µm separately.

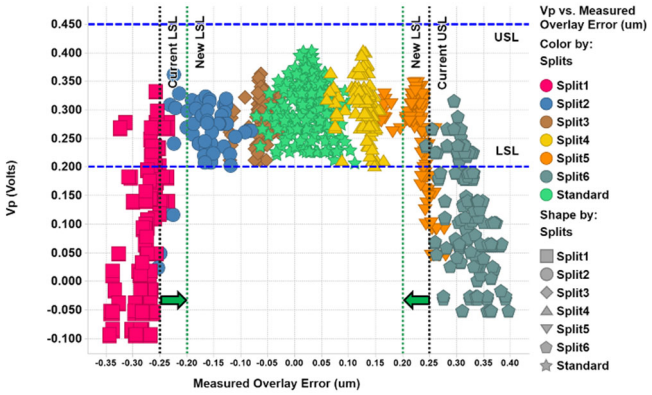


Fig. 6. The relationship between the measured overlay error and the pinch-off voltage Vp

This approach also has been used to evaluate the existing overlay spec limits. Pinch-off voltage (Vp) of pHEMT transistors is one of the key test parameters driving PCM and die sort yield. Experimental results in Figure 6 show that Egate misalignment to the wide recess (WRCS) layer (X-axis) affects Vp strongly. Vp rapidly exceeded the LSL when the overlay errors were greater than |±0.23|µm, and significant yield loss was observed. Based on the data shown in Figure 6, the current overlay spec limits of ±0.25µm would not allow acceptable process capability between Egate and WRCS alignment. Tightening the overlay spec limits from ±0.25µm to ±0.20µm is needed. The new overlay spec limits of ±0.20µm ensure that the alignment between Egate and WRCS has enough process window and yield loss can be prevented. The overlay control is critical for shipping lower PPM levels of defective die to customer. Many products depend on the overlay control to maintain good yield.

However, the capability of the tool platform only can support overlay errors from -0.30µm to 0.3µm. Running 7x24 production on steppers and controlling the misalignment ≤ |±0.25|µm seems impossible. To improve the overlay control, a team collaborated to work on the stepper alignment correction project. By analyzing the overlay data, calculating the inter-field and intra-field correction terms, and feeding back the corrections to stepper, not only the alignment requirements of ±0.25µm were met, but also allowed further tightening of the control limits for overlay error from ±0.25µm to ±0.2µm, which improved the overlay control by about 30%.

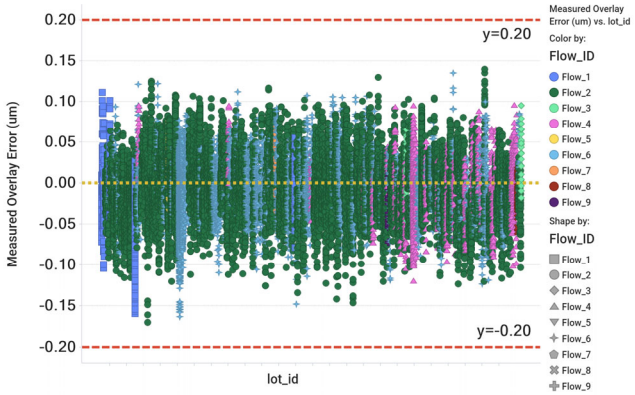


Fig. 7. The trend chart for overlay measurements

Implementing the stepper corrections, ensured that ample alignment margin in high volume manufacturing was obtained. This is demonstrated in Figure 7, which shows the overlay errors measured on 547 lots and 9 different process flows. All the individual measurement points are within the limits of |±0.20| µm. There was no rework due to misalignment. The results prove that the stepper alignment correction not only doesn't add additional production burden and increase photo rework rate, but also improves the overlay control and yield.

This paper has presented a systematic approach for determining the alignment spec limits. This allowed the limits to be set more accurately, effectively, and meaningfully. It has also been proven that the developed process ensures sufficient margin for high volume production.

## Conclusions

This work has proven that the newly developed overlay measurement structure can be used for obtaining accurate and repeatable measurements, monitoring the in-line overlay, building the correlation between the overlay error and parametric test values, and establishing of the alignment spec limits effectively. In addition, significantly improved stepper alignment performance was demonstrated by the use of this novel feature. The overlay error control limits can be tightened by 30% from ±0.3µm to ±0.2µm. The results showed running 7x24 production on steppers and controlling the misalignment within ±0.20µm is feasible and practicable. This systematic and thorough alignment margin study ensures that the developed process is robust for manufacturing, yield and reliability.

## Acknowledgements

Special thanks to Dana Schwartz, Pronab Das, Peter Moon and Jinhong Yang for valuable discussions. Also thank John Tils for data collection support.

## Reference

[1] C. Mack, 2012, *Fundamental Principles of Optical Lithography: The Science of Microfabrication*, Wiley, (Chichester, UK).

[2] C. Wang, et al., Effective In-Line Monitoring Structures for Critical Dimension Measurement in Photolithography, 2015 GaAs MANTECH Technical Digest, pp. 221-224, May 2015.

## Acronyms

HBT: Hetero-junction Bipolar Transistor
pHEMT: Pseudomorphic High Electron Mobility Transistor
CD: Critical Dimension
PCM: Process Control Module
DS: Die Sort
LDR: Layout Design Rule
USL: Upper Spec Limit
LSL: Lower Spec Limit

# Uncovering Process Interdependency Using Data Mining

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**Keywords: Advanced Data Analytics, Root Cause Analysis, Process Queue Time, Recipe Interaction**

## I. Background

Semiconductor manufacturing processes are complex, and so are issues related to them. The root cause of some of these process issues cannot always be accurately identified by analyzing only parameters linked to an individual production run. In some cases, an engineer must look beyond the current production environment to determine whether secondary factors such as equipment operation from a previous run or equipment idle time between runs could possibly create interdependencies that adversely affect the quality of the active production run.

## II. Process Interdependency Examples

For example, if two dissimilar recipes were executed contiguously with the same piece of equipment (recipe A first, then recipe B), it is possible that the first set or sets of production wafers from the latter recipe (recipe B) could experience quality issues if the proper re-conditioning of chamber parameters were not performed. In semiconductor manufacturing where process precision is extremely critical, parametric variation caused by carryover effects like this would more than likely result in product quality problems. Similarly, timing-related elements, like equipment idle time or wafer queue time, could also adversely influence the environmental parameters of process chambers and cause production issues. These are all elements of process interdependencies that should not be overlooked when performing root cause analysis.

## III. Root Cause Analysis of Interdependency Issues

The traditional approach in root cause analysis examines only data from the specific process run that is directly related to a quality or yield event. While this might be an effective approach to solving a number of issues, it is not effective in identifying root causes for issues due to interdependency. Only with a broader examination of process and engineering data beyond the targeted process run could interdependency issues be discovered.

Advanced data analytic tools provide a platform for engineers to expand the scope of root cause analysis to include engineering data that signal potential interdependent effects. This enables a more thorough and insightful assessment of failure events. Whether it is process queue time, system downtime, or recipe interaction data, with an advance analytic solution, engineers can quickly and Intelligently identify its correlation to process impact.

## IV. Case Study 1

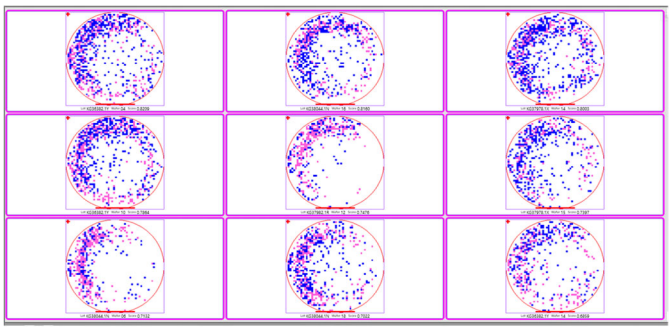

Figure #1 – Examples of wafers affected by the edge crescent-shaped low yield pattern

In the first case study, multiple lots were seen to be impacted by an edge crescent-shaped failure pattern - Soft Bin103 and Bin104 (Figure #1). Over 2% of the wafers in the 193 lots processed were affected by this pattern. A secondary analysis was performed comparing the affected wafers against the rest to determine the root cause. To increase the comprehensiveness of the analysis, along with the related FDC data, other interdependency variables such as process time, wait time, and recipe information were also included as cause variables to be examined (Figure #2).

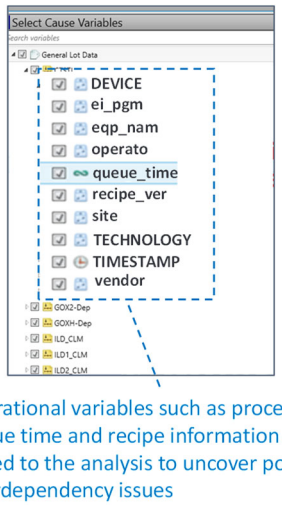


Figure #2 – Increasing analysis comprehensiveness by including potential interdependent variables

Modern root cause analysis solutions allow the inclusion of any operational and engineering variables including process stages tracking data, queue time, recipe versions, technology variables, and timestamp variables for analysis to assure that interdependency issues are not overlooked. In this example, with the addition of operational parameters as potential cause variables, the advanced data mining application easily pinpointed a high-potential root cause candidate – process queue time. All affected wafers had an abnormally high Process Queue Time of > 4.89sec during a specific oxide wet bench process step (Figure #3). Further offline investigation found that there was an equipment shutdown at this process step that caused high queue time. This information helps to identify an interdependency issue and narrow the scope of investigation for the engineer.

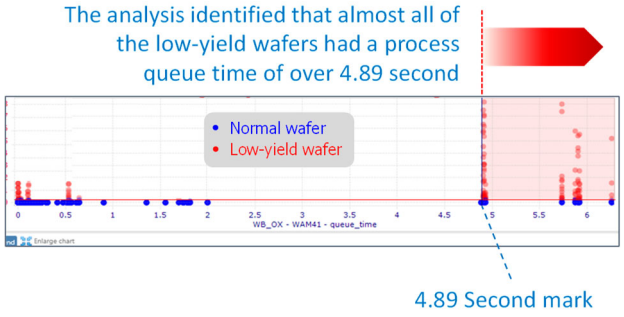


Figure #3 – Dependency analysis easily identified process queue time to be a low-yield factor

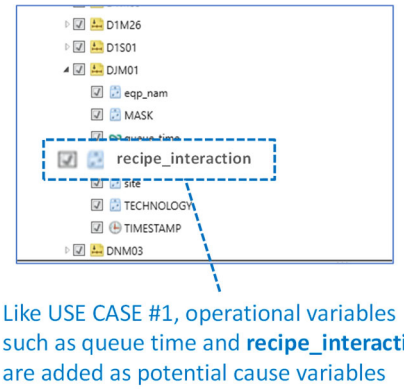


Figure #4 – Operational variables such as recipe_interaction is key to identifying the root cause in case study #2

## V. Case Study 2

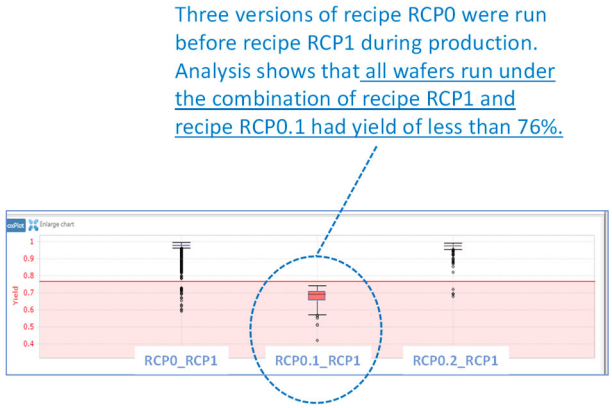


Figure #5 – An issue related to recipe interaction identified by dependency analysis

In the 2nd case study, a large number of wafers (277) were shown to have abnormally low yield of < 76%. A total of 6,681 wafers were queried for analysis, comparing the 277 low-yield wafers versus the remaining higher yield counterparts. Similar to CASE STUDY 1, in addition to the related FDC data, interdependency variables such as process tracking variables, queue time, and recipe_interaction, were included as potential cause variables (Figure #4).

Again, the advanced data mining solution quickly pinpointed an interdependency issue related to recipe sequencing during process stage: MET1 Dep and Sub-step: DJM01. During this process step, three slightly different versions of recipe RCP0 were executed prior to the processing of recipe RCP1. Analysis shows that every wafer processed under the combination of recipe RCP0.1

and recipe RCP1 had lower yield - under 76% (Figure #5). This provided engineering the necessary insight to further investigate. Subsequent offline investigation found that in the month of April 2019, a Metal1 adhesion layer thickness deposition evaluation was performed, and further Failure Analysis results validated the issue was caused by the recipe interaction of the metal deposition recipe RCP1 and prior adhesion layer deposition recipe RCP0.1.

## VI. SUMMARY

- When performing root cause analyses, it is important to look beyond the parameters within the active product run. Factors such as carryover effect and other environmental interdependencies should be considered for a more thorough investigation.
- Advanced data analytic solutions can help engineers expand the scope of analysis allowing them to identify root causes of interdependency-related issues more quickly and efficiently.

# Electrostatic discharge (ESD) in AlGaN/GaN HEMT due to fabrication process

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**Keywords: GaN, AlGaN, HEMT, ESD, Process**

**Abstract**

**GaN transistors have the capability of working with high voltage and high current, and GaN may be considered as ESD immune material. In this paper we shall review the root cause analysis of electrostatic discharge (ESD) defect formation and defect characterization in AlGaN/GaN HEMT wafers. An Atomic Force Microscopy (AFM) and a Focused Ion Beam Scanning Electron Microscope (FIB-SEM) cross-section revealed damage on the surface of the wafer, cracks through SiN passivation and into the AlGaN/GaN substrate. Root cause analysis investigation shows the ESD damage was formed in an automated wet chemistry fabrication process tool. An ESD formation mechanism was proposed, and its characterization and a solution to avoid it are suggested.**

## INTRODUCTION

Electro static discharge (ESD) is a rapid discharge event that transfers a finite amount of charge between two bodies at different potentials [1]. The amount of damage experienced in an integrated circuit (IC) is governed by the current densities and voltage gradients developed during the event. The movement of these charges occurs very rapidly, leading to high currents. When the current passes through an object, the impedance of that object establishes a voltage across it. The voltage establishes an electric field in the surrounding objects based on the geometry and dielectric material present in the structure. Both high current densities and high electric fields cause damage on semiconductor devices.

AlGaN/ GaN high electron mobility transistors (HEMT) are being use for high power application in RF frequency. Two important physical property of GaN is high critical electric field (~3.4MV/cm) and high electron concentration (~1e13 $cm^{-2}$). Those properties enable high breakdown voltage and high current density, which gives the possibility of generating high RF power in the transistors.

The capability of GaN IC's to work with high voltages and currents make it considered as ESD immune material. There are very few papers on ESD in GaN HEMTs and this topic been has been few interesting in the last years.

In this paper we will review the root cause analysis of ESD defect formation in AlGaN/GaN HEMT wafers due to fabrication process. An ESD formation mechanism was proposed, and the characterization of it and a solution to avoid it are suggested and implemented.

## PROCESS DETAILS

AlGaN/GaN HEMTs and MMICs were fabricated on 100mm GaN-on-SiC wafers. The fabrication process started with Ti/Al/Ni/Au metal stack evaporation followed by wet chemical lift-off process. Rapid thermal annealing (RTA) at 850ºC was used to form an ohmic contact. Passivation layer of SiN is deposited by Process Enhanced Chemical Vapor Deposition tool (PECVD). Device isolation was realized by using thick photoresist and ion implantation. The photoresist was removed by aggressive plasma stripping to remove the cured resist and finished with wet chemical stripping (lift-off) processes. The isolation patterns are within 5%-10% of the wafer area depending on the MMIC design. Further process steps to realize full MMIC such as supported T-gate, field-plate, first interconnect metals, resistors, MIM capacitors, thick Au-metal with air bridge capability, back-side process with via and thick metal plating were used.

## DEFECT CHARACTERIZATION

First detection of the defects was at a visual inspection station after the integrated isolation process, which is done manually by an optical microscope. Fig. 1 shows an affected metal ohmic structure. The defect was observed between two proximate ohmic contacts, and spreads all over the wafer. Another pattern found to be affected was a large metal structure, the defects concentrated at the corners of the pattern. Additional interesting observations were the defects

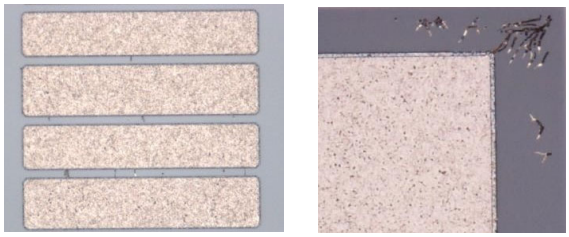

Fig. 1.Left: defect between two proximate ohmic contacts; right: defect at corner of the metal pattern, bounded by isolation layout.

show only at the active area of the wafer and are bounded by the isolation layout.

Study of a transfer length method (TLM) pattern showed a direct link between the spacing length of the ohmic contacts and defect density, as shown in Fig. 2. Another observation is of similar patterns which have the same spacing, but one is not isolated between the metals (active) while the other is isolated. The active area pattern shows defects while the isolated does not, highlighting the defect characteristics described before, shown in Fig.3.

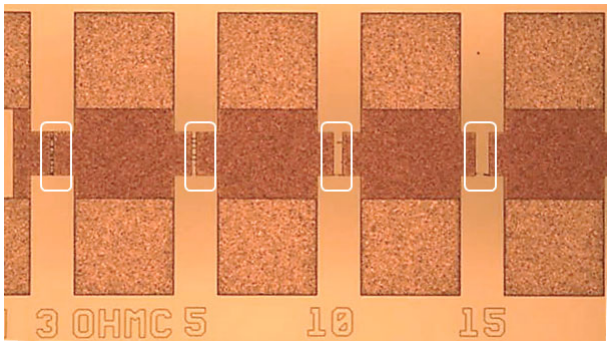


Fig. 2. TLM pattern show direct link between the spacing length of the ohmic contacts and defect density. Highest defect density is seen at 3nm spacing and the lowest density at 15nm spacing.

Fig. 3. Similar patterns have same spacing. The defect appears only at the active area.

Fig. 4 shows a FIB-SEM cross-section analysis which revealed damage on the surface of the wafer. The damage was characterized by melting channels of the SiN passivation and cracks through the AlGaN/GaN substrate. Fig. 5 shows an AFM scanning analysis, with the damage propagating into the substrate for a few hundred nanometers. The findings described in this section lead to the classification of the damage as an Electrostatic discharge defect (ESD).

## INVESTIGATION OF DEFECT ORIGIN

Knowing that the first detection of the defects was at the visual inspection station bounded the search for the root cause, followed by investigation of the isolation module. This led to understanding the defect nature related to

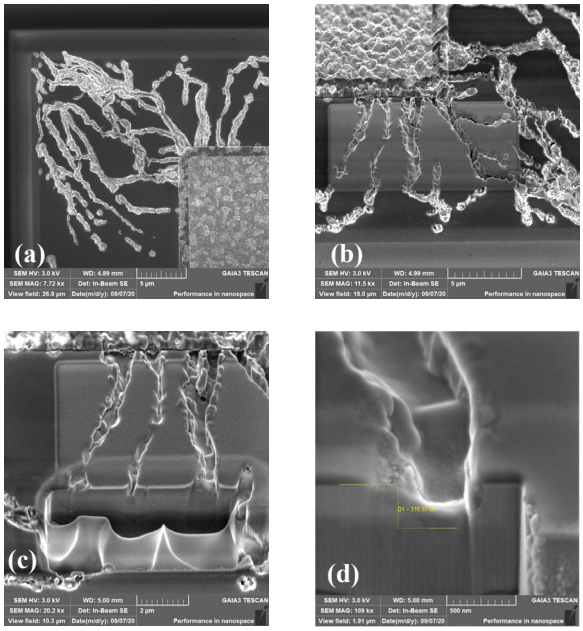


Fig. 4. FIB-SEM images of defect, (a) Top view,( b) Tilt view, (c) cross-section, (d) cross section and crack's depth measurement

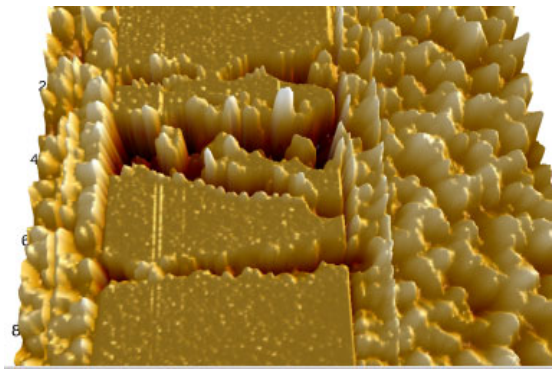

Fig. 5. AFM scanning of the surface of the wafers between two proximate ohmic contacts shows cracks.

electrostatic discharge, which limited the suspects to tools prone to causing this kind of defects. Tools in the process flow that have the highest probability for ESD related defects such as the implantation tool and those involving plasma were immediately marked as the main suspects. Commonality analysis disproved the RIE tool and pointed to one of the wet chemical lift off tools as a possible source. The investigation started with the implant tool. The implant process has been done at a vendor site. All the affected wafers fabricated in a sequence at the same day and no other wafers ran since the damaged batch to acquit the implant tool. Looking into data logs of the implant tool and comparing main process parameters of the affected wafers to base line wafers,

highlighted the beam current parameter was on the lower zone of its trend chart over the relevant period of time. An experiment was initiated to identify the origin of the defect focusing on implementation process. Five wafers were processed at the implant tool at three different beam currents set points to test the process window; low, base line and high set point values. The first assumption was that the wafers that were processed at the lowest beam current set point will show the highest magnitude of damage. However, visual inspection after the implant process wafers experiment did not show any signs of ESD damage. This finding weakened the assumption the implant process is the source for the defects, and moved the attention to the lift off machine. The next step in the flow is photo resist striping by the lift off machine. Wafers were processed in sequence, one by one and split between two wet stations. Station A is a batch immersion lift off tool, station B is a single wafer high pressure solvent spray tool. Summary of ion beam currents implantation process conditions, lift off tool types and the observations of a visual inspection are listed in Table 1. Both wafers which processed in tool B showed clearly ESD defect which points to it as causing the defect. Following this distinction, it was clearly required to delineate the scope of the damage and review wafers passing through this tool, seeking for ESD typical characteristic defects and to determine the starting time point of the problem. Several defected wafers were found in line at advance modules showing this defect in a low magnitude. Wafers pass through this tool at several steps in process flow, although only wafers which processed at Isolation module showed this defect. Examination of the process parameters of the different module's recipes showed the primary difference between them is the spray high pressure set point. At the Isolation module, pressure set point was the highest comparing to other recipes. Moreover, referring to tool A, which uses different resist stripping techniques, also reinforced suspicion to pressure related root cause for defect formation. To confirm this suspicion wafers were processed in tool B with lower pressure set points and did not show any evidence for ESD defects. Following this, wafers were processed in the tool at high pressure and gave clear signature the damage is caused only at high spray pressure condition.

TABLE I.
A SUMMARY OF BEAM CURRENTS CONDITIONS, LIFT OFF TOOLS AND OBSERVATION OF DEFECTS.

| Wafer | Beam Current | Lift Off Tool | Defect Observation |
|---|---|---|---|
| 1 | High | A | No |
| 2 | High | B | Yes |
| 3 | Low | A | No |
| 4 | Low | B | Yes |
| 5 | Base Line | A | No |

## DISCUSSION OF DEFECT MECHANISM

Studying the tool's configuration and process details were necessary to establish a possible model for defect formation root cause. The tool combined two process techniques; first module is a heated emersion processing and second module is a single wafer high pressure spray process. Following the soak the solvent wet wafer is transported to a single wafer spin process station for lift off processing. Most of the resist dissolved during the soak, and the cured resist residues are rapidly removed with high pressure process that includes fan spray of NMP. First to be inspected was the grounding of all relevant parts in the tool. Several parts were found ungrounded. After repairing the faults, wafer was processed and still showed ESD defect. This result lead to a model related to ESD generation due to friction between high speed liquid and nozzle surfaces. Static electricity can be generated between the liquid and the pipe wall when the liquid flows inside the pipe or can be generated by being ejected from the nozzle. In high pressure there is a critical spray droplet speed which can result in static electricity, when the charged fluid impacts the wafer surface it is discharging and it causes ESD defect on the surface of the wafer [2]. This model can describe the defect formation mechanism in this case. As described, the tool uses high pressure lift off technique. High speed flow of NMP is ejected from narrow nozzle and generates static electricity, shown in Fig. 6. The charged droplet strikes the surface of the wafer, the metal patterns on the active area on the wafers are charged and being discharged in conductive areas which are patterned by the isolation process. To avoid this defect, spray pressure was decreased to an optimum value and defect was eliminated.

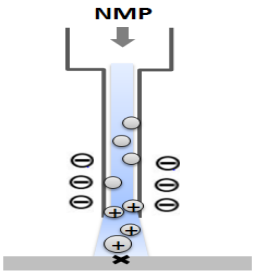


Fig. 6. A diagram of static electricity generated between the liquid and the pipe wall.

## CONCLUSIONS

This paper demonstrated an ESD damage formation in AlGaN/GaN HEMT wafers due to the fabrication process. By using root cause analysis the source of the ESD damage was identified and a model was proposed. A lift-off tool with high pressure capability caused fluidic discharge when impacts the wafer surface. To avoid this defect spray pressure was decreased to an optimum value and defect was eliminated.

## ACKNOWLEDGEMENTS

We would like to acknowledge INNOViON corp. team, John Schuur, Doug Gonelli and Ray Pong for excellent support. brain storming meetings and doing ion implantation experiments to solve this ESD puzzle from the ion implantation point of view.
We would like to acknowledge Ari Choen-Nov for the FIB-SEM anlaysis.

## REFERENCES

[1] J. E. Vinson and J. J. Liou. Electrostatic discharge in semiconductors devices: an overview, PROCEEDINGS OF THE IEEE, VOL. 86, NO. 2, FEB 1998

[2] Ji Hoon Cha et al. Electrostatic Discharge Control and Visualization in Spray Nozzle. Solid State Phenomena. Vol. 282, pp 77-80 (2018).

## ACRONYMS/NOMENCLATURE

ESD: Electro Static Discharge
GaN: Gallium Nitride
HEMT: High Electron Mobility Transistor
TLM: Transfer Length Method
FIB-SEM: Focussed Ion Beam milling combined with Scanning Electron Microscopy
AFM: Atomic Force Microscope

# SESSION 7:
# PLENARY 3

# Low-temperature direct wafer bonding innovating CS device technologies

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**Keywords: Low temperature direct wafer bonding, Surface activated bonding, interface, TEM, diamond**

**Abstract**

**Direct bonding of wafers is attractive in integrating dissimilar materials into advanced devices and modules, because different materials can be directly bonded at room temperature. Surface activated bonding (SAB) is especially promising, because wafers are bonded at room temperature, and no wet processing is required. The bonding quality is sensitive to the wafer morphology and flatness, because bonded interfaces are formed without intermediate layers. In the first step of the SAB process, the wafer surfaces are activated by irradiation with a fast atom beam (FAB). We discuss the effects of wafer morphology on bonding quality. We will describe the effects of FAB irradiation on the nanostructural and electrical properties of the bonded interfaces. We will also show recent results of direct bonding of diamond. This exciting result offers a new path for innovation in compound semiconductor technologies.**

## INTRODUCTION

Heterogeneous integration of dissimilar materials has achieved a great progress in the compound semiconductor industry, and it has enabled fabrication of several types of heterostructure devices. Direct bonding technologies performed at room temperature enable the integration of dissimilar materials with different lattice constants, crystal structures, and coefficients of thermal expansion [1] into exciting new device types which would otherwise be impossible to create. Among the several types of direct bonding technologies, surface activated bonding (SAB) is especially promising, because bonding can be achieved without any wet processing, and successful bonds can be formed at room temperature, without heating the wafers [2]. Various combinations of dissimilar materials have been successfully bonded, and the structural and electrical properties of the bonded interface have been characterized.

Here, we will focus on SAB as a method for fabricating novel semiconductor devices. After outlining the SAB process, we will discuss the requirements for successful wafer bonding, and describe the effects of different surface activation conditions on the properties of the bonded interface. The fabrication and characterization of junctions fabricated by direct bonding of diamond will also be described.

## METHODS AND EFFECTS OF SURFACE ACTIVATION

Figure 1 shows the process flow of surface activated bonding (SAB). First, wafers are loaded into a vacuum chamber, and a fast atom beam (FAB) of neutralized atoms (typically Ar) is used to remove the native oxide on the wafer surfaces. The pressure and acceleration voltage during FAB are ~$10^{-6}$ Pa and 1-2 kV, respectively. The activated surfaces of the two wafers are then bonded, by pressing them together with a bond pressure of ~10 MPa.

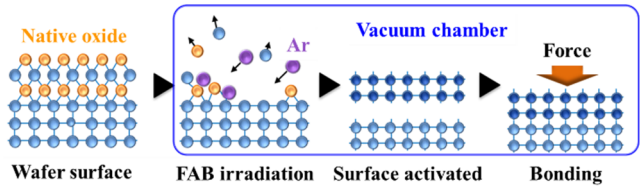


Fig. 1. Schematic process flow of surface activated bonding.

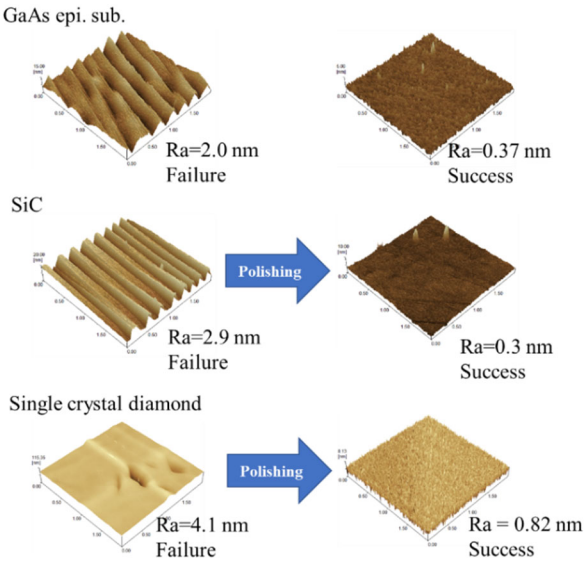


Fig. 2. AFM images and results of bonding test of wafers.

The bonding yield is sensitive to the wafer morphologies, including large scale flatness, bowing, and localized roughness. One empirical criterion is that the roughness average (Ra) of bonded surfaces should be <1 nm for successfully bonding semiconductor wafers. Assessing this

criterion can be done using an atomic force microscope. (AFM) images of several wafers used in the bonding test are shown in Fig. 2. The undulation of wafer surfaces observed in off-angle wafers degrades bonding yield, so it should be avoided. Other wafer surface morphology characteristics such as warp and thickness variation will often limit the bonding yield.

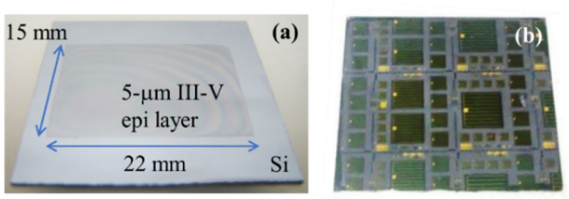


Fig. 3. (a) 5-μm III-V epi layer bonded to Si. (b) InGaP/GaAs/Si hybrid triple-junction solar cells [3].

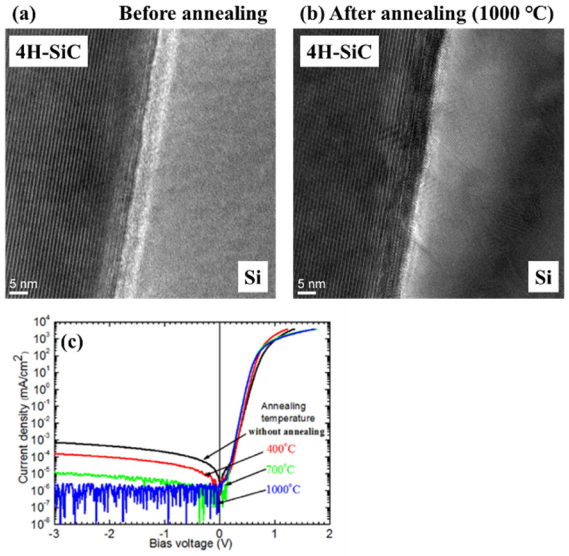


Fig. 4. TEM images of (a) as-bonded and (b) 1000-°C annealed $p^+$-Si/n-4H-SiC interfaces. (c) Current-voltage characteristics of $p^+$-Si/n-4H-SiC junctions annealed at different temperatures [4].

The surfaces of the wafers are etched slowly by sputtering during the FAB irradiation with Ar. The etch rate of Si is typically 2-3 nm/min. The surface roughness Ra increases for longer durations of FAB irradiation. The FAB duration and flux must be optimized; enough FAB to remove surface oxides and provide surface activation, but not so much as to excessively erode the surface. Using the optimized bonding conditions, we successfully prepared 5-μm thick III-V epi layer/Si junctions by bonding epi layers grown on GaAs (100) wafers to Si and selectively etching the GaAs wafers (Fig. 3(a)). InGaP/GaAs/Si hybrid triple-junction solar cells were fabricated using the III-V/Si junctions as is shown in Fig. 3(b) [3].

We observed amorphous-like layers and/or defect layers in the vicinity of as-bonded interfaces using transmission electron microscope (TEM) [4,5]. Deviation from stoichiometry was apparent in GaAs layers near as-bonded GaAs/Si interfaces [5]. In most cases such damaged layers caused by the FAB irradiation, become faint after annealing the junctions, as is typically seen in TEM images of Si/4H-SiC (Figs. 4(a) and (b)) [4] and GaAs/Si interfaces [5].

Damage due to FAB irradiation will introduce midgap defect states at the bonded interface, and will cause degradation in their electrical properties. The reverse leakage current observed $p^+$-Si/n-4H-SiC junctions was reduced by annealing them at 1000 °C (Fig. 4(c)) [4]. We also found that resistance across $n^+$-GaAs/$n^+$-Si junctions decreased from ~30 to 1.6-2.1 mΩcm$^2$ after annealing [6]. These results show that post-bonding annealing can improve the quality of junctions formed by SAB bonding. (This effect is analogous to the annealing induced reduction in damage and junction leakage currents seen after plasma damage in junctions from conventional dry etching.

## RECENT ACHIEVEMENTS—DIRECT BONDING OF DIAMOND

Semiconductor devices and modules with extremely low thermal resistance can be realized by directly bonding either semiconductors or metals (heat sink) to diamond, i.e., by employing the "X-on-diamond-on metal" configurations (Fig. 5). First, we directly bonded a Ib-type single crystal diamond to a Si (100) wafer. The diamond was firmly bonded to the Si wafer, even after annealing at 1000 °C, despite the large mismatch in the coefficients of thermal expansion [7].

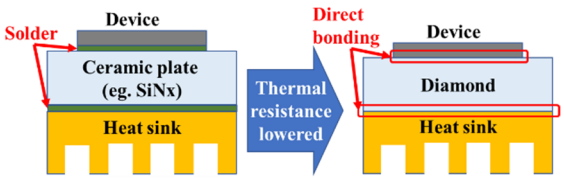


Fig. 5. Modules with direct-bonding based "X-on-diamond-on metal" configuration targeting the lowest thermal resistance.

We successfully fabricated FETs by the epitaxial growth on bonded diamond wafers and device fabrication process shown in Fig. 6. The substrate temperature during the epitaxial growth was as high as ~930 °C. The bonded Si/diamond junctions were stable against such a high temperature process. The TEM images (Fig.7) show that SiC intermediate layers formed at the bonded interfaces after annealing, which might explain the unexpectedly excellent tolerance of these junctions against thermal process.

We also bonded a 200-nm p-GaAs epi layer to diamond, and characterized the nanostructures of the bonded interface, before and after annealing at 400 °C. TEM images of interfaces before and after annealing are shown in Figs. 8(a) and 8(b), respectively. In contrast to other interfaces, defect layers observed in the as-bonded interface remained even after annealing, which suggests that the condition for surface

activation should be optimized for improving interface characteristics by post-bonding annealing.

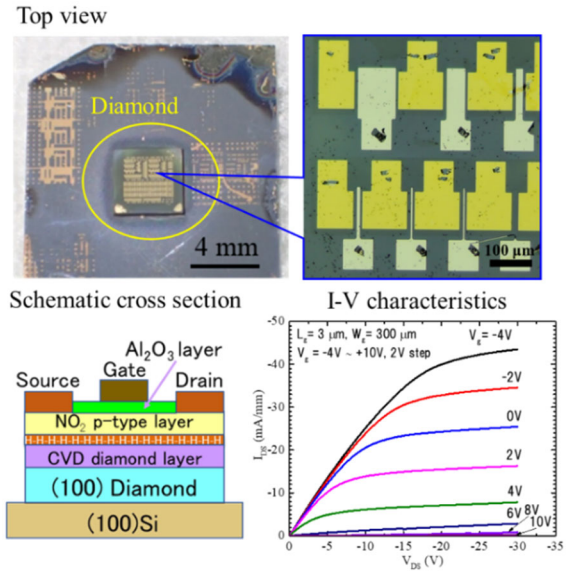


Fig. 6. Top view, schematic cross section, and current-voltage characteristics of diamond FETs fabricated on diamond bonded to Si (100) wafer [7].

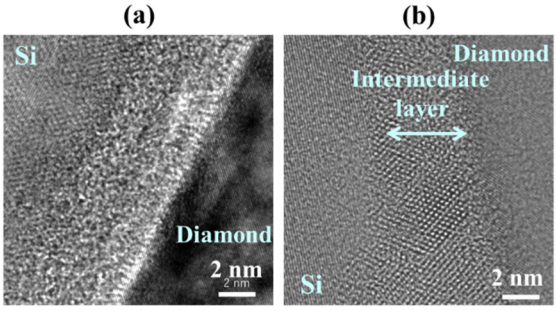


Fig. 7. TEM images of (a) as-bonded and (b) 1000-℃ annealed Si/diamond interfaces.

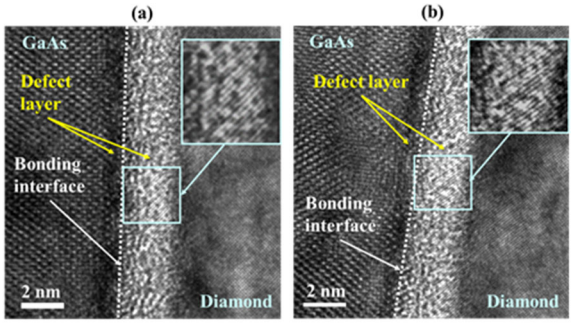


Fig. 8. TEM images of (a) as-bonded and (b) 400-℃ annealed GaAs/diamond interfaces [8].

The thermal properties of the GaAs layers were characterized by observing infrared (IR) emission from surfaces, while varying bias voltages parallel to GaAs/500-μm diamond interfaces. Results are summarized in Figs. 9(a) to 9(e). The observed thermal resistance of the GaAs/diamond junction (6 K/W, which corresponds to ~$1.4\times10^{-7}$ $m^2$·K/W by normalizing using the GaAs mesa area for heat dissipation, 60 μm by 400 μm) was smaller than that of GaAs/370-μm sapphire junction (34.9 K/W (~$8.4\times10^{-7}$ $m^2$·K/W)), because of the much higher thermal conductivity of diamond (~2000 W/mK) compared with sapphire (41 W/mK) [8]. The measured thermal resistance was comparable to approximate estimates of thermal resistance (1.4 and 54 K/W for GaAs layers on diamond and on sapphire, respectively). Our research has now been extended to direct bonding of GaN and diamond for fabricating GaN-on-diamond structures without intermediate layers. The nanostructural properties of GaN/diamond interfaces, and their thermal resistances are now under investigation.

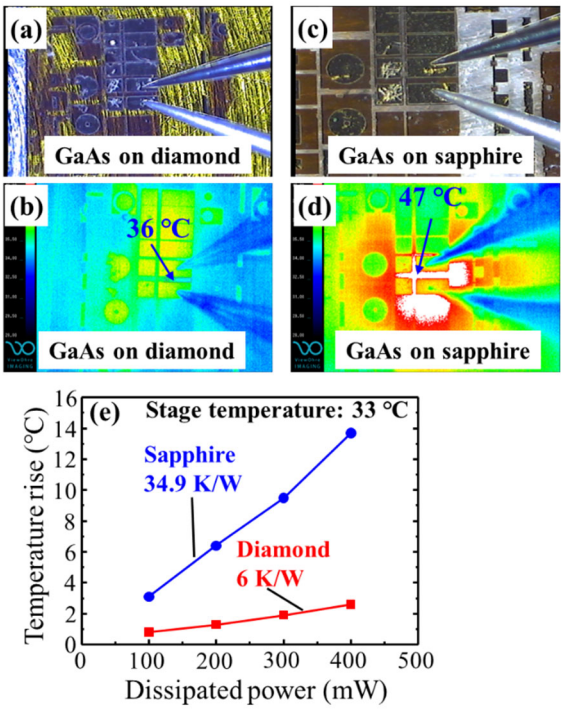


Fig. 9. (a)-(d) IR images of GaAs layer on diamond and GaAs layer on sapphire. (e) Relationship between temperature and dissipated power for GaAs layers [8].

Promising results have been obtained by bonding metals to diamond. Cu/diamond junctions were fabricated and their thermal properties were characterized. As is seen from TEM images (Figs. 10(a) to 10(c)), defect layers were apparent at as-bonded Cu/diamond interfaces. The thickness of these defect layers decreased by annealing junctions at 700 ℃. Using time-domain thermal reflectance, the thermal boundary resistance (TBR) of the bonding interfaces was estimated to be (1.7±0.2)×$10^{-8}$ $m^2$·K/W [9], which was close to that of evaporated Cu/diamond interfaces and ~1/10 of TBR of solder layers (Fig. 10(d)).

These results show that direct bonding technologies, such as SAB, are very promising for realizing advanced high power CS devices and modules with very low thermal resistance.

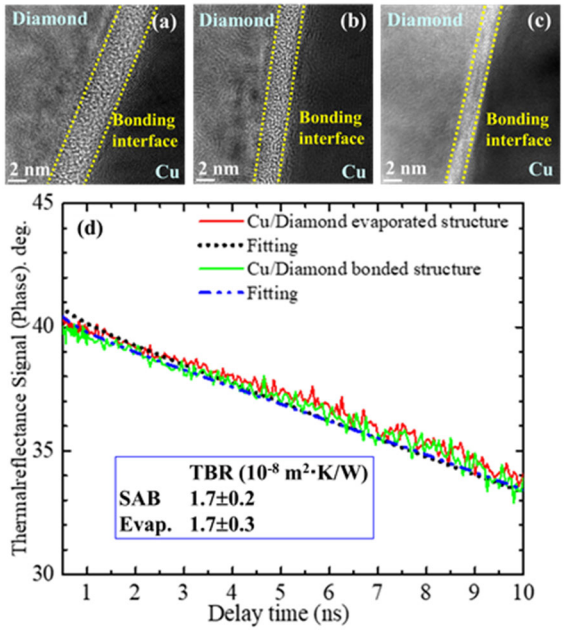


Fig. 10. TEM images of (a) as-bonded, (b) 500-℃ annealed, and (c) 700-℃ annealed Cu/diamond interfaces. (d) Thermal reflectance signals of Cu/diamond bonding interface and evaporated Cu/diamond interface [9].

## SUMMARY

Results from several applications of surface activated bonding (SAB) were described, with emphasis on characteristics of fabricated semiconductor junctions. The influence of wafer flatness and morphology on bonding yield were described. The effects of Ar FAB beam irradiation on the nanostructural and electrical properties of the bonded interfaces were discussed. We showed that post-bonding annealing plays an important role in improving structural and electrical quality of the bonded interface. Recent exciting initial results of bonding of diamond to other semiconductors and metals were presented. This work is ongoing and more will be reported in future publications.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] O. Moutanabbir and U. Gösele, Annu. Rev. Mater. Res. **40**, 469 (2010).

[2] H. Takagi, K. Kikuchi, R. Maeda, T. R. Chung, and T. Suga, Appl. Phys. Lett. **68**, 2222 (1996).

[3] Naoteru Shigekawa, Jianbo Liang, Ryusuke Onitsuka, Takaaki Agui, Hiroyuki Juso, and Tatsuya Takamoto, Jpn. J. Appl. Phys. **54**, 08KE03 (2015).

[4] J. Liang, S. Nishida, M. Arai, and N. Shigekawa, Appl. Phys. Lett. **104**, 161604 (2014).

[5] Y. Ohno, J. Liang, N. Shigekawa, H. Yoshida, S. Takeda, R. Miyagawa, Y. Shimizu, and Y. Nagai, Appl. Surf. Sci. **525**, 146610 (2020).

[6] Naoteru Shigekawa, Ryo Kozono, Sanji Yoon, Tomoya Hara, Jianbo Liang, and Akira Yasui, Sol. Energy Mater. Sol. Cells, **210**, 110501 (2020).

[7] Jianbo Liang, Satoshi Masuya, Seongwoo Kim, Toshiyuki Oishi, Makoto Kasu, and Naoteru Shigekawa, Appl. Phys. Express, **12**, 016501 (2019).

[8] Jianbo Liang, Yuji Nakamura, Tianzhuo Zhan, Yutaka Ohno, Yasuo Shimizu, Kazu Katayama, Takanobu Watanabe, Hideto Yoshida, Yasuyoshi Nagai, Hongxing Wang, Makoto Kasu, and Naoteru Shigekawa, Diamond and Related Materials, **111**, 108207 (2021).

[9] Jianbo Liang, Yutaka Ohno, Yuichiro Yamashita, Yasuo Shimizu, Shinji Kanda, Naoto Kamiuchi, Seongwoo Kim, Koyama Koji, Yasuyoshi Nagai, Makoto Kasu, and Naoteru Shigekawa, ACS Appl. Nano Mater. **3**, 2455 (2020).

## ACRONYMS

AFM: Atomic Force Microscope
FAB: Fast Atom Beam
Ra: Roughness average
SAB: Surface Activated Bonding
TBR: Thermal Boundary Resistance
TEM: Transmission Electron Microscope

# Driving lower fiber optical power consumption through monolithic electronic and optoelectronic integration

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**Keywords: InP, E-O integration, monolithic integration, receiver sensitivity, power consumption, optical communication**

**Abstract**

**There has been considerable effort in both SiPh and InP on developing optical PICs for datacenter and other applications. The partitioning between optical PICs and ASICs, though, necessitates unwanted parasitics, intrinsic to the architecture itself, which limit system performance. If this boundary between optical PICs and ASICs is removed, superior performance becomes possible, which in turn can drive lower fiber optical power consumption. Some specific examples are presented.**

## Introduction

It is well known that for datacenter, wireless and PON applications, overall power is a vital consideration. Separate from the overall carbon footprint and climate change considerations, datacenters are often located near a specific power source and have brick wall power limitations. In addition, any power consumed in transmitting, receiving or maintaining temperature locally has a multiplier effect in overall cooling of the datacenter. And received signals within datacenters or 5G often operate well in excess of 30dB from the quantum photon limit [1]. Considerable effort has gone into optical PICs, whether in SiPh or InP. SiPh has the advantage of larger wafers and greater overall infrastructure. InP has the advantage of direct bandgap native materials for light transmission and detection. Both are viable. ASICs have the maturity of a half century of Moore's Law. There are very few transistor options c.f. the plethora of potential elements in optics PICs. This means that the design flow of ASICs is quite mature whereas the design flow of optics PICs, whether SiPh or InP-based, tends to be less mature and more complex. Moreover, the ASICs which can be produced are massive in gate count – e.g. DSPs. Optics PICs, on the other hand, tend to have medium-sized element count in disparate elements, and are proceeding in gate count much slower than the Moore's Law for ASICs because of the complexity in disparate elements [2]. This segregation, though, leads often to the need to connect electrically the optical and electronic elements, and with associated parasitics at the very connection point where the signal can be the smallest or the penalty for parasitics can be the greatest. If these parasitic elements could be significantly reduced or eliminated, then performance could be improved and power within the datacenter decreased.

## Discussion and Results

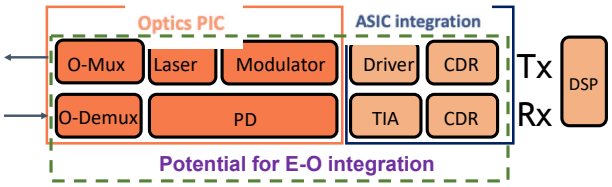


Fig. 1 Potential for E-O integration. Optics PICs and ASICs tend to have segregated functionality. E-O integration can bridge this gap, improving power consumption.

Fig. 1 shows schematically how such a fiber optical module or board partitioning looks. Those elements which are closest to the optics tend to be more analog in nature, relatively low in gate count sometimes, and more amenable to monolithic integration with optics PICs. SiPh tends to be run in more cost-effective technologies, meaning that the transistor gate length tends to be several generations behind the latest and greatest. This is because optical elements have significantly larger physical dimensions than transistors. Although it is possible to run the optics PIC functionality in low gate length Si technologies, the cost per area is usually prohibitive. In the larger gate length technologies, the gate count is necessarily limited, as is the electronic speed. And so it happens that in general both SiPh and InP-based photonics tend to be optoelectronics and optics rather than electronics. And for all its advantages, SiPh has the further disadvantage that there is no efficient direct bandgap material near 1.3 or 1.55um wavelength, meaning that light detection and most especially light generation are more difficult. It is unlikely that the high gate count of the DSP would be fruitfully reproduced in a high gate length Si technology or InP technology. However, analog functionality is quite another matter. Analog functionality is often better accomplished in bipolar than FET technology in the first place, whether in BiCMOS or InP. This makes SiGe:SiPh and InP ideal materials with which to implement analog functionality on the same substrate as the optics PIC. The present industrial state of the art for $f_T$ is approximately 300GHz for SiGe [Zimmer] and for InP [GCS]. This enables circuits with baud rates of 25GB or even 50GB.

In the case of transmitters, the integration of a driver with electronics would save considerable power by making the transmission line more efficient. The starting point, though, may be the receiver. A typical receiver sensitivity is far from the quantum limit, as is seen in Fig. 2. In this case, PON applications are separated from non-PON applications because of the up to 32:1 split from the head end to the client end, resulting in significantly better receiver sensitivity required. It is also worth noting that 2.5G PON and 10G datacenter applications are much older than the newer 25G applications, and these newer applications are, apples for apples, generally closer to the quantum limit, although still very far away. Of further note is applications with pin PDs usually need to satisfy overload requirements of +3dBm or so incident upon the receiver, with all the system architecture considerations implied upon the pin-TIA combination.

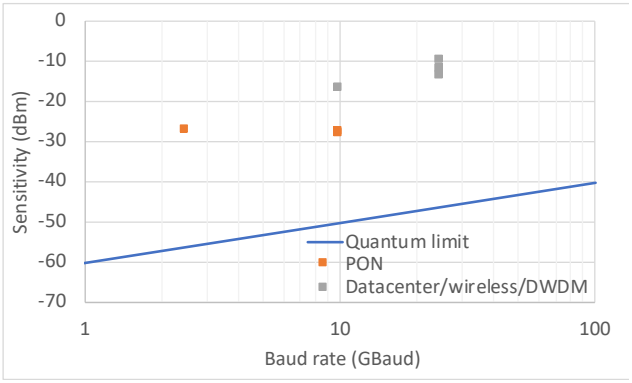


Fig 2. Sensitivity for typical applications c.f. the quantum limit.

For PON applications, an APD is typically used, which is usually 3-5dB better than a pin PD, whereas a pin PD is usually used for non-PON applications. The exception is for extended reach, where more reach than a pin PD would be desired, but because of gain-bandwidth limitation of commercially available APDs, it is challenging to use an APD at 25 GBaud or higher. In these cases, extensive DSP is often used to compensate for the poor high speed performance of APDs, but is it clear that the system limit is under strain. The usual way to compensate for this is to boost the transmitter power, but it is clear that the overall system power would be significantly reduced if the receiver could be improved at the fundamental level. All benefits to the receiver can in principle flow immediately to the transmitter launch level for a given link budget, immediately reducing the power of the overall system. The transmitter, in turn, can be made more power efficient in its own right, and building on the benefits already accrued from the superior sensitivity of the receiver.

The most common configuration for amplifying the small signal from a PD to an output level which can be useful to the outside world involves TIAs. The lower the capacitance of the pin and the TIA, the higher the transimpedance can potentially be without noise dominating. The most effective way to reduce the practical capacitance of a PD is to eliminate the bond pad capacitance. The intrinsic capacitance of the light-producing portion of the PD is necessary, but the bond

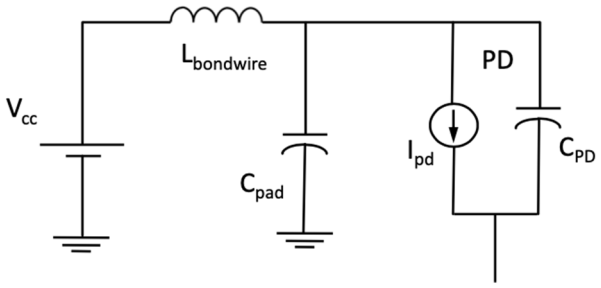


Fig. 3. Equivalent circuit for monolithically integrated PD.

pads merely serve to connect the PD to the outside world and their capacitance is merely parasitic. In this paradigm, reducing the active area of the PD, adding some complexity to the fiber alignment, is worth it, because C is no longer dominated by the bond pads. Using monolithic integration, one bond pad can be eliminated by direct interconnect between the pin PD output and the first stage TIA input. The other connection which supplies $V_{cc}$ can be considered in the context of the bondwire, as shown in Fig. 3. In this case there is only one bond pad, connected to an external voltage $V_{cc}$, because the opposite end of the PD is connected monolithically to the base of the input transistor on the TIA. $C_{pad}$ and $L_{bondwire}$ are the bond pad capacitance and wirebond inductance. The PD is represented as a current source $I_{pd}$ in parallel with the intrinsic capacitance $C_{PD}$. The one bond pad is eliminated and the second one can be ignored under certain practical conditions.

The most important consideration for the second bond pad is the resonance frequency relative to the bondwire, which is calculated in Fig. 4 as a function of frequency for a typical

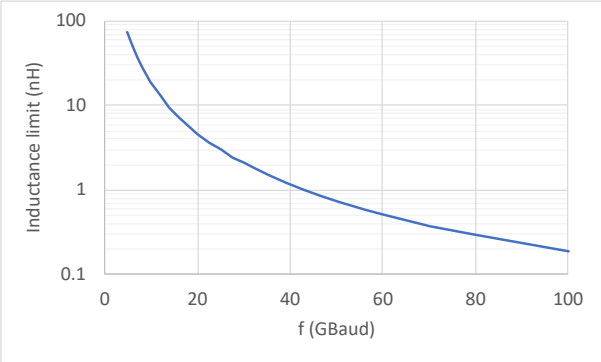


Fig. 4 Wirebond inductance limit as a function of resonance frequency for circuit in Fig 3. The assumed bondpad capacitance was 15fF.

bond pad capacitance of 15fF, which capacitance is a typical value based on vendor data. Below this limit the electrical effect of the bond pad can be ignored. For typical wirebond

lengths and diameters, in practice this means that no attention needs to be given to this below approximately 50GBaud, which is helpful for today's baud rates.

For baud rates for ~50GBaud and below, therefore, it is practical to consider monolithic integration of the PD and TIA. A further consideration, for long-reach and for PON applications, where APDs are already needed, is that a pin PD will, all else equal, always be faster than an APD because in the pin PD there is only one transit time for carriers, usually only part of the absorption region, whereas in the APD the initial carriers must travel from the absorption region to the multiplication region, be multiplied, and then the secondary carriers must return through the full distance through the absorption region to reach the contact [Campbell??]. If the pin-TIA connection can be made quieter, then there may be need to "force" an APD into the system architecture for sensitivity considerations, and also suffering the associated bandwidth and therefore DSP power penalties.

In summary, the foregoing demonstrates that there are parasitics benefits to monolithic integration of the PD and TIA, but do not yet demonstrate that there is an overall receiver benefit. Perhaps the most clear-cut way to evaluate this is by considering a single PD and first-stage TIA and evaluating the SNR. The associated SNR is the single largest indicator of eventual sensitivity at the higher voltage end of the circuit.

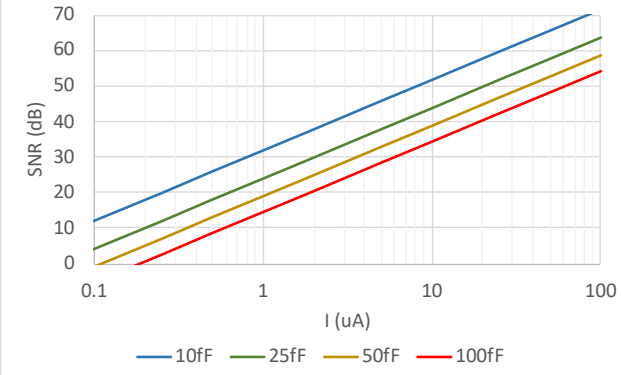


Fig. 5. SNR (dB) vs input photocurrent I for different C values.

Fig. 5 shows the SNR vs input photocurrent for different capacitance C values. In this case, an example transimpedance of 40dB-ohms was used. This could be made even higher because of the lower Johnson noise associated with the lower input capacitance, which is a key benefit of the monolithic integration approach, but even 40dB-ohms will serve to demonstrate the point. Red is "hotter" (more C) moving through the spectrum to blue, which is "colder" (less C). In this case the photocurrent is average value and an infinite ER was used for simplicity, meaning the zeros have no current. It is clear that the SNR increases by 20dB per decade of input photocurrent, which makes intuitive sense. As a design curve, Fig. 5 can be used for any given SNR, indicative of an incumbent SNR solution, drawing a horizontal line to see how much improvement in the photocurrent, and therefore input power, can be had by lowering the PD capacitance by means of monolithic integration. As a reference, for a typical quantum efficiency of 75%, 1uA average photocurrent at 1.3um is equivalent to -29dBm of input power, so this power scale goes from approximately -39..-9dBm of input power spanning three decades. As a ballpark figure, roughly 10dB of SNR should translate to sufficient sensitivity at a BER of 1E-12.

It is evident from Fig. 5 that although the C spacing between curves increases from blue towards red, the curves actually get closer together. This effect is shown more explicitly in Fig 6, which shows SNR vs C for different values of average input photocurrent. For PDs with high C there is limited benefit to using this technique, but for small geometry PDs for which the bond pads form a significant fraction of the capacitance, as is the case for 16um and 20um active area PDs today [4] and even smaller which can accommodate an optical fiber for packaging, there can be significant benefit. In this case, all else equal, an improvement in SNR of approximately 8dB can be expected for the same input power by lowering C or, equivalently, an improvement of approximately 4dB in input sensitivity for the same SNR from a practically achievable capacitance reduction. This improvement can be stacked with other improvements to the PD itself which might be realized because of the ability to monolithically integrate, and also with the accrued benefits of no external contact from the PD to the TIA, which is in general a source of noise for many reasons, including acting as an antenna for picking up other nearby signals as crosstalk as an integral part of the packaging considerations.

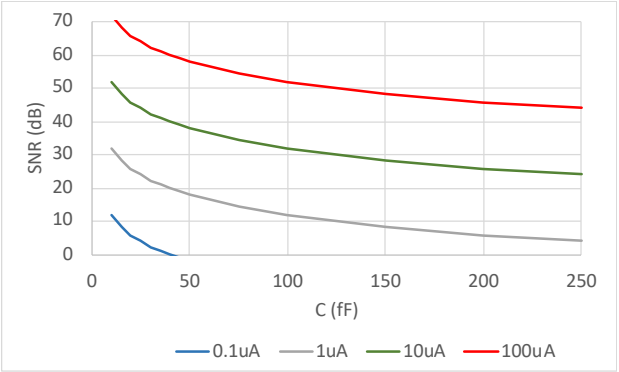


Fig 6. SNR (dB) vs C for different input photocurrents values.

It is worth considering why this work is not done commercially in general. It is clear that the idea of integrating a pin PD and TIA has been around for a long time [6]. It is also worth noting that in the past it is not clear that there was a performance advantage from monolithic integration. There is generally a cost and often a density advantage from monolithic integration, but monolithic integration is often a compromise among the integrated elements. Not so in this case, where clear performance advantages are observable.

ELPHiC has carried out more detailed modeling for a full pin-TIA circuit, and considering all the packaging parasitics. In the package, modeling shows that for a 10G PON application, significantly better than -30dBm could reasonably be expected in the TO can, meaningfully outperforming a typical APD-TIA incumbent solution, even after taking into account packaging considerations. This is particularly important in PON applications because the next gen PON will either be 25G or 50G in baud rate. For 25GBaud, an APD is conceivable if difficult to implement. For 50GBaud, an APD is out of the question. For this future application, if a 32:1 split ratio is to be preserved, there must be either an increase in transmitter power, which is highly undesirable, or an improvement in receiver technology architecture, which monolithic pin-TIA can offer. In this case one can avoid a significant increase in transmitter power and all the associated overhead despite the significant increase in baud rate.

Similarly, for fronthaul 5G applications ELPHiC modeling shows that a pin-TIA monolithically integrated solution is expected to outperform incumbent solutions. A receiver sensitivity better than -20dBm could reasonably be expected in the TO can, even after taking into account packaging considerations.

Note that both the 10G and 25G examples reported here are a significant improvement over incumbent solutions as shown in Fig. 2.

## APPLICATIONS

For APD-based applications today, such as PON or some of the extended reach 25G applications, it is conceptually easy to use a pin-TIA monolithically integrated combination as a substitute for APDs. A further system architecture advantage is the reduced power supply need, as an APD requires tens of volts whereas the pin-TIA combination requires only the standard 3.3V. This can greatly simplify board design.

For pin PD-based applications, monolithic integration can improve the sensitivity, which in many cases is an advantage either, from a system link budget perspective or to permit lower transmitter power. If the overload requirement is to be preserved, this implies an increased dynamic range requirement on the TIA. An important consideration is whether is it more important to preserve the overload requirement or to maintain the TIA dynamic range, which would imply a lower overload limit.

MSA standards already exist for many 10Gb/s and 25Gb/s applications. However, MSA standards have yet to be finalized for many 25GBaud and 50GBaud applications. A monolithically integrated receiver can help drive a lower transmitter spec, saving fiber optical power going forward.

## CONCLUSIONS

In conclusion, it is possible to repartition the overall fiber optical module or board chipset architecture in such a way as to permit the monolithic integration of optical PICs and electronics for the more analog electronics or where the gate count is not excessively high. In that case, the overall power in a fiber optical system can be substantially reduced first through improved receiver sensitivity, which permits lower transmitter power, and then through improving the transmitter itself through analogous means. Some specific example simulations have been shown which demonstrate this.

## ACKNOWLEDGEMENTS

This work is really a collaboration among many, to whom the author is indebted. In particular, medeling and concepts from Professor Rony Amaya (Carleton University), Jim Hjartarson, Andre Hagley, Rick Clayton, Shakeeb Abdullah, Wenyu Zhao and Rene Nyangezi have been most illuminating.

## REFERENCES

[1] L. Tarof *Fundamental and Technology Ecosystem Considerations for Photonics ICs and Datacenter Architectures*, 2019 Optinet, Paper T72, June, 2019.

[2] L. Tarof, *How advanced packaging can help align the evolution of photonic ICs with Moore's Law*, Laser Focus World, pp.20-21, Mar, 2017

[3] Thomas Zimmer et al, *SiGe HBTs and BiCMOS Technology for Present and Future Millimetere-Wave Systems*, IEEE Journal of Microwaves 1 (1), pp.288 – 298 (2021). 10.1109/jmw.2020.3031831 hal-03111157

[4] As one example of what is commercially available: *http://www.gcsincorp.com/dedicated_pure-play wafer foundry/InP%20HBT%20Technologies.php*

[5] J. C. Campbell, "*Recent advances in avalanche photodiodes*, IEEE Journal of Lightwave Technology **34**, (2), pp. 278-285 (2016), doi: 10.1109/JLT.2015.2453092.

[6] S.Chandresekhar et al., *Eight-Channel p-i-n/HBT Monolithic Receiver Array at 2.5 Gb/s Per Channel for WDM Applications*, IEEE Photonics Technology Letters **6** (10), pp.1216-1218 (1994).

## ACRONYMS

APD: Avalanche Photodiode
ASIC: Application Specific Integrated Circuit
CDR: Clock and Data Recovery
DSP: Digital Signal Processor
ER: Extinction Ratio
HBT: Heterojunction Bipolar Transistor
O-Demux; Optical Demultiplexer
O_Mux: Optical Multiplexer
PD: Photodiode
PIC: Photonics Integrated Circuit
SiPh: Silicon Photonics
SNR: Signal to Noise Ratio

# How are high-volume 3D Sensing applications shaping the Compound Semiconductor Industry?

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**Keywords: GaAs, 3D sensing, VCSEL, LiDAR, Datacom**

**Abstract**

**Today's remarkable high-volume demand in 3D sensing had a significant impact on the compound semiconductor industry. This report provides an overview of market triggers for VCSEL and the development of GaAs wafer and epiwafer industry, along with market forecast of different impacted segments.**

## INTRODUCTION

Until 2017, the VCSEL market was driven by Data communications (datacom) applications that emerged in 1996. Datacoms was the first industrial application to start integrating Vertical Cavity Surface Emitting Lasers (VCSELs). Their sweet spot has been in short-distance data communication due to their low power consumption and competitive price compared to Edge Emitting Lasers (EELs). Driven by the development of datacenters, the VCSEL market and production boomed in the 2000s with the internet's popularity, and then grew steadily. Some new applications for VCSEL emerged, like laser printers and optical mice, but were not strong growth drivers.

Since 2017, the datacom application that was driving the market has been replaced by 3D sensing application, especially since the implementation of the Face ID module in iPhones. Following the release of the iPhone X, several smartphone manufacturers followed the same path and implemented 3D sensing module in the front side of smartphone for face recognition.

3D rear sensing in mobile has diversified its application use cases. First used for photography, to enhance bokeh and zoom capabilities, it will expand into Augmented Reality (AR) and gaming. Beyond smart phones, time of flight (ToF) modules have a broad application market in front of them, including intelligent driving, robots, smart homes, smart TVs, smart security and virtual reality (VR)/AR. Currently, the application of ToF technology in these fields is still in its infancy.

Yole Développement (Yole) expects the global 3D imaging and sensing market to expand from $5B in 2019 to $15B in 2025, at a 20% Compound Annual Growth Rate (CAGR) as indicated in fig.1. The significance of the 3D sensing market means the transition from imaging to sensing is happening before our eyes. Artificial Intelligence (AI)-powered devices and robotics are gaining a better understanding of their surroundings and developing a new level of interaction with humans. Advanced Driver Assistance Systems (ADAS) are a highly anticipated application of 3D imaging and sensing technology. The most important

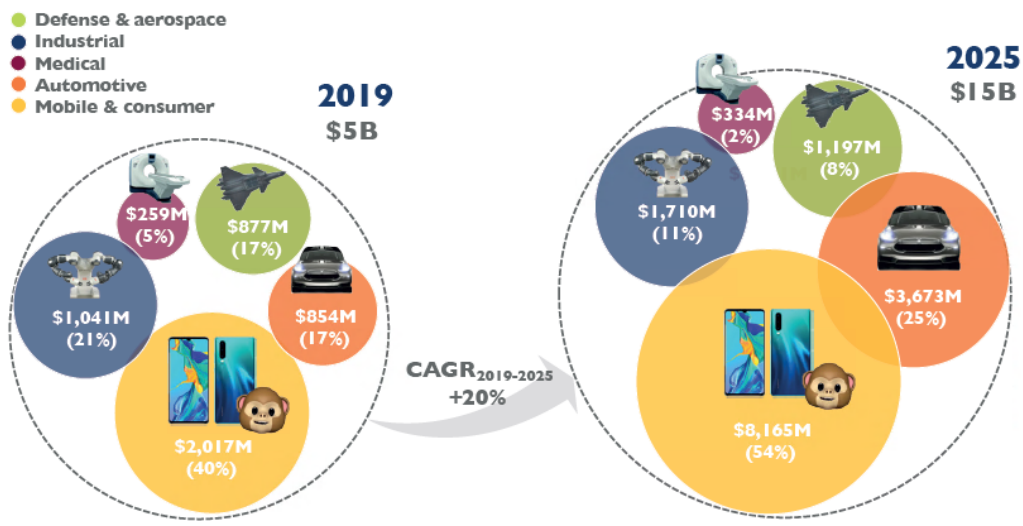


Fig. 1. 3D sensing and imaging – 2019-2025 market forecast (in $M)

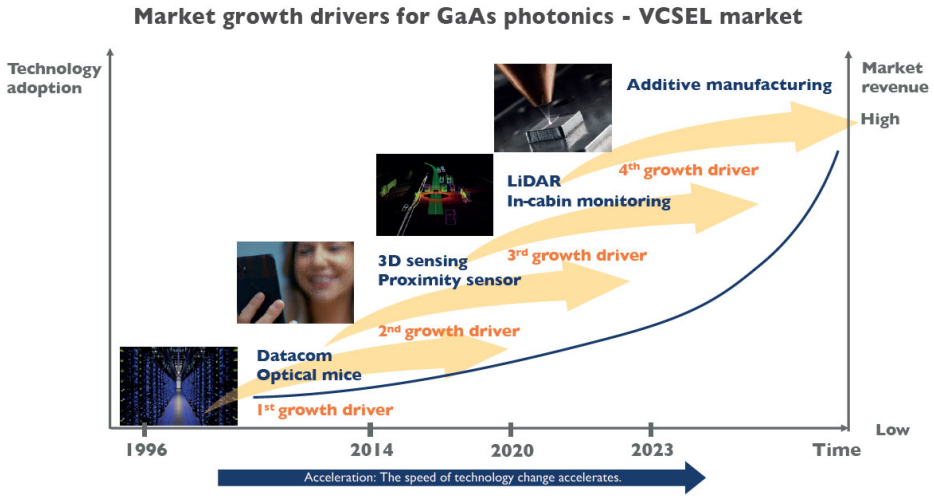


Fig. 2. Market growth drivers for GaAs photonics in VCSEL applications

component in this application, Light Distance and Ranging (LiDAR), is now focused on by a large number of suppliers. There are a wide range of LiDAR technologies to choose from, making the field as a very competitive one.

## GaAs wafer and epiwafer industry

Historically, GaAs wafer and epiwafer market for photonics were relatively small markets mainly focused on datacom applications. However, since the introduction of a 3D-sensing function in the iPhone X by sensing, VCSELs and EELs have great potential to be used in LiDAR technology for automotive applications, where they are both competing for short and mid-range detection. Today, VCSELs have paved the way for the GaAs wafer market to grow at a remarkable CAGR of 18% from 2019 to 2025.

Following the remarkable entry of GaAs VCSELs in the consumer market, the GaAs epiwafer supply chain has been constantly changing. In the photonics market, the epiwafer business model is application dependent. In datacom, it is mostly integrated, dominated by Finisar, Avago and II-VI. However, for 3D sensing and other VCSELs for smartphones, manufacturers prefer to outsource the epitaxy, a more flexible strategy adopted by Apple, which is supplied by IQE. IQE remains the biggest epiwafer supplier, with 61% photonic epiwafer market share in 2019. But, with increased adoption of 3D sensing, numerous players such as VPEC, II-VI Epiworks, Sumitomo Chemicals and Landmark are ramping up their production.

However, the 3D Sensing applications are not the only drivers for GaAs market growth. The direct view display market has seen growth driven by applications such as control rooms, corporate and indoor home theatre. In this context, MicroLED microdisplays emerged as a potential technology that can provide high performance, in terms of brightness, form factor, color and contrast. The fast progress in the prototyping of microLEDs is appealing to many manufacturers. MicroLEDs have the possibility of driving GaAs wafer market growth, with a conservative case of $46M in 2025, and an optimistic case where microLEDs could contribute tenfold more in 2025.

## Conclusions

The increase in VCSEL demand for 3D sensing paved the way for the growth of other high-volume applications such as LiDAR. The rapid evolution in the VCSEL as well as microLED applications, GaAs wafer/epiwafer market industry in coming years in the form of investment, new entrants and mergers and acquisitions (M&A).

## References

[1] Yole Report: “GaAs Wafer & Epiwafer Market: RF, Photonics, LED and PV applications, 2020
[2] Yole Report: : VCSELs – Market and Technology Trends 2020
[3] Yole Report: 3D Imaging & Sensing 2020

## Acronyms

VCSEL: Vertical Cavity Surface Emitting Lasers
EEL: Edge Emitting Lasers
LiDAR: Light Detection and Ranging
ToF: Time-of-Flight
CAGR: Compound Annual Growth Rate
DOE: Diffractive Optical Elements
AGV: Automatic Guided Vehicles
ADAS: Advanced Driver Assistance Systems

# Harnessing the Capacity Model Simulator For a 200mm III-V Greenfield Fab Strategic Planning

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***Keywords: MAXFab, Capacity modelling, Greenfield, CAPEX, Cycle time, Floor Space***

**Abstract**

**This paper discusses how a capacity model, MAXFab™ can be used to quickly calculate CAPEX, Cycle time, floor space, X-factors and tool quantity required to plan for a given demand across a time horizon either for a Greenfield or fab expansion. Data input requirements for the equipment, tool configuration, tool and auxiliary space, tool cost, process flow and others are also discussed. One of the important features of this capacity modelling tool is the ability to also simulate "Learning curve" when the fab is doing pilot, prototype or short loop testing to a mature fab and ramp for production.**

## INTRODUCTION

All models are wrong, but some models are useful. So the question you need to ask is not "Is the model true?" (it never is) but "Is the model good enough for this particular application?" [1]

At the midst of the COVID-19 pandemic, AR/VR applications for consumer use are being aggressively pursued, driving high demands for new LED technologies about to be commercialized. Several of our III-V Clients are developing novel solutions in that space looking to build new greenfield Fabs to satisfy demands. Since most applications rely on first time LED technologies (e.g. MicroLED) we face several challenges right from the beginning. Special equipment, new process flows, funky starting material, and uncertain performance characteristics to name a few. This requires a methodical approach and robust modelling tools to plan such new factories. This abstract will detail a case study completed during the COVID-19 pandemic months with such a Client.

We were tasked to help simulate capacity and CAPEX profiles for a large 200mm greenfield factory that would be able to mass-produce a large number of LED wafers within 10 weeks. Strategic "Go / No Go" decisions and internal risk assessments were dependent on the outcome of our analysis. We began by deploying one of our remote expert teams, well experienced in these types of efforts, and deployed our MAXFab™ Capacity Simulation Suite to overcome this challenge piece by piece.

## OUR WAY-OF-WORK WITH COVID-19 RESTRICTIONS

Due to tough COVID travel restrictions we had to use a new approach to complete this mission in no more than 10 weeks!

1. We set up very effective daily 30min joint Client-MAX check-point team meetings, review progress and gather feedback / data required for simulating capacity scenarios. Further Senior Management team reviews were conducted weekly.
2. We setup a virtual data-room like tracking structure to consolidate all information from the Client for tools, flows, performance factors, demand profiles, and RPT distributions, and provided a revision control tracking system so no information would be lost and all
3. Since many processing parameters were uncertain, each performance parameter source data was thoroughly analyzed by subject matter engineering experts from the Client side for historical variation, limits and constraints and benchmarked with our internal equipment performance databases.
4. For data integrity and completeness, the MAXFab™ suite provided a strict revision control feature that enabled the team to continuously refine every data element while automatically recording each change the user performed and thus saving a ton of administrative tracking of many changes made.
5. Once the model revision was complete and demand profiles uploaded, "what-if" volume ramp scenarios were generated and analyzed to simulate CAPEX, Cycle Time, and OPEX requirements. All model assumptions were documented and capacity detractors such as

waiting time, percentage of lots on hold, rework factors and sampling rates for metrology tools accounted for.

6. User training and licensing took place remotely using the MS Teams® platform and effectively transferred the software suite at the end of the process. Remote support is routinely carried out.

## CAPACITY SIMULATOR OVERVIEW

The integrated capacity model consist of 4 main modules that provide a complete capability to simulate a new greenfield Fab for CAPEX, OPEX, floor space and cycle time constraints. It uses state-of-the-art algorithms to balance capacity and cycle time considerations, and forecasts total space and cost behaviors based on user preference.

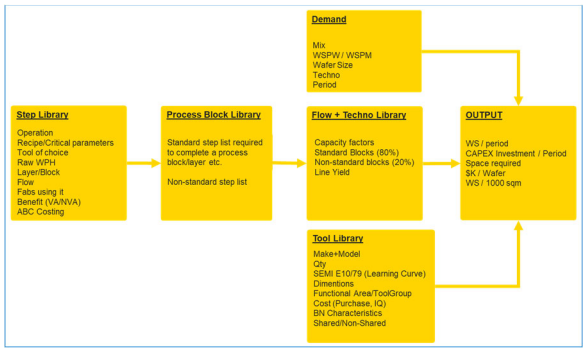


Fig. 1: Modules Overview

## DATA INPUT EASILY DONE

Data input for equipment types, and capacity parameters' assumptions are inputted in the Tool Library module which stores all the tool information, for example, make and model, tool dimension and service space requirement, availability and gap factor, CAPEX for the tool and auxiliary

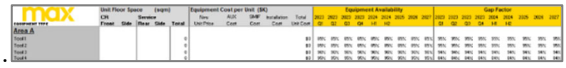

Fig. 2: Tool Library Module

The step and technology libraries module details all the steps required for the product flow. This includes, step name, description, recipe name, tool type assigned, raw process time (RPT) or machine rate (WPH), step type (process or metrology), sampling rate in the case of metrology steps.

| Step ID | Layer | Area | Tool | RPT / Run (m) | UPH | 1/UPH | Wafer Size | Tool ID | Step Description |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Layer1 | Area A | Tool 1 | 200.00 | 3.00 | 0.33 | 200 | ETOO1 | Step description 1 |
| 2 | Layer1 | Area B | Tool 2 | 158.00 | 9.49 | 0.11 | 200 | MABC1 | Step description 2 |
| 3 | Layer1 | Area B | Tool 3 | 70.00 | 21.43 | 0.05 | 200 | MABC2 | Step description 3 |
| 4 | Layer1 | Area B | Tool 4 | 25.00 | 60.00 | 0.02 | 200 | MFNG1 | Step description 4 |
| 5 | Layer1 | Area C | Tool 5 | 12.50 | 120.00 | 0.01 | 200 | HAND1 | Step description 5 |
| 6 | Layer1 | Area B | Tool 6 | 250.00 | 300.00 | 0.00 | 200 | MEPP1 | Step description 6 |

Fig. 3: Step and Technology Libraries Module

Multiple process flows (some call them process routes) can be grouped into Technology level blocks with providing an additional grouping level and toolset-level process parameters such as rework (e.g. for photolithography), load size (for batch processing tools), surge and sampling (for metrology) factors. Technology blocks allow for implementing learning curve assumptions for almost every parameter over a predefined planning horizon. This is critical for simulating Fab efficiency improvements from start-up to full production.

Demand planning and smoothing algorithms are a key feature of this platform. The user can input different demand profiles and instantly refresh the model to display CAPEX and OPEX requirements given cycle time constraints. We will then use this data to analyze CAPEX utilization profiles for each different demand scenario.

| Technology Family | Flow | 2023 Q1 | 2023 Q2 | 2023 Q3 | 2023 Q4 |
|---|---|---|---|---|---|
| A Tech | A Flow 1<br>A Flow 2 | 1,000 | 1,000 | 1,250 | 1,500 |
| B Tech | B Flow 1<br>B Flow 2 | 2,100 | 2,100 | 2,200 | 2,500 |
| Total Tech Family 1 | | 1,000 | 1,000 | 1,250 | 1,500 |
| Total Tech Family 2 | | 2,100 | 2,100 | 2,200 | 2,500 |
| Total | | 3,100 | 3,100 | 3,450 | 4,000 |

Fig. 4 Demand Horizon Module

## BALANCING CYCLE TIME CONSTRAINTS

Cycle time simulations are consistent with the operating curve model (Queueing Theories). They are calculated at the process step level in each flow and give us the most granular view for cycle time contribution at that level. Lot transportation times and percentage of lots on hold are also accounted for to simulate a realistic fab environment. Our model simulates the "price" of balancing output with cycle time performance by limiting utilization gap factors and applying surge factors for selected toolsets (e.g. metrology tools) and therefore increasing their CAPEX investment required. "What-if" analysis comes handy in this case.

## EQUIPMENT CONFIGURATION OPTIMIZATION

While putting data into the tool library or step library may be a mechanical exercise, multi-chamber (cluster) tools require significant optimization to efficiently process all different processes and minimize CAPEX investment. This will eventually minimize spares required per tool, facilitate technician training and

provides a systematic way to increase tools as the fab expands. Our team spent a considerable time working out the right chamber configurations for PVD and Wet chemistry tools which were CAPEX intensive and complex to model. "Mini Throughput" models were developed with the Client engineering team that once completed, a better understanding of clustering was produced and CAPEX utilization was significantly increased.

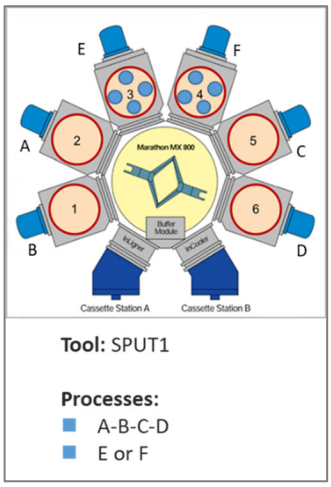


Fig. 5 PVD optimized Tool Configuration

RESULTS

The Client goal was to simulate CAPEX investment requirements for their planned greenfield Fab while understanding OPEX and floor space requirements behaviors. Special attention was given to $$ per wafer and CAPEX Utilization metrics (defined as total CAPEX investment required x equipment utilization x equipment bottleneck index), typically targeted at 85% for a greenfield Fab. In this case, our model ran an incremental CAPEX investment scale for 5,000 to 25,000 WSPW where for each point it determined the CAPEX Utilization vs. target and if it was a CAPEX investment "sweet-spot" or an optimum investment point along that scale. This was extremely important for the team to right-size the Fab and allow for correct business ramp phases as time progressed.

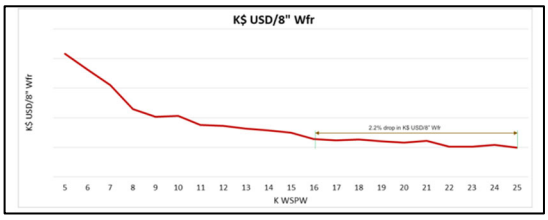


Fig. 6 CAPEX investment / Wafer

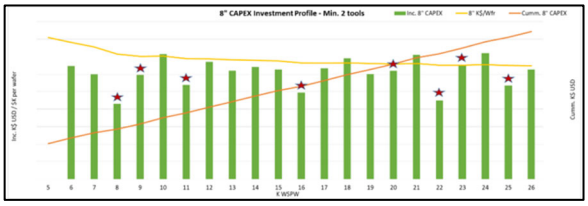


Fig. 7 CAPEX Sweet-Spots

Our model total CAPEX estimates were approximately 20% lower when comparing to initial estimates made by the Client. ~10% CAPEX savings were attributed to the equipment configuration optimization models. This novel way of modelling provides a Step-by-Step approach to CAPEX required for any demand. This itself will easily save ~ 40% of man-hours if calculating from scratch.

CONCLUSIONS

Using a collaborative way-of-working to successfully deliver accurate, complete and timely Fab sizing parameters during this "new normal", we had to enhance our robust simulation tool so we could input data quickly, it could be easily understood by any person not even totally familiar with these types of modelling tools, and have it integrating a complete view of CAPEX, OPEX and floor space requirements for the new greenfield Fab. We delivered a CAPEX profile at an 83-85% CAPEX utilization, and easily saved about 50% of the typical personnel-hours required to build this type of a simulator.

REFERENCES

[1] Box, G., Luceño, A., Paniagua-Quiñones, C. M. d. *Statistical Control By Monitoring and Adjustment*. Wiley 2009.

ACRONYMS

AR/VR: augmented reality / virtual reality
LED: light emitting diode
RPT: raw process times
CAPEX: Capital Expenditures
OPEX: Operating Expenditures
WPH: Wafers per Hour
PVD: Plasma Vapor Deposition
WSPW: Wafer Starts per Week

# SESSION 8:
# MATERIALS AND CHARACTERIZATION

# Demonstration of High-quality GaN Epitaxy on 200 mm Engineered Substrates for Vertical Power Device Fabrication

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**Keywords: Vertical trench MOSFET, GaN, engineered substrates**

**Abstract**

**Engineered substrates with a poly-AlN core, thermally matched to GaN, are promising to reconcile the use of high-yield GaN wafers with thick buffers on large scale substrates (≥ 200 mm). We demonstrate crack-free 5.4 µm-thick high quality GaN epitaxial layers grown on 200 mm substrates, with a good control of wafer bow and a PN-junction that reaches 440 V. A semi-vertical trench gate MOSFET device architecture has been used to demonstrate the excellent device performance in ON-state, reaching 1.2 kA/cm$^2$ and a low on-resistance of 5.7 mΩ·cm$^2$. A next generation epitaxial stack has been developed approaching 1.5×10$^{16}$ cm$^{-3}$ net doping concentration in the n-drift layer combined with a very good and uniform crystal quality, with the GaN <102> peak as low as 400 arcsec.**

## INTRODUCTION

Engineered substrates are promising to extend the voltage range beyond 650 V on large area substrates with thick GaN layers, while avoiding wafer breakage during device fabrication. Qromis Substrate Technology (QST®) has been a pioneer in this regard and commercially offers 200 mm engineered substrates with SEMI standard thickness. The QST® substrate consists of a polycrystalline ceramic core (poly-AlN), covered by several encapsulation layers, on top of which is a $SiO_2$ bonding layer and a single crystalline Si layer which serves as the nucleation layer for the MOCVD growth [1].

The fabrication of vertical GaN devices for high voltage applications has been reported on Si substrates up to 150 mm diameter [2]. To further scale up both the substrate size and GaN stack thickness on Si, is extremely challenging, due to the mismatch in thermal expansion coefficient and lattice constant between GaN and Si. With the use of these engineered substrates, the path towards vertical GaN device fabrication on large diameters is enabled, with scalability potential up to 300 mm. In literature, high quality GaN layers with vertical transistor and diode processing are demonstrated on GaN substrates [3-5], but only small area substrate sizes are available to date, with a very high substrate cost [6]. Compared to Si, the engineered substrate with poly-AlN core is a better candidate to grow high quality epitaxial GaN layers on large area substrates, since it is matched to GaN in the coefficient of thermal expansion. On engineered substrates, lateral pGaN gate HEMT devices have been demonstrated up to 650 V [7,8]. Scaling up this voltage will further increase the footprint of lateral HEMT devices, due to the need to increase gate to drain spacing, which will also affect the on-state performance of the fabricated devices. In vertical transistors, with the electric field vertically distributed over the GaN epitaxial stack the footprint of the device is independent of the target voltage, which makes this technology very suited for high voltage applications.

In this work, we demonstrate high quality GaN epitaxy on 200 mm engineered substrates for vertical device fabrication. In a first section, the GaN epitaxy is described showing also the voltage blocking capability of the PN-junction. Subsequently, the trench gate MOSFET device fabrication and ON-state performance of the device are reported.

## GAN EPITAXY

Crack free 5.4 µm-thick GaN layers (Fig. 1.(a)) were grown by means of MOCVD using an AIX G5+ C Planetary Reactor® from AIXTRON, Germany. The 5×200 mm mini-batch reactor combined with cassette-to-cassette configuration allows for a high productivity while maintaining a very low number of particles for optimal yield. The stack consists of a 200 nm AlN nucleation layer, a strain-compensating buffer, a 1 µm uid GaN layer for defect reduction, a 750 nm n$^+$-GaN bottom contact, a 3 µm-thick n$^-$ GaN drift layer, a 400 nm Mg-doped p-GaN layer and a 200 nm n$^+$-GaN top contact layer. Owing to the CTE-matched substrate and the choice of the epi stack, bow tuning below |50| µm can be achieved independent of the drift layer thickness. This is exemplarily shown in Fig. **1**.(b) for the stack depicted in Fig. **1**.(a). The good control of wafer bow enables device processing in a 200 mm process line, compatible with CMOS technology.

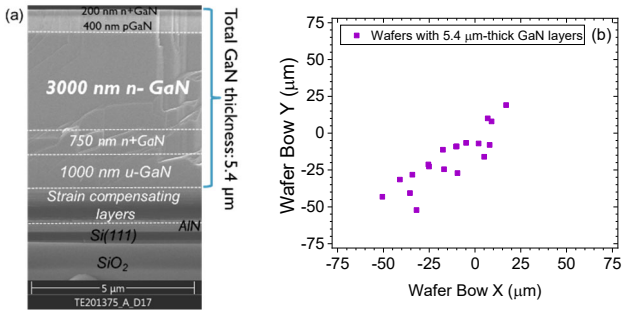



Fig. 1. (a) Cross-sectional SEM image and (b) wafer bow of 200 mm engineered substrates with 5.4 µm-thick GaN.

A SIMS analysis of the stack, depicted in Fig. 2, provides details on the chemical concentration of the individual layers. The $n^+$-GaN layers are doped with 5.5 $\times 10^{18}$ Si/cm$^3$. The pGaN layer has a $1.2\times10^{19}$ Mg/cm$^3$ doping level, with a net p-doping of $2\times10^{18}$ cm$^{-3}$. The drift layer has a Si doping level of $4\times10^{16}$ cm$^{-3}$ with a C background level of 1.5 $\times 10^{16}$ cm$^{-3}$.

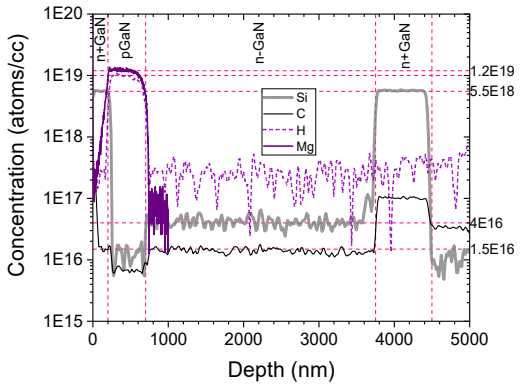



Fig. 2. SIMS analysis of doped GaN layers in grown GaN stack.

From Hall measurements an active n-type concentration of roughly $2.15\times10^{16}$ cm$^{-3}$ and a moderate drift layer mobility of around 473 cm²/ (V.s) was extracted (TABLE I). For the Hall measurements a test structure was grown with identical layers as the device stack up to the $n^-$ drift layer, apart from the $n^+$-GaN buried layer, which was replaced by a uid-GaN layer, to make the Hall measurement possible.

TABLE I
CHARACTERISTICS $n^-$ DRIFT LAYER, EXTRACTED FROM HALL MEASUREMENTS

| n (cm$^{-3}$) | ρ (Ω·cm) | µ (cm²/ (V.s)) |
|---|---|---|
| $2.15\times10^{16}$ | 0.62 | 473 |

For the epi stack as presented in Fig. **1** with an $n^-$ drift layer containing a Si doping of $4\times10^{16}$ Si/cm$^3$ and a good crystal quality, the PN-junction reaches ~440 V in reverse bias, as depicted in Fig. 3.

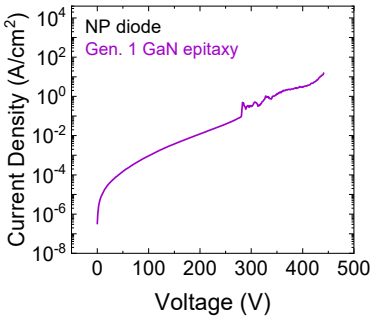



Fig. 3. Reverse J-V characteristic of PN-diode reaching 440 V, for the Gen.1 GaN layer stack.

Further work on GaN epitaxy has been executed, demonstrating a much-improved crystal quality and uniformity, illustrated by the XRD FWHM values in Fig. 4.(a), comparing 2 generations of GaN epitaxial layers, both with a 3 µm-thick drift layer, achieving a FWHM value as low as 400 arcsec for the GaN <102> peak, for the generation 2 stack. The amount of edge type dislocations in a stack is directly linked to crystal quality observed in the GaN<102> peak [9]. When comparing the generation 1 and generation 2 epitaxial stack, we were able to shrink the edge type dislocations by 30% in the center and 60% in both halfway and edge area of the wafer, resulting in an estimated amount of 4-5x10$^8$ cm$^{-2}$, as depicted in Fig. 4 (b). The improved crystal quality for the generation 2 epitaxy was obtained, by an adaptation of the Al containing strain compensating layers in the bottom of the stack. Furthermore, a decrease of Si doping level in the $n^-$ drift layer to $2\times10^{16}$ cm$^{-3}$ was achieved, in combination with a very good suppression of the Carbon background doping, below 1x10$^{16}$ cm$^{-3}$. These improvements are expected to further boost the voltage blocking capability of the PN diode in future work.

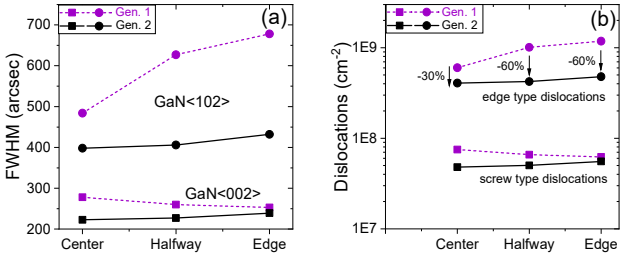
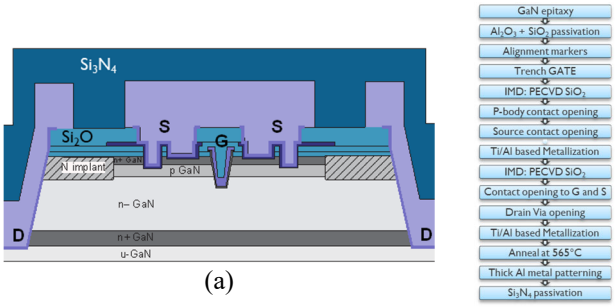



Fig. 4. (a) XRD FWHM of GaN <102> and GaN <002> peaks, (b) estimated number of dislocations for the Gen. 1 and 2 GaN layer stacks.

## DEVICE FABRICATION

A semi-vertical trench gate MOSFET device was fabricated as test vehicle to demonstrate the device performance in ON-state. The electrons flow from the source to the inversion channel in p-GaN, through the $n^-$ drift layer and are then collected via an $n^+$-GaN layer with a drain contact

at the frontside of the wafer. A schematic representation is given in Fig. 5.(a).




(a) (b)

Fig. 5. (a) Pictorial representation and (b) process sequence order for trench gate MOSFET device.

First a thin $Al_2O_3$ and $SiO_2$ layer is deposited as surface passivation. The $n^+$-GaN and p-GaN top layers are isolated from the drain by an N implant. Next the trench gate is processed. The dry etch and wet etch steps have been optimized, resulting in a smooth gate trench sidewall [10], as depicted in Fig. 7.(a). The gate architecture is then further processed with a 2.5 nm $Al_2O_3$ and a 50 nm $SiO_2$ bilayer dielectric finishing with a TiN/Ti/Al based gate metal stack on top. The contacts to the source $n^+$-GaN, p-body and drain $n^+$-GaN layers are made using thin Ti/Al containing metal stacks. An anneal at 565°C is used for the Ohmic contact formation, after the drain metallization and patterning is processed, as shown in the process sequence in Fig. 5. The metallization is finished with a 4 µm-thick Al metal stack on top of the source and drain fingers and in the bond pad areas. By letting the thick power metal run over the gate, a minimum $L_{SG}$ of 1.25 µm could be used in the design, which is beneficial for the ON-state performance of the devices. Finally, the device is finished with a 2 µm-thick $Si_3N_4$ passivation layer. In Fig. 6 a SEM image of the cross section of the active area of the processed device is depicted, with 2 source fingers and the trench gate architecture in the center. The buried $n^+$-GaN layer is connected from the frontside, which is depicted in a cross-sectional SEM image in Fig. 7.(b).

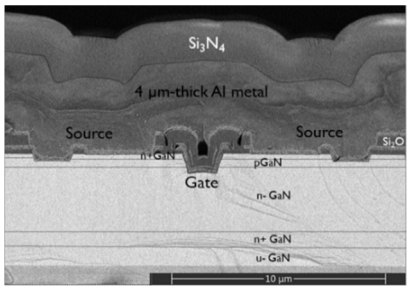



Fig. 6. Cross-sectional SEM image of the active area of the trench gate MOSFET device, depicting the gate and source regions.

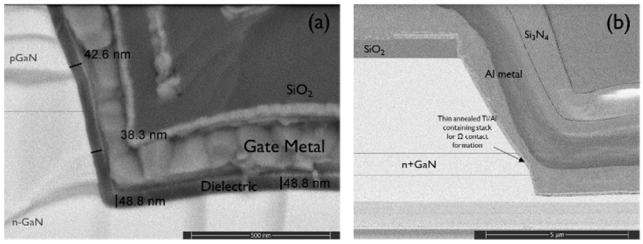



Fig. 7. Cross-sectional SEM image depicting (a) a zoom-in of the gate trench corner with a smooth GaN side wall, (b) a drain contact to the buried $n^+$-GaN layer, which is made from the frontside of the wafers.

## ON-STATE PERFORMANCE

Multi-finger devices with a total effective gate width of 60 mm and an active area of 0.56 $mm^2$ were electrically characterized, and typical output and transfer characteristics are depicted in Fig. 8. The transistors exhibit a high drive current of 1.2 $kA/cm^2$ and a low on-resistance of 5.7 $m\Omega \cdot cm^2$ (normalized by the active area). The threshold voltage is 2 V.

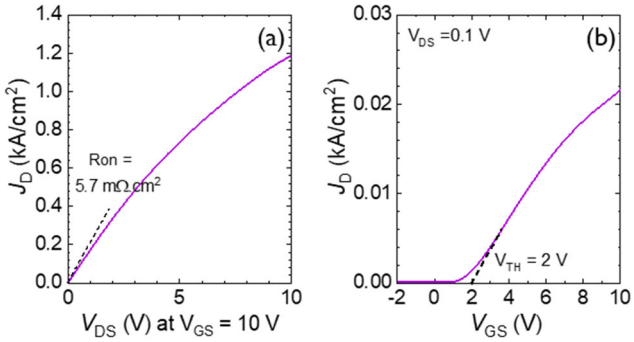



Fig. 8. Typical (a) output and (b) transfer characteristic of trench gate MOSFET device.

## CONCLUSIONS

We demonstrated crack-free 5.4 µm-thick high quality MOCVD-gown GaN epitaxial layers on 200 mm engineered substrates, with a good control of wafer bow and a diode blocking capability of 440 V. A next generation epitaxial stack has been developed approaching $1.5\times10^{16}$ $cm^{-3}$ net doping concentration in the $n^-$ drift layer combined with a very good and uniform crystal quality, with the GaN <102> peak as low as 400 arcsec. A semi-vertical trench gate MOSFET device architecture has been used to demonstrate the excellent device performance in ON-state, reaching 1.2 $kA/cm^2$ and a low on-resistance of 5.7 $m\Omega \cdot cm$.

ACKNOWLEDGEMENTS

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REFERENCES

[1] V. Odnoblyudov et al., U.S. Patent, 15, 621,335, 15 Feb 2018.

[2] R. A. Khadar et al., "Fully Vertical GaN-on-Si power MOSFETs," in *IEEE Electron Device Letters*, vol. 40, no. 3, pp. 443-446, March 2019, doi: 10.1109/LED.2019.2894177.

[3] W. Li et al., "Development of GaN Vertical Trench-MOSFET With MBE Regrown Channel," in IEEE Transactions on Electron Devices, vol. 65, no. 6, pp. 2558-2564, June 2018, doi: 10.1109/TED.2018.2829125.

[4] H. Ohta *et al*., "Vertical GaN p-n Junction Diodes With High Breakdown Voltages Over 4 kV," in *IEEE Electron Device Letters*, vol. 36, no. 11, pp. 1180-1182, Nov. 2015, doi: 10.1109/LED.2015.2478907.

[5] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty and D. Bour, "Vertical Power p-n Diodes Based on Bulk GaN," in IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 414-422, Feb. 2015, doi: 10.1109/TED.2014.2360861.

[6] Y. Zhang et al., "Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes." IEEE Transactions on Electron Devices 62, no. 7 (July 2015): 2155–2161.

[7] K. Geens *et al*., "650 V p-GaN Gate Power HEMTs on 200 mm Engineered Substrates," in *IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Raleigh, NC, USA, 2019, pp. 292-296, doi: 10.1109/WiPDA46397.2019.8998922.

[8] X. Li *et al*., "Integration of 650 V GaN Power ICs on 200 mm Engineered Substrates," in *IEEE Transactions on Semiconductor Manufacturing*, vol. 33, no. 4, pp. 534-538, Nov. 2020, doi: 10.1109/TSM.2020.3017703.

[9] M.A. Moram and M.E. Vickers, "X-Ray diffraction of III-nitrides," in reports on progress in Physics, vol. 72, no. 3, Feb. 2009.

[10] P. Diehle et al., "Root cause analysis of gate shorts in semi-vertical GaN MOSFET devices," in The 13th International Conference on Advanced Semiconductor Devices And Microsystems (ASDAM), Smolenice, Slovakia, November 2020, pp. 10-13.

ACRONYMS

MOSFET: metal–oxide–semiconductor field-effect transistor
SEMI: Semiconductor Equipment and Materials International
CMOS: complementary metal-oxide-semiconductor
MOCVD: Metal-organic chemical vapor deposition
uid-GaN: unintentionally doped GaN
SEM: Scanning Electron Microscope
SIMS: Secondary-ion mass spectrometry
XRD: X-ray diffraction
FWHM: Full width at half maximum of XRD profiles
$L_{SG}$: Source-to-Gate Length

# Evaluation of novel iron-free QuanFINE® structure by 100nm and 150nm AlGaN/GaN HEMT technology

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**Keywords: Epitaxy, AlGaN/GaN, QuanFINE®**

**Abstract:**

**This work evaluates SweGaN's novel QuanFINE® structure with the UMS 100 / 150nm GaN-HEMT technology, in comparison to GH15-10 reference material based on AlGaN/GaN grown on a thick Fe-doped buffer. Characterizations focus on electrical DC- and RF-parameters obtained on process control monitors after front side processing and first robustness assessment by DC-step stress testing.**

## INTRODUCTION

Conventional AlGaN/GaN structures are typically grown on semi-insulating SiC substrates using a 1µm to 2µm C- or Fe-doped GaN buffer layer. The thick buffer layer is mandatory to reduce growth defects resulting from lattice mismatch to the substrate material. Isolation and therefore confinement of the 2DEG in the GaN channel is realized by the dopants forming deep acceptor traps [1,2]. Unfortunately, these traps have been identified as a source of DC- and RF-dispersion effects [3,4] such as drain- or gate lag which limits RF-performance as well as introduce unwanted memory effects with long time constants. SweGaN recently introduced a "buffer-free" GaN-on-SiC HEMT structure [5] demonstrating competitive RF-performance using a 250nm gate length HEMT technology. Here, the AlN nucleation layer acts as a back barrier of an unintentionally doped sub micrometer GaN layer.

In this work UMS has extended the evaluation of the QuanFINE® structure to reduced gate lengths of 100nm through comparison to conventional AlGaN/GaN structure based thick Fe-doped buffer material.

## EXPERIMENTAL

### *Description*

QuanFINE® features an iron-free HEMT hetero-structure with GaN channel (<250 nm), where electrons are confined in a 2DEG between the front-side and backside barrier formed by the AlN nucleation layer. To evaluate this structure for gate lengths down to 100nm, the channel thickness has been reduced from sample A to C. The barrier structure is similar to the reference sample in all cases. Table I summarizes the key electrical epitaxy properties, where QuanFINE® structures compare well to conventional AlGaN/GaN reference material based on a thick Fe-doped buffer.

Wafers were fabricated at UMS using the qualified high-performance GH15-10 GaN-HEMT technology. To assess the pinch off properties of HEMT devices, the gate length was varied between 150nm and 100nm using the UMS dielectric assisted gate technology to realize a slanted gate-foot profile.

TABLE I KEY EPITAXY PARAMETERS.

| Sample | A | B | C | Ref |
|---|---|---|---|---|
| Rsheet (Ω/sq) | 289.2 σ=0.8 | 294.7 σ=0.5 | 294.2 σ=1.1 | 295.8 σ=2.0 |
| µ (cm²/Vs) | 2090 | 2074 | 2138 | 1960 |
| Ns (1/cm²) | 1.1+e13 | 1.0e+13 | 1.0e+13 | 1.1e+13 |

### *Results*

After front-side processing, manual and automatic electrical characterization was undertaken on process control modules uniformly distributed over the 4" wafer.

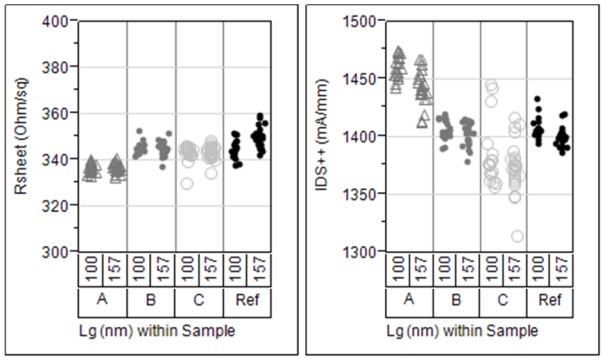


Fig. 1. Sheet resistance (l) and maximum drain saturation current (r) at VDS = 7V, VGS = +3V.

As shown in the left part of Fig 1, the sheet resistance from TLM measurements of QuanFINE® epitaxy is similar to the reference material. The maximum drain current density IDS++ depends on the QuanFINE® channel thickness and demonstrates a similar level for sample-B compared to the reference (Fig. 1, right).

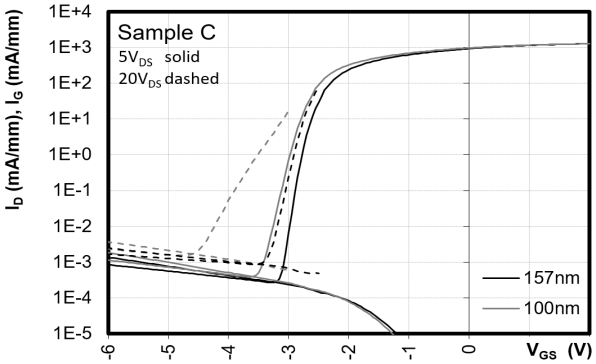


Fig. 2. Sub threshold characteristics of sample-C.

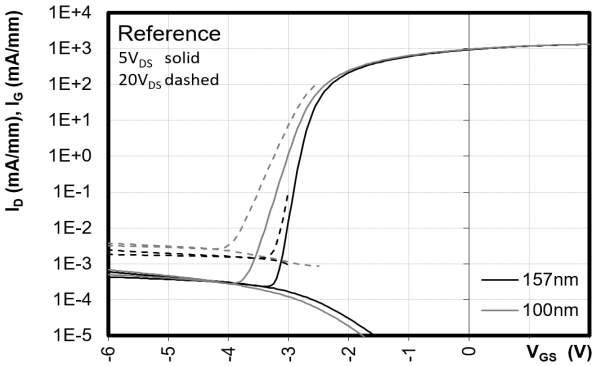


Fig. 3. Sub threshold characteristics of the reference.

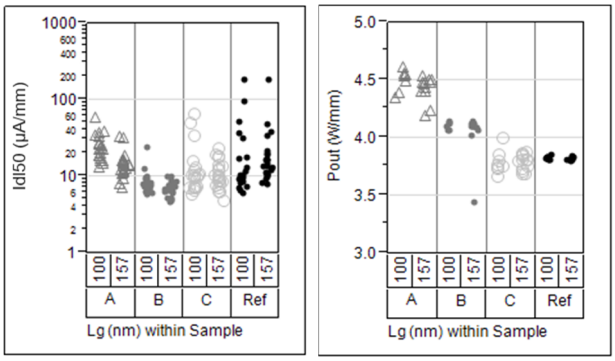


Fig. 4. Drain leakage (l) at VDS = 50V, VGS = -7V and 9GHz RF-output power density (r) on 8x75µm device operated at VDS = 20V.

The comparison of pinch off behavior for sample-C (Fig 2) with the thinnest channel and the reference (Fig 3) is shown for both gate lengths for VDS = 5V and 20V. While similar properties are observed for the nominal gate length devices, a clean pinch off behavior becomes difficult to achieve for sample-C for 100nm gate lengths. However, drain leakage density remains well below 100 µA/mm at Vds = 50V on all samples as shown in the left part of Fig 4. Transistor saturated RF-output power at 9GHz and 20V drain bias between 3.7 and 4.5 W/mm (Fig 4, right) shows a good correlation for samples A-C with the maximum drain saturation current in Fig 1.

Large-signal RF power sweeps in a 50Ω environment at VDS = 20V and low quiescent bias (Idq = 50mA/mm) are used to identify weak channel charge confinement, indicated by gain expansion between low (-5dBm) and high (+15dBm) input powers as shown in Fig 5 and Fig 6. Sample-B and C are stable for 150nm gate lengths, however sample-A with the thickest channel, shows gain expansion of approximately 1dB. For a 100nm gate length, sample-C shows more than 1dB gain expansion, confirming marginal charge confinement, as already expected from sub-threshold characteristics (Fig 2).

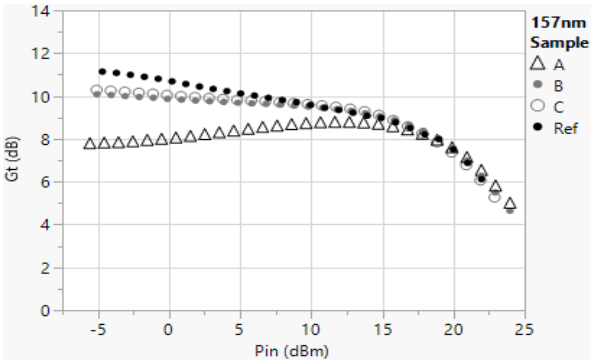


Fig. 5. 50Ω power sweep at 9GHz on 8x75µm FET with 150nm gate length operated at VDS = 20V/Idq = 50mA/mm.

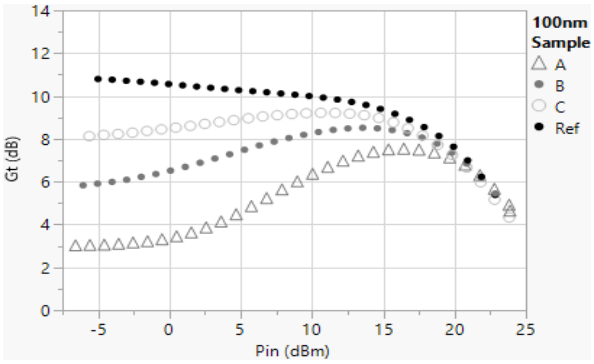


Fig. 6. 50Ω power sweep at 9GHz on 8x75µm FET with 100nm gate length operated at VDS = 20V/Idq = 50mA/mm.

To assess device robustness wafer level reliability tests on 150nm gate length at 150°C back plate temperature have been undertaken on 2x40µm devices operated in a pinched-off condition at VGS = -7V and application of an increasing VDS between 30V and 120V in 10V steps with intervals of 30 minutes for each step. Devices were characterized between each step. The evolution of the drain saturation current IDSS at VDS = 7V, VGS = 0V and the pinch off voltage VG100 at 1% of IDSS are shown in Figures 7 and 8, respectively for

this test. The reference device reveals a slight decrease in drain saturation current and positive shift in pinch off before failing at Vds = 100V, which is in accordance to the limitation of the thick Fe-doped buffer for the given device geometry of the test structure. All QuanFINE® devices pass the step stress test until the limit at 120V without failure and independent of channel thickness, indicating improved device robustness due to the novel epitaxial structure. Drift of the drain saturation current and the pinch off voltage are similar for samples A-C, where absolute values correlate with the channel thickness. However, drift of the pinch off is more pronounced on the QuanFINE® devices and may relate to charging effects in the AlN nucleation layer. Anomalies in pinch off voltages at Vds = 80V and 110V on sample A and B were not found to be systematic on the four stressed devices per wafer. No such behavior was observed on sample C with the thinnest channel or the reference material. Additional statistics for device robustness and life tests in package are required for better understanding of device stability.

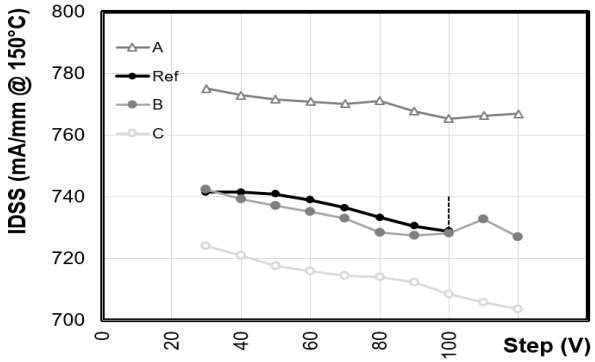


Fig. 7. Drain saturation current IDSS at VDS = 7V, VGS = 0V at 150°C after each step of DC-step stress testing in pinched conditions at VGS = -7V and 30min per VDS-step.

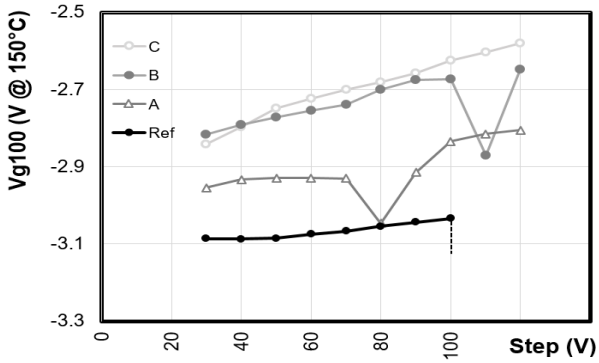


Fig. 8 Pinch off voltage VG100 at 1% of IDSS at 150°C after each step of DC-step stress testing in pinched conditions at VGS = -7V and 30min per VDS-step.

## CONCLUSIONS

This paper reports first HEMT device performance using SweGaNs novel "iron-free" QuanFINE® material in conjunction with the UMS high performance GH15-10 (150nm gate length) technology [6, 7]. Medium channel thickness material demonstrated excellent performance compared to conventional AlGaN/GaN reference material based on a thick Fe-doped buffer on SiC substrate. Initial indications show improved device robustness under high Vds and pinched-channel conditions. Charge confinement could be further improved by reducing the channel thickness; however, further material optimization is necessary to reduce RF gain expansion for very short gate lengths devices (100nm). Although more analysis is required to compare the RF-performance at 30GHz, memory effects and the long-term performance of packaged devices, SweGaN material QuanFINE® is seen as a very promising alternative to the conventional thick Fe-doped buffer layers in next generation GaN HEMT design.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] S. Heikman et al., *Growth of Fe doped semi-insulating GaN by metalorganic chemical vapor deposition*, Appl. Phys. Lett., vol. 81, no. 3, p. 439, 2002.

[2] X-Li et al., *Carbon doped GaN buffer layer using propane for high electron mobility transistor applications: Growth and device results*, Appl. Phys. Lett., vol. 107, no. 26, Dec. 2015.

[3] M. Meneghini et al., *Buffer Traps in Fe-Doped AlGaN/GaN HEMTs: Investigation of the Physical Properties Based on Pulsed and Transient Measurements*, IEEE Transactions on Electron Devices, vol. 61, no. 12, pp. 4070-4077, Dec. 2014.

[4] Sebastian Gustafsson et al., *Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs With Carbon-Doped Buffer,* IEEE Transactions on Electron Devices, Vol 62, No. 7 pp. 2162-2169, July 2015.

[5] D.-Y. Chen et al., *Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors*, IEEE Electron Device Letters. Vol 41, No. 6 pp. 828-831, June 2020.

[6] V. Di Giacomo-Brunel et al., *Industrial 0.15-µm AlGaN/GaN on SiC Technology for Applications up to Ka Band*, 13th EuMIC Madrid (Spain). pp. 1-4, Sept. 2018.

[7] M. Dinari et al., *Three Stage 5-18.5 GHz High Gain and High Power Amplifier Based on 0.15 µm GaN Technology*, 13th EuMIC Madrid (Spain). pp. 81-84, Sept. 2018.

## ACRONYMS

DC: Direct Current
2DEG: 2-Dimensional Electron Gas
HEMT: High Electron Mobility Transistor
Ref: Reference sample
RF: Radio Frequency
UMS: United Monolithic Semiconductors

# Thin $Al_{0.5}Ga_{0.5}N$/GaN HEMTs on QuanFINE® Structure

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**Keywords: RF, AlGaN, GaN, HEMTs, QuanFINE®, and Short channel effect.**

## Abstract

**The performance of HEMTs fabricated on a thin $Al_{0.5}Ga_{0.5}N$/GaN heterostructure with a total barrier thickness of 6.5 nm is presented and benchmarked to the epi-structure with a 13 nm thick $Al_{0.3}Ga_{0.7}N$ barrier on an identical QuanFINE® structure. DC transfer characteristics on both samples with a gate length of 100 nm demonstrate a high current above 1 A/mm. A higher extrinsic $g_m$ of 550 mS/mm is measured on the sample with a thinner high Al content barrier. Moreover, low trapping effects with a 12-14 % buffer-related dispersion at a $V_{DSQ}$ of 25 V are characterized for both samples, which indicate the advantage of the iron-free QuanFINE® heterostructure.**

## Introduction

GaN HEMTs are gaining attention in the applications of high-frequency devices due to high breakdown voltage and high electron mobility, which yield a high power density with good efficiency. AlGaN barrier with a thickness above 10 nm and the Al composition beneath 30 % is commonly utilized for GaN HEMTs [1]. However, the transconductance ($g_m$) is limited due to the thick barrier layer. Therefore, a thinner AlGaN barrier with higher Al content (>30 %) is proposed to improve gate response [2]. Lattice-matched InAlN barrier is another approach to reduce the barrier thickness, which has a higher 2DEG density than the AlGaN barrier thanks to a stronger polarization force. However, plausible Indium aggregation in the barrier might limit the reliability of devices [3].

The buffer is conventionally Fe or C doped to render good isolation [4]. However, devices made on Fe- or C-doped buffers suffer from trapping effects. Recently, a novel QuanFINE® heterostructure, which has a thin UID-GaN layer sandwiched in between a barrier and an AlN nucleation layer, potentially allows the AlN nucleation layer to act as a back-barrier and to reduce the trapping effects [5, 6].

In this study, the first demonstration of a high Al-containing thin $Al_{0.5}Ga_{0.5}N$ barrier on a QuanFINE® structure was investigated. Device fabrication with DC and pulsed-IV characterization will be presented.

## Epi-Growth

The epitaxial layers were grown on a semi-insulating SiC substrate utilizing a MOCVD by SweGaN. Using SweGaN proprietary epitaxial growth process, a low thermal-boundary-resistance AlN nucleation layer was grown and followed with a 250 nm UID-GaN layer [5, 6]. On top of this, a 5.0 nm $Al_{0.5}Ga_{0.5}N$ layer (1.5 nm AlN exclusion layer and 3.5 nm $Al_{0.5}Ga_{0.5}N$ layer), and a 1.5 nm GaN cap layer were grown as the active layers (denoted as $Al_{50}$, Fig. 1a). A $n_s$ of $1.22 \cdot 10^{13}$ $cm^{-2}$ and a $\mu_e$ of 1700 $cm^2/V \cdot s$ were characterized by contactless Hall measurements (Lehighton) and $R_{sh}$ of 315 Ω/sq was characterized by Eddy current measurement after epitaxial growth. These values demonstrate the good 2DEG properties achievable with a thin $Al_{0.5}Ga_{0.5}N$ barrier on QuanFINE®-structure. The other epi-structure which has an 1 nm AlN exclusion layer, a 10 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, and a 2 nm GaN cap layer with a $n_s$ of $1.16 \cdot 10^{13}$ $cm^{-2}$, $\mu_e$ of 2030 $cm^2/V \cdot s$, and $R_{sh}$ of 286 Ω/sq was grown on nominal QuanFINE®-structure (denoted as $Al_{30}$, Fig. 1b) to benchmark to $Al_{50}$. [6]

## Device Fabrication

The epi-wafers were cleaned by the RCA cleaning process followed by a passivation-first 60 nm thick SiN layer deposited by LPCVD before device processing. Mesa etching was defined for device isolation and the ohmic contacts were achieved by deeply recessed Ta-based metal stacks [7]. A low $R_c$ of ~0.3 Ωmm for both samples is characterized by TLM measurements. Two-fingers gates with passivation-assisted field plates, which have an $L_g$ of 100 nm and a gate width of 2x50 µm were defined by e-beam lithography with metal evaporation followed by lift-off process (Fig. 1).

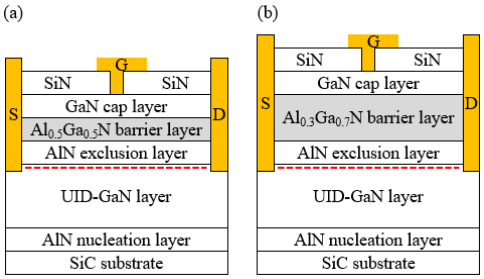


Fig. 1. Schematic of device layout for (a) $Al_{50}$ and (b) $Al_{30}$.

## HEMTs Results

Different I-V measurement windows ($V_{GS}$) were performed on two samples due to the shifting of $V_{TH}$. HEMTs on both samples show a high $I_{DS}$ of ~1.1 A/mm (Fig. 2). A higher extrinsic $g_m$ of 550 mS/mm and a $V_{TH}$ of -0.9 V were measured on $Al_{50}$ as compared to that on $Al_{30}$ with a $g_m$ of 500 mS/mm and a $V_{TH}$ of -1.8 V (Fig. 3) [6], which are mainly caused by a thinner AlGaN barrier. Short channel effects are revealed on $Al_{50}$ and $Al_{30}$ at high drain bias with an average DIBL shifting of 82 mV/V, and 50 mV/V, respectively, extracted at the $I_{DS}$ of 1 mA/mm, while over the range of measured $V_{DS}$ from 1 to 25 V (Fig. 4). A higher leakage current was measured on $Al_{50}$, which might be caused by a thinner barrier with a different Schottky barrier condition. These results indicate that further buffer confinement and mitigation of leakage currents are required for short gate length devices.

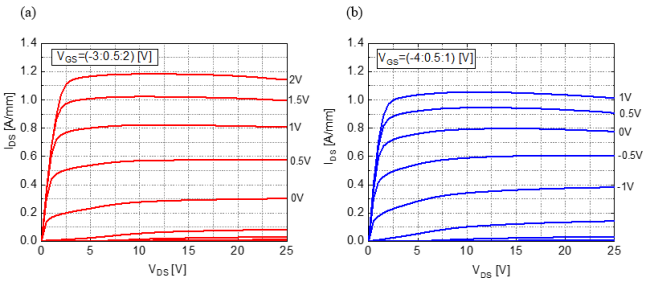


Fig. 2. I-V measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

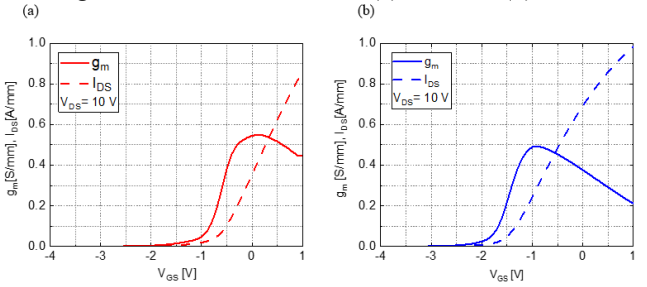


Fig. 3. $g_m$ measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

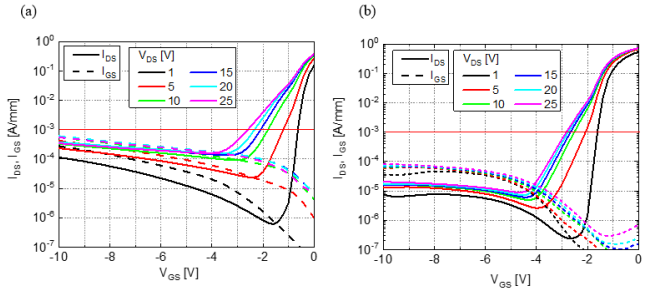


Fig. 4. DIBL measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

A low surface-related current collapse of 0.5 % and 4 % were measured on $Al_{50}$ and $Al_{30}$, respectively, which indicate that the LPCVD SiN passivation is compatible with different barrier design (Fig. 5). Moreover, low buffer-related dispersion of 12 % and 14 % for $Al_{50}$ and $Al_{30}$, respectively, highlight the advantage of using QuanFINE®, which removes the intentional iron and carbon dopants in GaN.

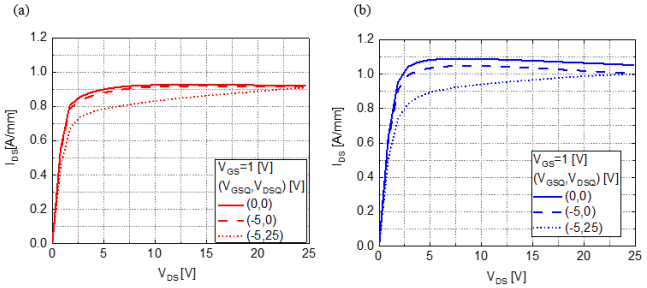


Fig. 5. Pulsed-IV measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

## Conclusions

A 50% Al content thin AlGaN barrier is successfully grown on QuanFINE® heterostructure with excellent 2DEG properties. High $I_{DS\text{-}sat}$ and $g_m$ combined with low trapping effects can potentially translate to a better large-signal RF performance. Further improvements of the 2DEG confinement from the backside such as inserted AlGaN back-barrier and/or reduced UID-GaN layer thickness of QuanFINE® are required for highly down-scaled HEMT technologies.

## Acknowledgments

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## References

[1] J. Bergsten *et al.*, "AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor," *Japanese Journal of Applied Physics,* vol. 55, no. 5S, p. 05FK02, 2016.

[2] T. Zimmermann *et al.*, "AlN/GaN insulated-gate HEMTs with 2.3 A/mm output current and 480 mS/mm transconductance," *IEEE Electron Device Letters,* vol. 29, no. 7, pp. 661-664, 2008.

[3] A. Malmros *et al.*, "Impact of channel thickness on the large-signal performance in InAlGaN/AlN/GaN HEMTs with an AlGaN back barrier," *IEEE Transactions on Electron Devices,* vol. 66, no. 1, pp. 364-371, 2018.

[4] J. Bergsten *et al.*, "Electron trapping in extended defects in microwave AlGaN/GaN HEMTs with carbon-doped buffers," *IEEE Transactions on*

*Electron Devices,* vol. 65, no. 6, pp. 2446-2453, 2018.
[5] J.-T. Chen *et al.*, "A GaN–SiC hybrid material for high-frequency and power electronics," *Applied Physics Letters,* vol. 113, no. 4, p. 041605, 2018.
[6] D.-Y. Chen *et al.*, "Microwave Performance of 'Buffer-Free'GaN-on-SiC High Electron Mobility Transistors," *IEEE Electron Device Letters,* vol. 41, no. 6, pp. 828-831, 2020.
[7] Y.-K. Lin *et al.*, "A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs," *Semiconductor Science and Technology,* vol. 33, no. 9, p. 095019, 2018.

ACRONYMS

HEMTs: High electron mobility transistors
$L_g$: Gate length
$I_{DS}$: Drain-source current
$I_{DS\text{-}sat}$: Drain-source saturation current
$R_c$: Contact resistance
$R_{sh}$: Sheet resistance
$n_s$: 2DEG concentration
$\mu_e$: Electron mobility
2DEG: Two dimensional electron gas
UID-GaN: Unintentional doped-GaN
LPCVD: Low pressure chemical vapor deposition
$V_{GS}$: Gate-source voltage
$V_{TH}$: Threshold voltage
DIBL: Drain induced barrier lowering

# Low Off-State Leakage Current Normally Off p-GaN Gate HEMT Using the $Al_{0.5}Ga_{0.5}N$ Etching Stop Layer Design

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**Keywords: p-GaN gate HEMT, normally off, etching stop layer, and high selection ratio**

## Abstract

**In this work, normally off p-GaN/AlGaN/GaN high-electron-mobility transistors (HEMTs) were developed using $Al_{0.5}Ga_{0.5}N$ etching stop layer. Compared with AlN etching stop layer, the device not only decreased lattice defects but has also improved the linearity in drain current, which can be attributed to lattice matching. The results show that the $Al_{0.5}Ga_{0.5}N$ etching stop layer can reduce surface dislocation and obtain better characteristics. The p-GaN HMET using $Al_{0.5}Ga_{0.5}N$ etching stop layer achieved a higher drain current on/off ratio of $2.47\times10^7$, lower gate leakage current of $1.55\times10^{-5}$ A/mm, and low on-state resistance of 21.65 Ω·mm. The dynamic $R_{ON}$ of $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer device are 1.69 times and 2.26 times.**

## Introduction

Gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) show promising potential for high switching speed and high-power semiconductor device applications owing to their high electric field strength, high mobility, and good thermal stability [1]. Normally off behavior of AlGaN/GaN HEMTs with a sufficiently large and stable $V_{TH}$ is highly desirable due to single voltage supply consideration. Thus, several researches have been proposed to realize the normally off operation characteristics of the AlGaN/GaN HEMTs, such as ultrathin barrier (UTB) [2], gate-recessed structures [3], [4], fluorine treatment [5], [6], and p-type gate. However, the structure with p-type gate has drawn increasing attention in the industry due to its low on-state resistance and large threshold voltage. Since the p-GaN gate etching process is a key factor in device processes, an appropriate etching depth control is strongly required. The residual p-GaN layer beyond the gate area depletes the 2DEG channel and causes a low forward current. Moreover, if the AlGaN barrier layer is etched in this step, the channel carrier density is decreased because of decreasing the spontaneous polarization. The techniques of $Al_{0.5}Ga_{0.5}N$ etching stop layer were researched. In addition to matching the lattice, the lattice defect is still decreased. In this work, an $Al_{0.5}Ga_{0.5}N$ etch stop layer was used between the p-GaN and AlGaN barrier and compared with AlN etching stop layer. Moreover, high-performance normally off p-GaN/AlGaN/GaN HEMTs have been realized.

## Experimental Procedures

In this work, the p-GaN/AlGaN/GaN HEMT was grown on 6-inch Si (111) substrates by MOCVD. Figure 1(a) shows the component structure, in which the active Mg concentration was $1\times10^{18}cm^{-3}$. For device fabrication, the active region was protected by photoresist, and the mesa-isolation region was etched to a depth of 200 nm in a reactive ion etching chamber using $BCl_3/Cl_2$ mixed gas plasma. A 5-μm-long p-type GaN gate finger was formed by etching using the p-GaN/$Al_{0.5}Ga_{0.5}N$ interface design. A mixture of $BCl_3/Cl_2/SF_6$ gas plasma was adopted to remove p-GaN for 120 s to form the gate terminals, with a resulting etching rate of 0.625nm/sec. The $SF_6$ plasma reacted with Al atoms and formed a thin $AlF_3$ etching stop layer when the mixed gas plasma reached the $Al_{0.5}Ga_{0.5}N$ barrier layer. As shown in Fig. 1(b), the p-GaN removal depth was measured using an atomic force microscope. To ensure uniform and complete removal of the p-GaN layer, a 240-s etch was used with 120-s over etching, and an obvious etching stop function was achieved by adopting $Al_{0.5}Ga_{0.5}N$ layer design [7]. Subsequently, the sample was immersed into diluted HF/$NH_4OH$ chemical solution to remove the newly formed $AlF_3$ and $AlO_x$ compounds. Ti/Al/Ni/Au (25/120/25/150nm) ohmic metal stack was then deposited as source and drain by electron beam evaporation (E-gun), and it was annealed at 875°C for 30 s in an $N_2$ atmosphere by RTA system. Third, the device was fabricated with implant isolation by oxygen implantation. Finally, the Ni/Au (25/120nm) gate electrode with the gate length of 2 μm was deposited by electron beam evaporation, and 100 nm of SiN was passivated.

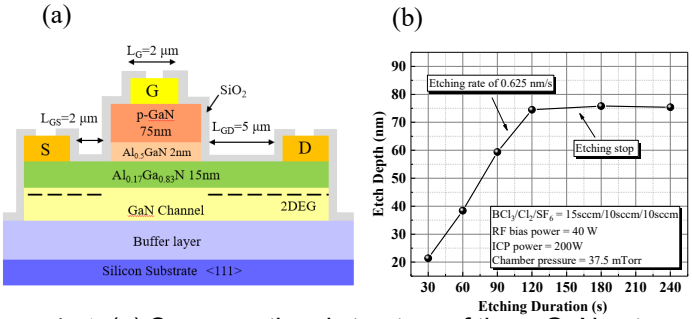


Fig.1. (a) Cross-sectional structure of the p-GaN gate HEMT and (b) p-GaN removal depth as a function of etch duration

## RESULTS AND DISCUSSION

Figure 2 shows the X-ray diffraction (XRD) measurement. The full width at half maximum (FWHM) of the (002) symmetric reflection and the (102) asymmetric reflection was taken as a measure of crystalline quality. In this work, we measured the surface of the device, mainly analyzing the crystal quality of the surface. The (002) rocking curve scan yields information about the extent of tilt with respect to the surface of the device, and its FWHM is a qualitative measure of the screw dislocation density ($N_{screw}$) [8]. The (102) scan yields twist with respect to the surface of the device, and its FWHM is measure of edge dislocation density ($N_{edge}$). After calculation, the total dislocation ($N_{total}$) using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer is $2.23\times10^{8}$ and $3.57\times10^{8}$per $cm^{-2}$, respectively. As shown in Fig. 2, the screw dislocation density and edge dislocation density are lower in case of using $Al_{0.5}Ga_{0.5}N$ etching stop layer.

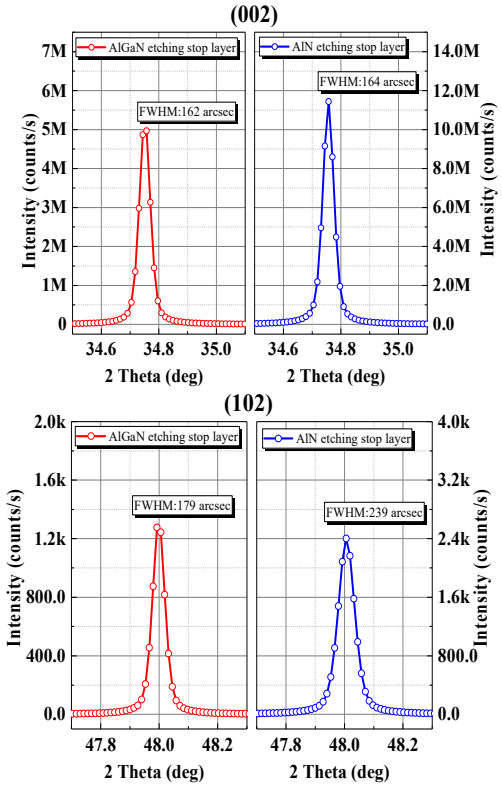


Fig.2. XRD measurement—the full width at half maximum (FWHM) of the (002) symmetric reflection and the (102) asymmetric reflection using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer

Figure 3(a) and (b) shows the log-scale transfer ($I_{DS}$–$V_{GS}$) and output ($I_{DS}$–$V_{DS}$) characteristics using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer. As shown in Fig. 3(a), the off-state current for using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer was $4.11\times10^{-6}$ and $4.31\times10^{-5}$ mA/mm, respectively. This implies that using $Al_{0.5}Ga_{0.5}N$ etching stop layer results in lower trap density in the device channel. By contrast, lower aluminum mole fraction in etching stop layer can decrease the trap density of channel and can cause lattice matching. Additionally, the maximum output current density ($I_{Dmax}$) was 121 and 67 mA/mm at a gate bias of 4V, respectively. The $I_{Dmax}$ value using $Al_{0.5}Ga_{0.5}N$ etching stop layer was 43% higher than that of using AlN etching stop layer due to the suppressed trap density of channel.

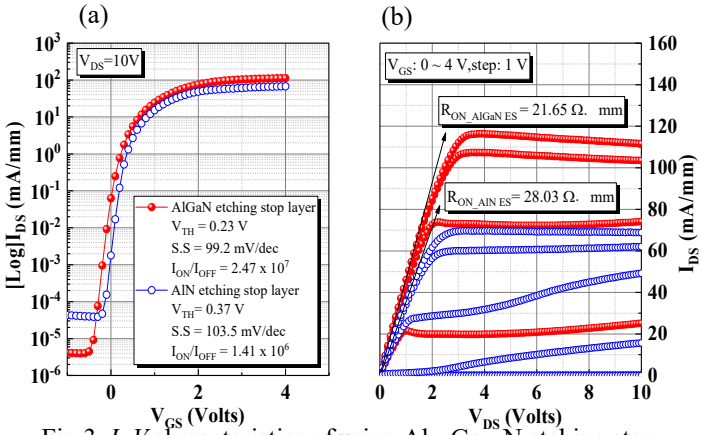


Fig.3. *I–V* characteristics of using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer with $L_{GS}/L_G/L_{GD}/W_G$ = 2/2/5/100 µm, (a) transfer characteristic, and (b) output characteristic

Figure 4(a) shows the gate leakage current $I_{GS}$ of a 2-µm gate device. Clearly, using $Al_{0.5}Ga_{0.5}N$ etching stop layer exhibits better gate leakage than AlN etching stop layer, with a gate leakage improvement from $9.27\times10^{-5}$ to $1.55\times10^{-5}$ at a gate bias of −10V. After calculation, the static on-resistance using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer is 21.65 and 28.03Ω·mm, respectively, corresponding to a specific on-resistance ($R_{sp}$) of 2.59 and 3.36 m Ω·$cm^2$. The off-state breakdown voltage using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer was 561V and 501V at $V_{GS}$ = −1V, and FOM was 83.11 and 44.37MW/$cm^2$, respectively, as shown in Fig4(b).

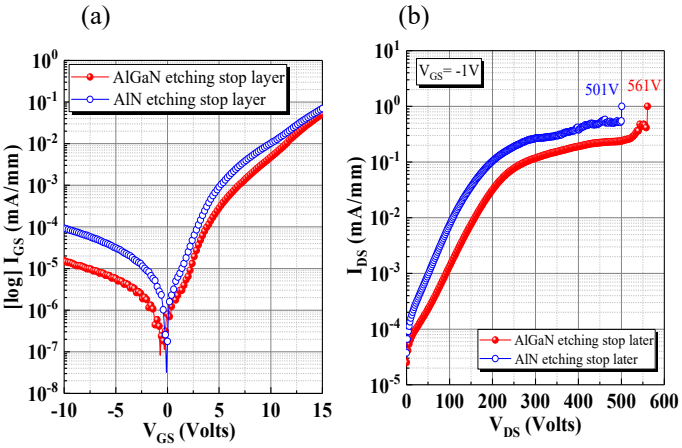


Fig.4. (a) Gate leakage characteristics and (b) off-state breakdown voltage measurement

As shown in Fig. 5, the $I_{DS}$–$V_{DS}$ pulsed characteristic was also measured from different quiescent bias points at $V_{GS}$ = 4 V to investigate the influence of off-state gate bias stress on dynamic $R_{ON}$ and $I_{DS}$. The reference off-state was set as ($V_{GSQ}$, $V_{DSQ}$) = (0 V, 0 V), which does not induce any relevant trapping. The device is switched with 2-µs pulse width and 200-µs period, respectively. The quiescent gate bias ($V_{GSQ}$) was swept from 0 to −3 V. Apparently, the current collapse of the AlN etching stop layer device is worse than that of the $Al_{0.5}Ga_{0.5}N$ etching stop layer device, and the high gate lag of the AlN etching stop layer device under relatively gate voltage stress results in $I$–$V$ slope decreases, indicating that its surface defect trap density is higher than that of the $Al_{0.5}Ga_{0.5}N$ etching stop layer device. The dynamic $R_{ON}$ ($R_{ON}/R_{ON(0,0)}$) of the $Al_{0.5}Ga_{0.5}N$ etching stop layer device slightly increased with higher gate bias stress from 0 to −3 V due to low electron injection into the surface trap states from the gate electrode, and the dynamic $R_{ON}$ ratio increased to 2.26 at the off-state gate bias stress of −3 V for the AlN etching stop layer device.

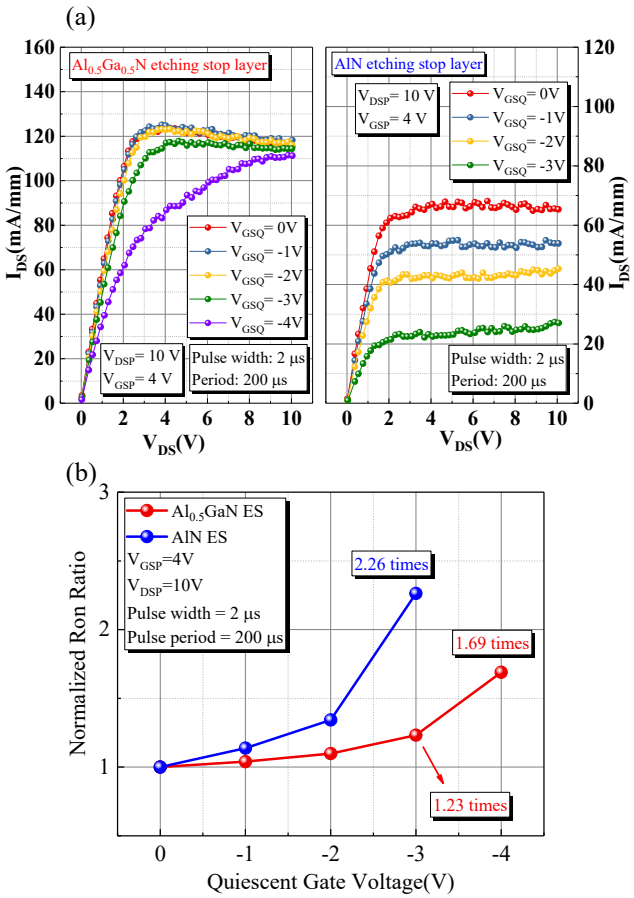


Fig.5. (a) Pulsed $I_{DS}$–$V_{DS}$ characteristics from quiescent gate bias point of 0 V to an on-state at 4 V with 2-µs pulse width and 200-µs pulse period—afterward, the quiescent gate bias ($V_{GSQ}$) was swept from 0 to −3 V and (b)

## CONCLUSIONS

In this work, $Al_{0.5}Ga_{0.5}N$ etching stop layer was applied for p-GaN/AlGaN/GaN HEMT. The dislocation density was clearly proved after XRD measurement. Using $Al_{0.5}Ga_{0.5}N$ etching stop layer exhibited lower dislocation density, lower off-state current, lower gate leakage, lower on-resistance, higher on/off ratio, and higher off-state breakdown voltage. The dynamic $R_{ON}$ of $Al_{0.5}GaN$ etching stop and AlN etching stop device are 1.23 times and 2.26 times at the off-state gate bias stress of −3 V, respectively. Using $Al_{0.5}Ga_{0.5}N$ etching stop layer can match the lattice and improve the ratio of dynamic resistance. Therefore, using $Al_{0.5}Ga_{0.5}N$ etching stop layer is a promising method for fabricating high-performance normally off p-GaN HEMTs.

## REFERENCES


[1] W. Saito et al., "High breakdown voltage AlGaN–GaN power-HEMT design and high current density switching behavior," IEEE Trans. Electron Devices, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.

[2] Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, "Enhancement-mode AlGaN/AlN/GaN high electron mobility transistor with low ON-state resistance and high breakdown voltage," Jpn. J. Appl. Phys., vol. 45, nos. 42–45, Nov. 2006, Art. no. L1168.

[3] T. Oka and T. Nozawa, "AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications," IEEE Electron Device Lett., vol. 29, no. 7, pp. 668–670, Jul. 2008.

[4] K. W. Kim et al., "Effects of TMAH treatment on device performance of normally off $Al_2O_3$/GaN MOSFET," IEEE Electron Device Lett., vol. 32, no. 10, pp. 1376–1378, Oct. 2011.

[5] W. Chen, K. Y. Wong, and K. J. Chen, "Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters," in Proc. IEEE IEDM, Dec. 2008, pp. 1–4.

[6] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "High performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment," IEEE Electron Device Lett., vol. 26, no. 7, pp. 435–437, Jul. 2005.

[7] D. Buttari et al., "Selective dry etching of GaN over AlGaN in BCl3/SF6 mixtures," in Proc. IEEE Lester Eastman Conf. High Perform. Devices, 2004, pp. 132–137.

[8] H. P. Lee, J. Perozek, L. D. Rosario, C. Bayram, "Investigation of AlGaN/GaN high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations," Sci. Rep., Nov. 2016.

# A Study of Wafer-Scale Breakdown Characteristics of Vertical GaN PIN Rectifiers

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## Abstract

**We report the development of vertical GaN PIN rectifier fabrication processing using an ion implantation isolation technique to create floating field guard ring (FGR) structures. With proper engineering in implantation profile and FGR geometries, fabricated devices demonstrated uniform blocking voltage (BV) for 1.2-kV-class devices across a 2-inch free-standing GaN substrate. A material analysis technique that can quickly detect bulk defects in the wafer scale was developed using a confocal photoluminescence under sub-bandgap photon excitation at $\lambda$ = 400 nm. The wafer-mapping capability was used to investigate the correlation between bulk impurities and the BV performance.**

Keywords: High power switches, GaN, photoluminescence, rectifiers, wafer-level characterizations.

## INTRODUCTION

Gallium Nitride (GaN) is a wide-band-gap semiconductor that is widely used in optoelectronics and power electronics. For GaN devices to reach theoretical power switching limits with reliable operation, it is crucial to mitigate field crowding effects [1] [2]. This may be achieved with effective electrical field termination at the edge of the active device region.

In this paper, we report the development of a novel floating field guard ring (FGR) field termination technique for vertical GaN PIN rectifiers. The FGRs were formed by alternating the p-type GaN layer and highly-resistive GaN layer in the lateral extent of the devices. The highly-resistive GaN layer were created by selective-area ion implantation with nitrogen ion species. The nitrogen ion implantation creates controlled number of donor-like nitrogen vacancies and formed a compensated semiconductor in the implanted region. With proper choices of implantation schedule, we achieved effective field termination for vertical GaN PIN rectifiers for 1.2-kV-class applications. The developed processing technique implemented on a 2" free-standing GaN substrated exhibited uniform and reliable breakdown characteristics on the wafer scale.

To understand the impact of as-grown defects in GaN on device performance, a confocal photoluminescence under a sub-bandgap photon excitation at $\lambda$ = 400 nm was used to investigate the correlation between bulk impurities and the BV performance as well as the effect of different floating guard ring (FGR) designs on device performance.

## MATERIAL GROWTH AND DEVICE FABRICATION

GaN p-i-n APD epitaxial structures were grown on a 2-inch free-standing GaN substrate using an AIXTRON 6×2" close-coupled showerhead (CCS) metalorganic chemical vapor deposition (MOCVD) reactor. The epitaxial layers consists of 1000-nm *n*-type GaN:Si layer ([*n*] ~ $7\times10^{18}$ cm$^{-3}$), a 8-µm undoped GaN drift layer ([*n*] ~ $2\times10^{16}$ cm$^{-3}$), and a 450-nm *p*-type GaN:Mg layer ([*p*] ~ $2\times10^{18}$ cm$^{-3}$).

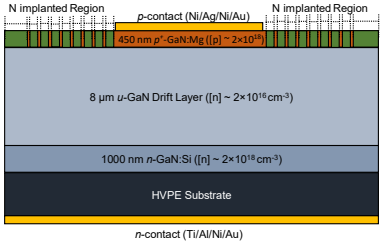


Figure 1. A schematic cross-section drawing of a vertical GaN *p-i-n* rectifier with nitrogen-implanted isolation and FGR design. Nitrogen implanted area is the green-colored region.

In this study, FGRs were designed specifically for a blocking voltage of 1.2 kV. These designs were performed in a TCAD Sentaurus™ simulation package and were reported earlier in [3]. Proper choices of the nitrogen ion-implantation energy and doses were chosen following the design strategies as reported in [4] to achieve effective device isolation and for the FGR formation. A schematic cross-sectional view of the vertical GaN PIN rectifiers with the FGRs is shown in Figure 1. Figure 2(a) shows a typical FGR design that effectively mitigate the electric field distribution by extending the depletion regions throughout the FGR. By properly choosing the gaps of the p-GaN guard rings, (e.g., < 2 µm for 1.2 kV of BV), Figure 2(b) shows uniform potential gradient along the FGR. As a result, the field crowding effect and premature surface breakdown can be effectively mitigated.

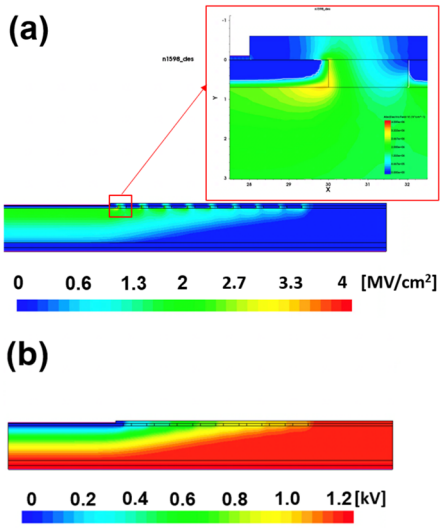


Figure 2. TCAD simulation of the vertical GaN p-i-n rectifier with 8 FGRs (FGR gap=2µm, width=4µm) at reverse bias -1200V: (a) Electric field distribution, (b) Potential distribution.

The device fabrication processing started with a backside *n*-type metallization with Ti/Al/Ni/Au stack followed by a nitrogen ion implantation for device isolations A three-step ion implantation schedule was implemented with energies of 45 keV, 140 keV, and 290 keV, respectively, to achieve flat implantation profile and to form an "isolation" layer by compensating the Mg dopants in the *p*-GaN and for the formation of FGRs. After the ion implantation, the *p*-contact was formed by Ni/Ag/Ni/Au metal stacks and the devices are passivated with $SiO_2$. A picture of completed vertical GaN *p-i-n* rectifiers on a 2-inch HVPE substrate is shown in Figure 3.

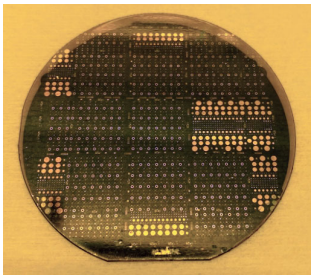

Figure 3. Fabricated vertical GaN p-i-n rectifiers grown on a 2" free-standing GaN substrate.

## Device Performance Discussions

Figure 4 shows the forward bias characteristics of the devices. The ideality factor was 2.1, and the turn-on voltages were ~4.3 V at 100 A/cm$^2$. Typical specific-on resistance ($R_{on}A$) was 1.31 mΩ·cm$^2$ at 1.1 kA/cm$^2$. The $R_{on}A$ could be further reduced by driving the device to higher current density, as shown in the graph. Figure 5 shows a cumulated reverse-biased I-V curves of 120 randomly selected devices measured across the 2-inch wafer. Among these devices under tests (DUTs), 112 devices exhibited BV of greater than 1.1 kV. The devices that showed low BV < 1.1 kV were subject to further study. The majority of the low BV devices (6 devices) have apparent surface textures near or on the devices area. Some devices were intentionally fabricated on "dot-core" sites on the wafer (not shown in Figure 2), which resulted in premature breakdown less than 200 V. There were also 2 devices that we could not find reasons with visible indications for low BVs and will be subject to further investigation.

Figure 6 shows the correlation of the BV as a function of the device's diameters. Devices of the same diameters but with different number of FGRs were also populated in the plot. Except for devices sitting on the "dot core" site, the BV of the devices were around 1.2 kV regardless of the device diameters. This result may imply high-quality epitaxial layer growth and effective ion-implantation isolation technique was achieved in this work. In such device design, a buried junction structure that suppresses premature breakdown mechanism such as surface breakdown or field crowding effects. As a result, the breakdown voltage is predominantly dictated by the bulk material properties. It is concluded that the uniform device performance can be attributed to high-quality substrate, optimized epitaxial growth, and robust device fabrication on a wafer-level scale.

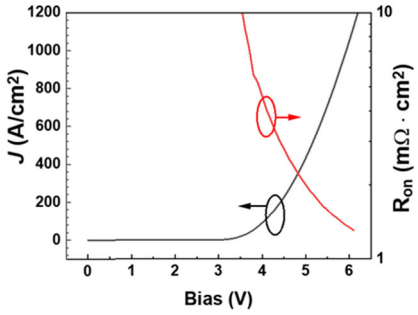


Figure 4. A forward I-V curve in linear scale with specific-on resistance ($R_{on}A$).

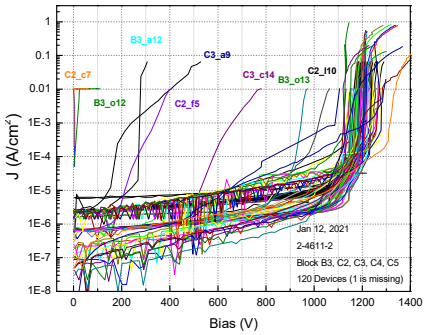


Figure 5. Reverse I-V characteristics of vertical GaN p-i-n rectifiers of randomly chosen 120 devices across a 2-inch wafer. The IDs of the devices with BV < 1.1 kV are marked in the plot.

A confocal PL intensity imaging system was used to scan the 2-inch round GaN device sample. PL intensity associated with each device was compared to the device performance to understand how the bulk defects impact on the device leakage current, BV, and reliability. Surface defect-induced premature BV can be easily ruled out with an optical microscope as shown in Figure 7. Other defect-related early BV will be investigated further with the confocal PL. In the current PL system, a pulsed laser with 400 nm excitation wavelength is used, and broad band PL signals with wavelengths greater than 450 nm are collected. The PL signals are sensitive to point defects and their related defect complexes as they serve as radiative recombination centers. A higher PL intensity indicates a locally higher impurity level.

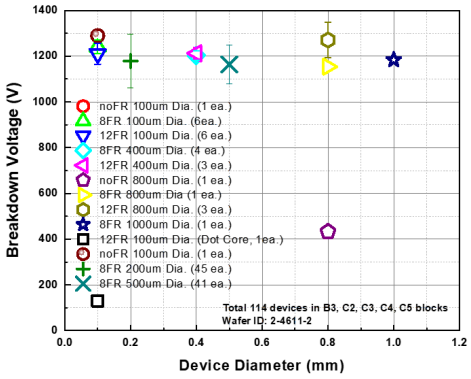


Figure 6. Breakdown voltage versus device diameters from 100 µm to 1 mm with different FGR designs.

Figure 8 shows PL intensity comparison of a 2-inch free-standing GaN substrate before and after *p-i-n* epilayer growth. The identical feature of periodical high PL intensity regions suggests that the impurities originate from the substrate, instead of epi-growth process. The HVPE substrate was presented with periodically positioned domains "cores" to concentrate the dislocations below the cores and reduce dislocation density elsewhere. During the epitaxial lateral over-growth, the impurities (e.g., oxygen) are incorporated to the semipolar planes and the process ends up with a higher impurity level at the coalescence region (dark red in PL map).

The HVPE substrate used in the study exhibited arrays of dot cores throughout the wafer with a 1-mm pitch. An interest of study may arise regarding the device performance variation relative to the presence of these cores. Figure 9 shows a study of the BV versus the distance of a 100-µm-dia. device to the nearest dot core sites. While most of the devices have BV greater than 1 kV, the devices fabricated on dot cores had BV less than 200 V. The results seemed to indicate that the areas outside of the dot cores could reliably yield high-performance electronics, while any devices ran across the core sites would result in premature breakdown features. For devices fabricated on the HVPE substrate, the BV is limited by dislocation density given that an optimized device design which prevents premature failure. The lowest PL signals were found in dot-core area. A threading dislocation can be modeled as a negatively charge cylinder which repels adjacent electrons to form a depletion region. The generated e-h-pairs are quickly separated, and no carrier recombination is represented in its vicinity [5-8]. However, the devices with distances to the dot cores greater than 200 µm did not show clear dot-core-dependent BV characteristics. This might be due to the reduced dislocation density in these regions [9].

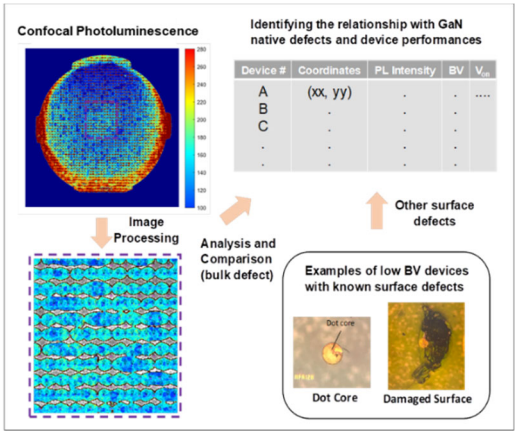


Figure 7. Schematic diagram of the material analysis and device characterization to identify the correlation between devices performance and defects. Surface defects can be easily identified with an optical microscope. Bulk defects could be identified with time-resolved confocal photoluminescence and image processing.

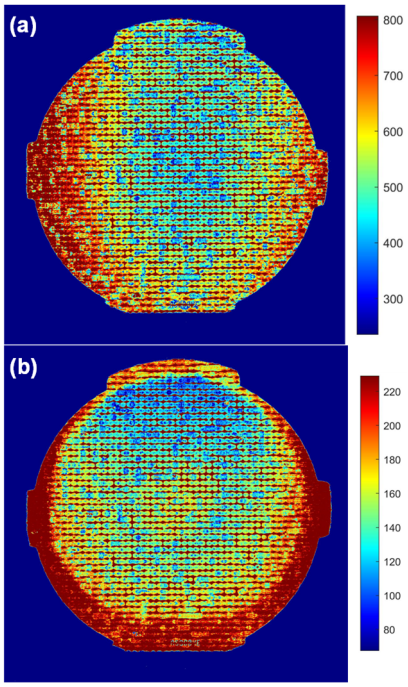


Figure 8. Confocal PL intensity maps (400 nm excitation) of a 2-inch GaN wafer (a) prior to epilayer growth and (b) post epilayer growth.

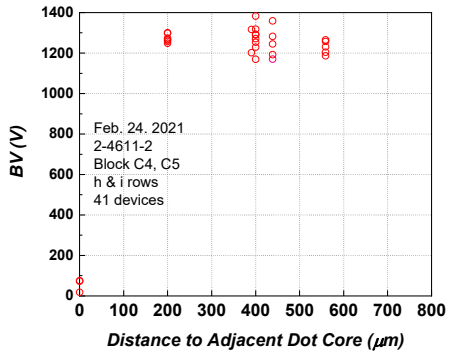


Figure 9. BV vs the distance to adjacent dot cores of 41 devices with 100 μm diameter.

The correlation between PL intensity and device BV was investigated related to data in Figure 9. However, there is no clear relationship discovered between impurity levels and the device breakdown voltage in this study. The impurity related defects are typically associated with device degradation. To understand the impact, high-temperature reverse bias (HTRB) and high-temperature operating life (HTOL) tests will be performed on selected devices in high PL and low PL intensity regions in future study.

## CONCLUSIONS

Vertical GaN p-i-n rectifiers were fabricated on a 2-inch HVPE substrate. Proper ion implantation conditions using nitrogen ions were chosen to provide effective device isolation and novel ion-implantation enabled FGR designs. The TCAD device simulation was performed to optimize such FGR design and the device performance was experimentally validated. The fabricated devices demonstrated uniform and reliable operations of 1.2-kV BV that facilitate further study of device failure mechanisms related to the wafering and epitaxial material quality. A confocal PL was used to investigate the origin of premature BV devices associated with bulk defects. The result showed that the devices fabricated on dot core sites had significantly low BV. The location of dot core could also be identified with low PL signals. However, the devices with a distance to the adjacent dot cores are not impacted by high dislocation density concentrated in the dot cores. Further studies on bulk defects in the substrate, and its impact on long-term device reliabilities will be studied in the future.

## ACKNOWLEDGEMENT

This work was supported by the U.S. Department of Energy (DOE), Office of Energy Efficiency and Renewable Energy (EERE), Advanced Manufacturing Office (AMO) and performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract No. DE-AC52-07NA27344, LLNL-ABS-820651.

## REFERENCES

[1] H. Ohta, N. Asai, F. Horikiri, Y. Narita, T. Yoshida, and T. Mishima, "4.9 kV breakdown voltage vertical GaN p–n junction diodes with high avalanche capability," *Japanese Journal of Applied Physics,* vol. 58, no. SC, p. SCCD03, 2019.

[2] J. Wang *et al.*, "High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination," vol. 113, no. 2, p. 023502, 2018.

[3] M. Cho, Z. Xu, M. Bakhtiary-Noodeh, T. Detchphrom, R. D. Dupuis, and S.-C. Shen, "Design of Ion-Implanted Junction Termination Extension for Vertical GaN Pin Rectifiers," *ECS Transactions,* vol. 98, no. 6, pp. 49-59, 2020.

[4] C. Tsou, M. Ji, M. Bakhtiary-Noodeh, T. Detchprohm, R. D. Dupuis, and S. Shen, "Temperature-Dependent Leakage Current Characteristics of Homojunction GaN p-i-n Rectifiers Using Ion-Implantation Isolation," *IEEE Transactions on Electron Devices,* vol. 66, no. 10, pp. 4273-4278, 2019.

[5] E. Baghani and S. K. O'Leary, "Dislocation line charge screening within n-type gallium nitride," vol. 113, no. 2, p. 023709, 2013.

[6] D. Cherns and C. G. Jiao, "Electron Holography Studies of the Charge on Dislocations in GaN," *Physical Review Letters,* vol. 87, no. 20, p. 205504, 2001.

[7] N. G. Weimann, L. F. Eastman, D. Doppalapudi, H. M. Ng, and T. D. Moustakas, "Scattering of electrons at threading dislocations in GaN," vol. 83, no. 7, pp. 3656-3659, 1998.

[8] E. Müller, D. Gerthsen, P. Brückner, F. Scholz, T. Gruber, and A. Waag, "Probing the electrostatic potential of charged dislocations in n-GaN and n-ZnO epilayers by transmission electron holography," *Physical Review B,* vol. 73, no. 24, p. 245316, 2006.

[9] K. Motoki, "Development of Gallium Nitride Substrates," 2010.

## ACRONYMS

MOCVD: Metalorganic chemical vapor deposition
BV: blocking voltage
PL: photoluminescence
FGR: floating guard ring
HVPE: hydride vapor phase epitaxy
HTRB: high temperature reverse bias
HTOL: high temperature operating life

# Using the CnCV Technique to Explore AlN as an Alternative Passivation Layer in GaN HEMT Technology

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**Keywords: AlN, ALD, GaN, HEMT, non-contact CV, corona**

**Abstract**

**AlN has shown potential promise as an alternative passivation dielectric to the standard $Al_2O_3$ in GaN HEMT structures. In this work we investigate thermal ALD AlN as an alternative for $Al_2O_3$ passivation of the AlGaN surface in a HEMT structure. However the replacement of a passivation dielectric in a device requires careful investigation and can be a costly and time consuming process. Therefore, the low cost, quick feedback corona non-contact CV (CnCV) technique has been employed in this investigation in order to efficiently study thermal ALD AlN passivation in a non-contact, preparation-free manner. The CnCV technique was used to assess key HEMT structure parameters such as pinch-off voltage (Vp) and 2DEG sheet charge ($Q_{2DEG}$) on a thickness skew of thermal ALD AlN and reference process $Al_2O_3$ passivated HEMT structures. This allowed efficient determination of the AlN thickness necessary for matching of the $Q_{2DEG}$ to the $Al_2O_3$ reference process. Dielectric thickness non-uniformity of the AlN was also assessed directly on the AlGaN HEMT structure using CnCV measured SASS voltage (not possible using standard ellipsometry). Reduction of $D_{it}$ at the AlGaN interface for the thermal ALD AlN compared to $Al_2O_3$ was also demonstrated by photo-assisted CnCV results with confirmation from dynamic Rds(on) measurements on final device structures. This work demonstrates the distinct advantages the CnCV technique and the results show the promise of thermal ALD AlN as an alternative passivation dielectric for AlGaN.**

## INTRODUCTION

In this work the corona non-contact CV (CnCV) technique has been utilized to assess thermal aluminum nitride (AlN) as a potentially advantageous alternative to the mainstream $Al_2O_3$ passivation layer commonly used in GaN HEMT technology. Plasma-enhanced ALD AlN has been previously reported to reduce $D_{it}$ at the interface between ALD passivation and AlGaN in HEMT structures, with positive impact on GaN device stability [1]. Less is known about thermal ALD AlN in GaN devices. Compared with PE-ALD, thermal ALD has several advantages such as batch processing, a simpler and more mature toolset and no potential plasma damage to passivated surface [2].

Replacing a material, such as a passivation dielectric, in a device requires significant process flow modifications and re-development of individual process steps. This can be a very costly and time-consuming process. Therefore a low cost, quick feedback metrology technique to carefully investigate new materials can be very advantageous. In this respect the CnCV technique can be of great benefit. CnCV offers non-destructive, preparation-free wafer level measurement. Since 2018 it is available in tools designed specifically for wide-bandgap semiconductor technology. CnCV tools have been already extensively applied for characterization of SiC, GaN and AlGaN/GaN HEMT [3,4].

The non-contact electrical measurements in CnCV are based on precise dosing of charge, $\Delta Q_C$, on the surface, performed with a corona discharge in air. The charging serves as a bias and the response is monitored as a change of the surface voltage, $\Delta V$, measured with a non-contact Kelvin probe.

## EXPERIMENTAL RESULTS AND DISCUSSION

The key parameters extracted from CnCV measurements is this study include pinch-off voltage ($V_P$), 2DEG sheet charge ($Q_{2DEG}$) and positive SASS voltage (the dielectric tunneling voltage under positive corona bias). For ALD dielectrics the SASS voltage typically scales with ALD cycles, providing a measure of the deposition process and film thickness.

A skew of thermal ALD AlN samples with varying ALD cycles was deposited on standard normally-on AlGaN/GaN HEMT structures on Si substrates. Reference process samples included thermal ALD $Al_2O_3$ coated and bare AlGaN/GaN HEMT structures.

Figs 1 and 2 show the capacitance-voltage, CV, and capacitance-charge, CQ, characteristics measured on thermal ALD AlN samples along with with the reference $Al_2O_3$ and bare HEMT samples. CV is used for the determination of $V_P$ and 2DEG sheet charge. The latter is obtained by integration of the capacitance similar to the conventional contact CV technique. The unique CnCV C-Q characteristics allow the novel direct determination of the 2DEG sheet charge as the amount of deposited charge from the initial state condition (0 charge in Fig. 2) to the pinch off condition, Vp. The measured sheet charge values, $Q_{2DEG}$, are presented in Fig 3. They are normalized to the $Al_2O_3$ value, treated as the reference. Good agreement between the two independent determinations of $Q_{2DEG}$ is evident. With the information in Fig. 3, one can quickly target what number of AlN ALD cycles that will give the closest 2DEG sheet charge to the reference $Al_2O_3$ process. In the present skew, the 50 cycle AlN sample has a 1.2x higher

$Q_{2DEG}$ than the reference $Al_2O_3$ sample. This type of process targeting for a new material is made cost and time effective with the CnCV technique.

The CnCV SASS voltage measurements were used to gain quick, direct insight into thermal ALD AlN growth on AlGaN. The ΔSASS voltage values in Fig. 4 are after subtraction of SASS voltages measured on a bare AlGaN HEMT structure without an ALD layer. Therefore the ΔSASS values reflect the growth of thermal ALD AlN films on AlGaN as a function of ALD cycles. At 50 cycles and above the dependence becomes linear. However values deviating from the linear dependence below 50 cycles may be an indication of an incubation effect analogous to that in thermal ALD AlN growth on Si that occurs for the first 50 cycles [5]. The SASS voltage was also used to assess the within wafer thickness variation of passivation films on HEMT structures. This application is especially important considering that ellipsometry measurements of AlN thickness on complex AlGaN/GaN structures are difficult and require extensive modelling. The across wafer diameter line scans of the SASS voltage are shown in Fig. 5 for the AlN skew and the reference $Al_2O_3$ sample. Larger within wafer non-uniformity is evident for some of the AlN samples when compared to the ref. $Al_2O_3$.

Pulsed Ids(Vds) curves measured shortly after off-state quiescent biases on final device transistors in Fig. 6 show a reduction in dynamic Rds(on) for the 50 cycles thermal AlN compared to the reference $Al_2O_3$. This is ascribed to lower $D_{it}$ levels at the AlGaN interface which is corroborated by photo-assisted CnCV measurements showing a lower deep interface state concentration for the thermal ALD AlN passivated samples compared to the reference $Al_2O_3$.

## REFERENCES


[1] Sen Huang et al, IEEE Electron Device Letters, 33(4), 516-518 - April 2012.

[2] Zhao, Sheng-Xun, et al., Nanoscale research letters 11.1 (2016), pp.1-5.

[3] M. Wilson, A. Findlay, A. Savtchouk, J. D'Amico, R. Hillard, F. Horikiri and J. Lagowski, ECS J. Solid State Sci. Technol., Vol. 6, issue 11 (2017), S3129-S3140.

[4] M. Wilson, Compound Semiconductor, 25-6 (2019), pp. 20-26.

[5] Van Bui, H., et. al., J. Vac. Sci. Technol. A, Vol. 33, No. 1, (2015).


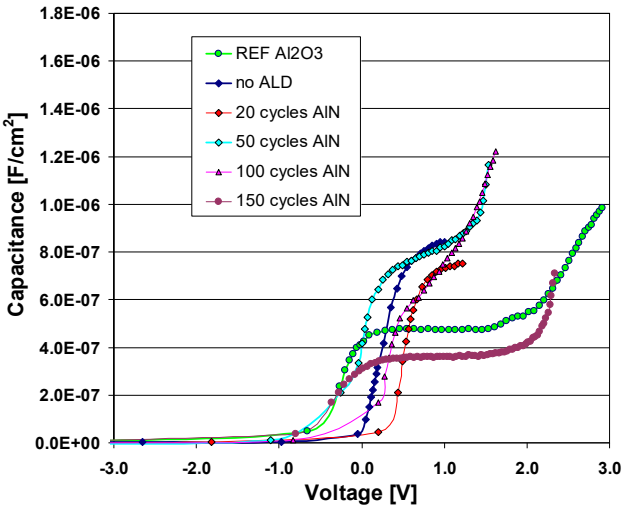


Figure 1. CV characteristics for the skew of thermal ALD AlN samples along with the reference ALD $Al_2O_3$ and bare HEMT samples.

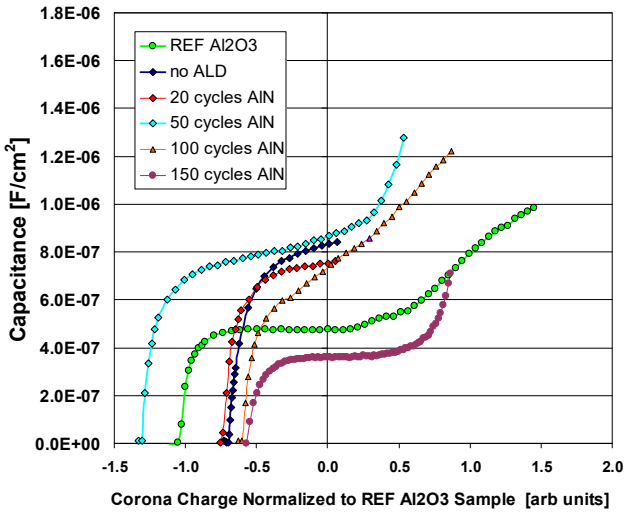


Figure 2. CQ characteristics for the skew of thermal ALD AlN samples along with the reference ALD $Al_2O_3$ and bare HEMT samples. Corona charge on x-axis has been normalized to the reference $Al_2O_3$ sample.

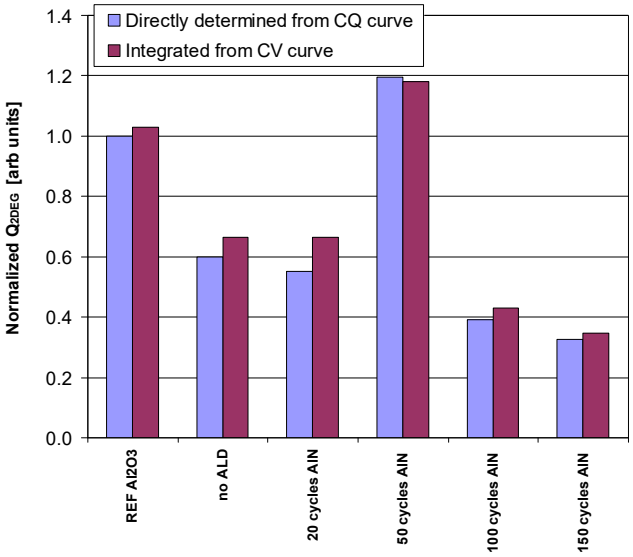


Figure 3. 2DEG sheet charge ($Q_{2DEG}$) comparison of thermal ALD AlN skew to the reference thermal ALD $Al_2O_3$ layer. The $Q_{2DEG}$ values are normalized to the ref. $Al_2O_3$ sample. The 50 cycle AlN sample has 1.2x larger $Q_{2DEG}$ than the ref. $Al_2O_3$.

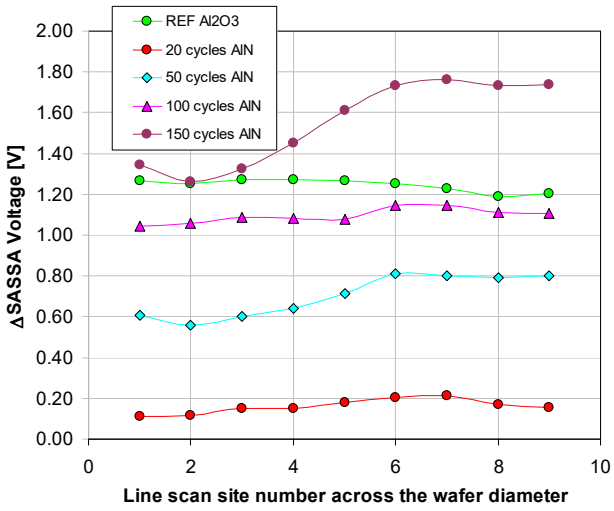


Figure 5. A line scan across the wafer diameter of the ΔSASS voltage (indicator of physical thickness) for the thermal ALD AlN skew and ref. $Al_2O_3$ passivated HEMT structures. Larger within wafer non-uniformity was observed for the some of the AlN samples than the ref $Al_2O_3$.

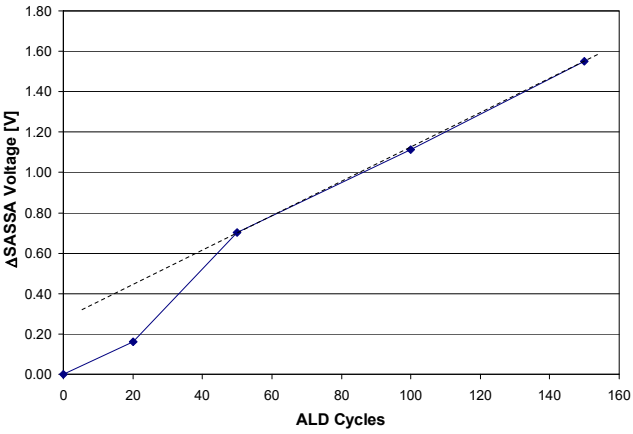


Figure 4. ΔSASS voltage (measure of physical thickness) versus thermal ALD growth cycles for AlN on AlGaN indicates incubation effect for cycles below 50.

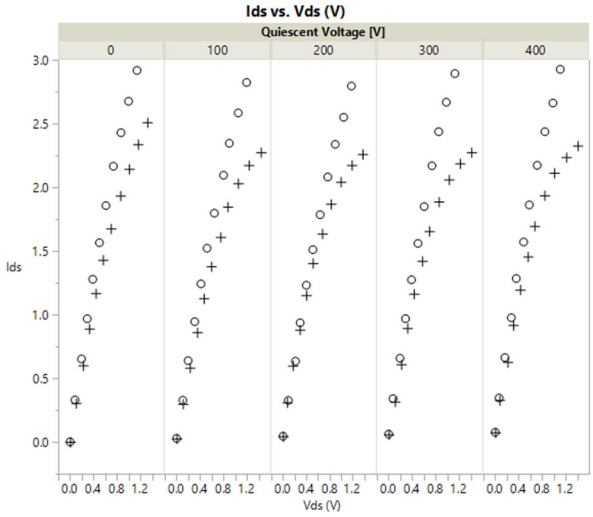


Figure 6. Current-Voltage (Ids vs Vds) results from pulsed IV on final device transistors show improvement in passivation evidenced by the reduction in dynamic Rds(on) for the 50cycle thermal ALD AlN sample (open circles) compared to the ref $Al_2O_3$ sample (crosses).

# SESSION 9:
# DEVICES 2: FILTERS AND PHOTONICS

# 5G SMARTPHONE AND TELECOM INFRASTRUCTURE ARE EMPOWERED BY COMPOUND SEMICONDUCTOR

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**Keywords: wireless infrastructure, compound semiconductors, RFFE, 5G, GaN, GaAs, SiC, Covid-19**

**Abstract**

**The paper presents the market overview of different compound semiconductor such as GaN, GaAs, and SiC impacted by the deployment of 5G in wireless infrastructure and in the new generation of handset applications. The Covid-19 impact and trade war issue are discussed, as well as technology and market trends and Yole's forecast for the coming years.**

## INTRODUCTION

5G plays the main driver for both the markets of radio frequency front end (RFFE) applications and telecom infrastructure to grow. By using compound semiconductor, including GaAs, GaN and SiC, more mature supply chain empowers new applications based on the 5G's advantages of faster data rates and reduced network latency.

## 5G'S IMPACT ON FRONT-END AND CONNECTIVITY

As 5G has started, China, South Korea and USA are early adopter countries of 5G where all major carriers have launched their network. In Japan, in Europe and for the rest of the world, 5G network rollout is moving forward at a slower pace. The Chinese market will pull most of the demand for 5G smartphones in 2020. Whereas the US government is putting a strong emphasis on 5G and Wi-Fi 6 with unprecedented spectrum action plans to accelerate the technology adoption at a broader scale.

RF content and complexity is increased with the introduction of 5G and WiFi6, a 5G handset will feature a 4x4 Multiple Input Multiple Output (MIMO) downlink for frequencies above 2.5GHz. Also, WiFi 6E will extend the frequency coverage of Wi-Fi signals to 6 GHz, where SiGe performance is limited and GaAs adoption is favorable. And in return it will result in a greater penetration of GaAs power amplifiers (PAs) for the high-end sub-6GHz phones.

Overall, the RF-front-end and connectivity market was valued at $15.2B in 2019, and will grow with 11% Compound Annual Growth rate (CAGR) between 2020 and 2025 to reach $25.4B by 2025, as shown in Fig.1. GaAs is the main building block for 3G and 4G handset PAs. With the transition to 5G, it will continue its significant deployment in sub-6GHz phones, as the GaAs PA meets the stringent requirements for power and linearity in the RFFE handset module. In the automotive market, connected vehicles and V2X (Vehicle-to-Everything) will become standard features by 2022, increasing the RF GaAs market in the mid-long term.

## GAN BASED WIRELESS INFRASTRUCTURE MARKET

Over recent years, GaN has been significantly adopted by the RF industry owing to its higher power output at high frequencies, and its smaller footprint. In the dynamic 5G infrastructure market, deployment of higher frequencies in the sub-6GHz as well as in the mm-wave regimes has pushed manufacturers to look for more efficient antenna technology platforms.

Worldwide investment in telecom infrastructure has remained stable in the past decade, with a recent increase coming from Chinese government efforts. The trend toward higher frequencies offers a sweet spot for RF GaN in PA in 5G network at frequencies below 6GHz, in remote radio head (RRH). This application is expected to drive GaN market growth in the next five years. Even though the next generation active antenna systems (AAS) could offer an advantage to silicon LDMOS technology, due to technical limitations such

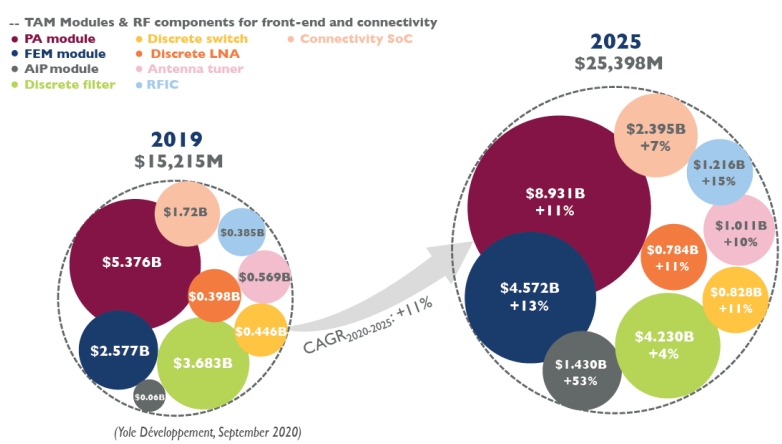


Fig. 1. RF front-end connectivity market forecast 2019-2025

as thermal management and the localized need for such antennas in mostly high-density areas, RRHs will not be replaced and will stay for the long term, using GaN PAs.

In fact, since the apparition of first commercial products 20 years ago, GaN has become a serious rival to silicon Laterally Diffused Metal Oxide Semiconductor (LDMOS) and GaAs in RF Power applications, with a continuous improvement of performance and reliability at lower cost. The first GaN-on-Silicon Carbide (SiC) and GaN-on-Si devices appeared at almost at the same time, but GaN-on-SiC has become more technologically mature. Currently dominating the GaN RF market, GaN-on-SiC penetrated the fourth 4G Long-Term Evolution (LTE) Wireless infrastructure market and is expected to be deployed in RRH architectures in 5G's sub-6Hz implementations. Nevertheless, in parallel, there has also been remarkable progress in cost-efficient LDMOS technology, which is likely to challenge GaN solutions in 5G sub-6Ghz AAS and massive MIMO deployments. In this context, GaN-on-Si stands as a potential challenger with possible expansion to production on 8-inch wafers and promises cost-efficient solutions for commercial markets. Even though, as of 2019, GaN-on-Si remains in small volume manufacturing, it is expected to challenge the existing LDMOS solutions in the Base Transceiver Station (BTS) and RF energy market. Another target of GaN-on-Si companies is the high-volume consumer 5G handset PA market, it could have opportunity to coexist with GaN-on-SiC.

As shown in Fig. 2, the GaN RF device is valued at $740M in 2019, and it will reach beyond $2B by 2025, driven by two main applications: telecom infrastructure and defense.

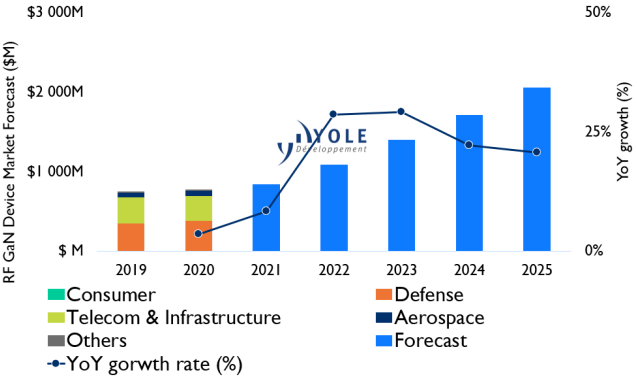


Fig. 2. GaN RF device market forecast

## COVID-19 AND TRADE WAR IMPACTS

Two major global incidents shake the global economy in 2020, the Covid-19 and the tension between the US and China. While Chinese 5G deployment remained unchanged following the pandemic, the European and US 5G deployments had slight delays in H1-20. Starting H2-20, we witnessed an acceleration of 5G network build-out and GaN-based design wins. The situation is expected to come back to normal slowly by the end of H2-20.

In consumer segmentation, the handset production decreased in H1-2020 compared to the same period in 2019. The lockdown in China created disruption in the supply chain, but the strong penetration of 5G and WiFi6 kept driving the strong growth of GaAs PA market.

Since 2018, the GaN RF telecom infrastructure market has been severely impacted by the trade conflicts. The Chinese market led by Huawei represents a large market for 5G GaN wireless infrastructure. US-based device manufacturers had to stop shipping GaN PAs to Huawei in 2019. The US has banned all semiconductor manufacturers from selling to Huawei if their products contain US technology. Since a large majority of semi-insulating SiC substrates are supplied by American wafer manufacturers, the Chinese OEM is again facing a risk of short-supply in the short term.

GaAs RF has a well-established supply chain with many global players, therefore it's less impacted. Key players in the supply chain recently expanded capacity to meet the demands.

## CONCLUSIONS

Despite the disruption of Covid-19 and trade war issue in 2020, 5G is still the main motivation to drive the growth of the compound semiconductor, from the perspectives of supply chain, technology development and end system adaption. GaN is expected to take more market share in telecom infrastructure for the following years and GaAs will continue empowering the adoption of 5G and wifi6 connectivity in the new generation of phones in 2021 and probably the years to come.

## REFERENCES


[1] Yole's - Compound Semiconductor Monitor Service Q4-2020: Module I: Power SiC and Power GaN

[2] Yole Report: GaN RF MARKET: APPLICATIONS, PLAYERS, TECHNOLOGY, AND SUBSTRATES 2020

[3] Yole Report: GaAs WAFER AND EPIWAFER MARKET: RF, PHOTONICS, LED, DISPLAY AND PV APPLICATIONS 2020

[4] Yole Report: 5G's Impact on RF Front-End and Connectivity for Cellphones 2020


## ACRONYMS

RFFE: Radio-Frequency front-end
MIMO: Multiple Input, Multiple Output
PA: power amplifiers
CAGR: Compound Annual Growth Rate
V2X (Vehicle-to-Everything)
RRH: remote radio head
AAS: active antenna systems
LDMOS: Laterally Diffused Metal Oxide Semiconductor
BTS: Base Transceiver Station
LTE: Long-Term Evolution

# State-of-the-Art Etch and Deposition Processing of highly doped ScAlN for 5G and Wi-Fi Filter Applications

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**Keywords: BAW Filter, FBAR, Resonator, 5G, Piezoelectric Aluminium Scandium Nitride, PVD, Plasma Etch**

**Abstract**

**The performance advantages of 5G over previous generations of mobile networks are huge, even in the early phase of 5G rollout. As 5G evolves, so too does Wi-Fi technology, which will continue to offer the best option for short range home/office communications. Bulk Acoustic Wave (BAW) filters have been used for many years for the highest frequency bands for 4G LTE, and will continue to be used for 5G and Wi-Fi. The latest 5G and Wi-Fi bands operate at significantly higher frequency than previous generations, and with a much larger bandwidth. For the filter manufacturer the higher frequency and increased bandwidth means thinner filters with much higher piezoelectric coupling. These requirements pose a significant challenge to the PVD and plasma etch equipment supplier. Here we discuss advances in PVD and plasma etch techniques used to manufacture the latest generation of BAW filters.**

## INTRODUCTION

SAW (surface acoustic wave) and BAW filters have been used in mobile communications for some 20 years. SAW filters, being relatively low complexity and hence low cost, are used wherever possible. BAW filters, which are inherently more complex and more costly, are only used when SAW devices cannot meet the technical demands required for the particular application. In general this means SAW filters are used at lower frequencies and BAW filters at higher frequencies, with the demarcation around 1.5GHz [1].

The piezoelectric element of the resonator at the heart of the BAW filter has been manufactured from Aluminium Nitride (AlN) for many years. AlN is an attractive material for device manufacturers due to its CMOS compatibility, low temperature coefficient of frequency and relative ease of deposition and etching. Whereas the acoustic wave in a SAW filter travels transversely along the device, the acoustic wave in a BAW filter travels through the bulk of the layer, ie through its thickness. The resonator layer thickness must be equal to half the wavelength of the signal at the desired filter frequency, so higher frequency filters need thinner layers of piezoelectric material.

The piezoelectric response, often referred to by the electro-mechanical coupling coefficient, $K^2$, of AlN is low compared to some other piezoelectric and ferroelectric materials. It is high enough, however, for conventional BAW filters with centre frequency in the range 1.5 – 2.5GHz, where the piezo layer thickness is of the order of 1µm. As radio bands with higher frequencies and wider bandwidths are required, materials with higher piezoelectric coupling are needed. AlN doped with other metals has been of particular interest, with work carried out to investigate the suitability of Al(Mg, Hf)N, Al(Mg, Zr)N [2], CrAlN [3], and YAlN [4], although most attention has been paid to ScAlN. It has been shown that ScAlN films with up to 43at% Sc may have ~400% higher piezoelectric coupling coefficient than AlN [5].

The introduction of new higher frequency radio bands, with unprecedented bandwidths of several hundred MHz, for 5G, and even higher frequency bands for Wi-Fi, presents a considerable challenge for the filter manufacturer. Filters for radio bands in the range of 5-6GHz must contain piezo layers that are substantially thinner than previous generations. The huge demand for bandwidth means coupling coefficients must be significantly higher also. ScAlN with Sc content up to 30at% will be used for these applications, and the deposition and etching of these materials presents significant problems.

## ScAlN DEPOSITION

There are several measurable qualities of a deposited ScAlN film that have a definite impact on its piezoelectric performance.

Within wafer (WIW) and wafer to wafer (WTW) stress variation is the most critical aspect of ScAlN deposition, because they are directly related to coupling. It has long been recognised that coupling is the most critical quality of the piezo layer [6]. With radio bands going to higher frequencies with greater bandwidths the requirement for greater coupling is even stronger. The stress state of ScAlN has a direct impact on the coupling. Tensile layers have a higher coupling coefficient than compressive layers, and the sensitivity of the coupling coefficient to the stress increases with Sc content. A piezo layer deposited with a certain mean stress will have a degree of stress variation across the wafer, the WIW stress, and a degree of mean stress variation between wafers, the WTW stress. The WIW and WTW stress define the range of coupling across all the filter devices, and so have the major influence on the device yield.

Thickness non-uniformity of the deposited layer is critical because the layer thickness defines the resonator frequency.

A wide thickness variation results in a wide range of resonator centre frequency, which will impact device yield. The difference between thickness non-uniformity and stress is the device manufacturer can trim the devices to unify the resonator frequency, although trimming is an expensive process that should be kept to a minimum.

Crystal defects or misoriented grains are ScAlN grains that do not grow with the desired c-axis orientation. Since they are not aligned with the bulk of the film they do not add to the piezoelectric coupling, and are effectively dead space. These defects tend to form more readily as Sc content increases. If they are not controlled they can have a major impact on device yield.

## INVESTIGATION

ScAlN films have been deposited by Pulsed DC Magnetron Reactive Sputtering from single ScAl alloy sputter targets with $Ar/N_2$ gas, using SPTS Sigma® PVD module. The DC magnetron utilises a high ion density towards the target mid-radius to give the best possible deposition thickness uniformity (Fig. 1).

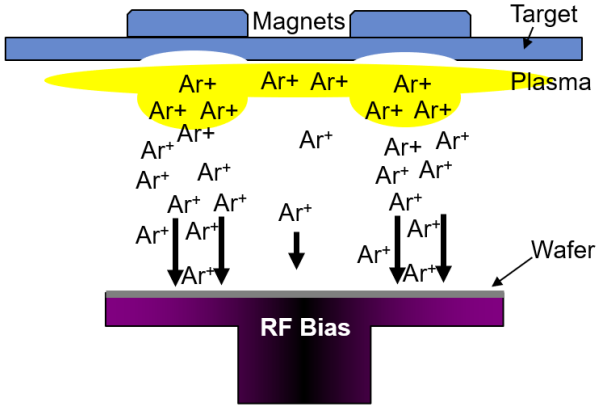


Fig. 1. Schematic representation of DC Magnetron highlighting ion density distribution across sputter target.

The high ion density region, coupled with wafer RF bias that is used to control the ScAlN mean stress, causes high ion bombardment towards the wafer edge, which leads to a high compressive stress. Conversely the low ion density region in the target centre leads to a more tensile stress. If no stress control measures are used, the magnitude of the WIW stress may be >500MPa (Fig. 2, top).

The Crossbow system controls WIW stress by reducing the ion bombardment variation across the wafer. This results in reduced WIW stress level to <100MPa (Fig. 2, bottom).

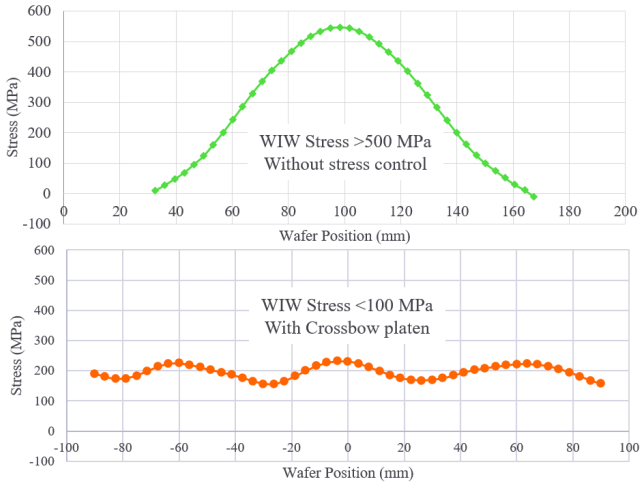


Fig 2. WIW stress for $Sc_{30at\%}AlN$ film with no stress control techniques applied, >500MPa (top) and with Crossbow stress control, <100 MPa (bottom)

Similarly, without stress control techniques the piezo layer mean stress will vary, particularly at the start of a batch of wafers (Fig 3., left). This means many conditioning wafers must be used to stabilise the stress, taking up to 2hrs production time. Using Crossbow the number of conditioning wafers can be reduced to one, with WTW stress < 30MPa. Importantly, WTW stress remains in control after short delays up to 30mins without additional conditioning (Fig 3., right).

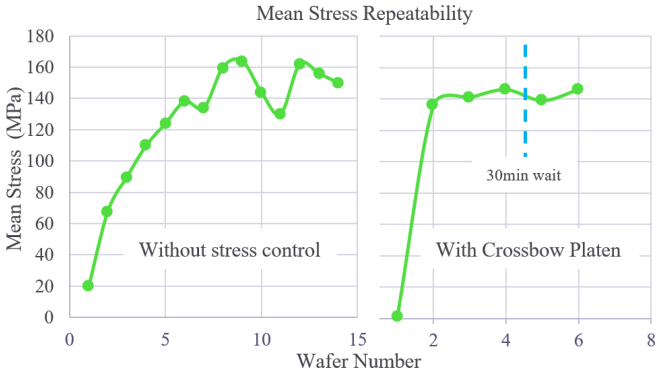


Fig 3. ScAlN WTW mean stress variation without stress control techniques (left), using Crossbow stress control (right)

Since ScAlN thickness non-uniformity is also important, the method of stress control should not have any detrimental impact on the thickness non-uniformity. Fig 4. shows thickness non-uniformity plot for the same $Sc_{30at\%}AlN$ film shown in Fig. 2 (bottom). Thickness non-uniformity is controlled to $\leq 0.3\%$ 1σ.

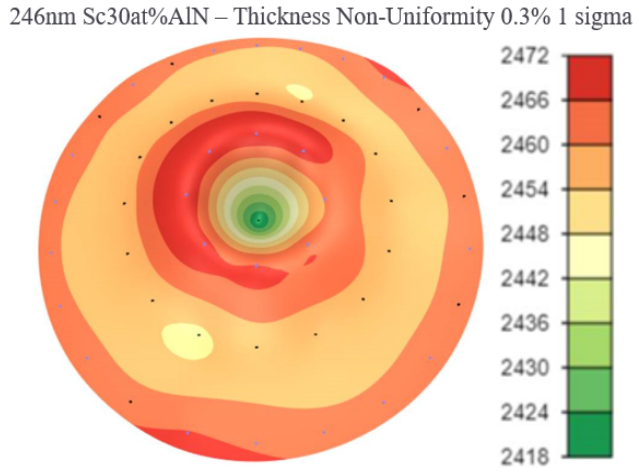


Fig. 4. Thickness non-uniformity plot for 246nm layer of $Sc_{30at\%}AlN$ deposited using Crossbow system

Crystal defect control techniques were developed for $Sc_{\leq 20at\%}AlN$ to give <5 defects per 100µm$^2$. The same control techniques were found to be ineffective for $Sc_{30at\%}AlN$ (Fig 5. left). Novel techniques have been developed to control defects in $Sc_{30at\%}AlN$ to <5 defects per 100µm$^2$ (Fig 5. right).

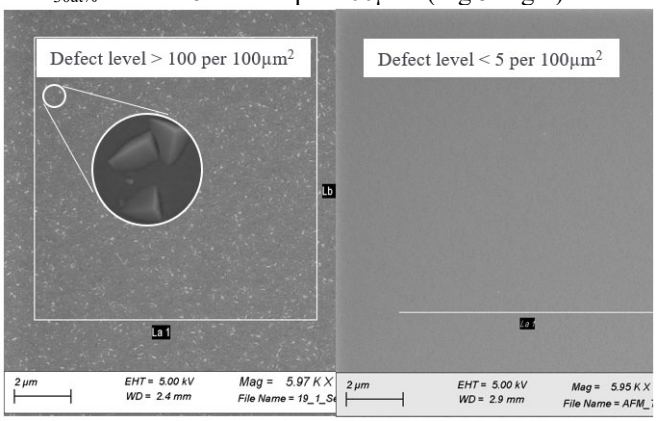


Fig. 5. $Sc_{30at\%}AlN$ deposited with poor (left) and good (right) defect control techniques

## ScAlN ETCH

Once the ScAlN film (and electrodes) have been deposited, the filter structure must be defined. As BAW filter feature sizes have reduced over time, the industry has moved from wet etching to dry etching to define the AlN piezoelectric layer (and the associated metal electrodes).

Fig 6 illustrates a typical structure that needs to be etched for a BAW device, with the piezoelectric layer sandwiched between two metal electrodes. There are multiple etch steps in the process (1) etching through the top electrode layer, typically <200nm thickness (2) etching the piezoelectric layer ≤1um and stopping on the bottom electrode with minimal loss and (3) etching the bottom electrode if required.

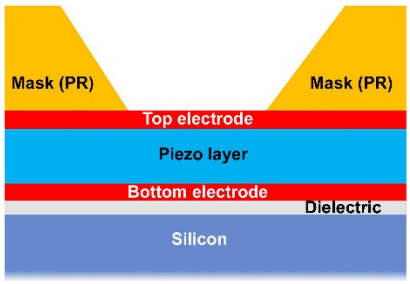


Fig 6. Simplified diagram of a typical BAW layer structure

Typical production requirements from device manufacturers for ScAlN BAW etching include WIW and WTW non-uniformity to maximise device yields, and high etch rate to improve productivity. Device makers are currently working on Sc content typically in the range of 15-40at%. Unfortunately, increasing the Sc content makes dry etching more problematic because of the low volatility of scandium halides relative to those of Al and N. In fact, this etch process becomes impossible in a standard ICP module at Sc-contents >25% (See Fig 7).

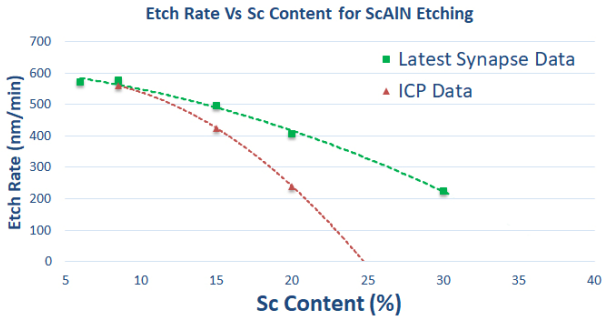


Fig 7. Impact of Sc content on etch rate in a standard ICP vs high density Synapse™ module

## INVESTIGATION

Recent data suggests that a standard ICP reactor is capable of etching un-doped AlN and ScAlN up to ~20% after which no productive etch rate is expected. For wider process capability and to future-proof technology selection this work has found that the Synapse™ plasma etch system, which has a unique source design offering x10 higher ion density than a standard ICP module offers a productive etch rate at much higher Sc contents. This high density source has been engineered specifically to etch strongly bonded materials such as ScAlN but also SiC, glass, sapphire and other materials. Recent studies conclude at low scandium content <10% the etch rate of the higher density source and ICP is comparable. However, as the Sc increase a steeper drop in etch rate is observed in the ICP module with high density source demonstrating 60% higher etch rate at ~20at% with a 400nm/min etch rate. At 30at% Sc the Synapse™ still offers productive etch rates of 230nm/min, where ICP would offer no viable etch (see Fig 7). Fig 8 shows a partial etch of a Sc30at.%AlN sample.

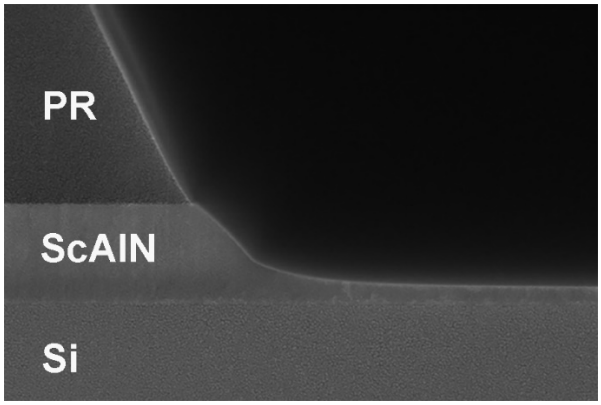

Fig 8. Partial depth $Sc_{30at\%}AlN$ Etch

As the bulk etch of the ScAlN layer nears the bottom electrode, process parameters are typically changed to minimise electrode loss. A soft landing step is implemented with a slower etch rate to provide typical electrode loss in the range of 10-20nm. For BAW devices, sidewall angle of the piezo layer is typically between 10-45° and tapering is preferred for subsequent coverage by thin films. This is achieved using a $Cl_2$-based plasma chemistry in the Synapse™ module, and by paying particular attention to the mask profile. As device size reduces, manufacturers are seeking steeper sidewalls so their features occupy less real estate. In cases where ScAlN is etched for MEMS devices the piezo layer profile are typically steeper at >70°. A common problem of etching any low volatility film is re-deposition of by-products on the wall or mask of the etched feature. These can be difficult to subsequently remove and can also obstruct the etch front. The more physical nature of the high ion density process and the lower operating pressure available allows for easier management of that re-deposition than in an ICP module, allowing Synapse™ to produce steeper profiles with less re-deposition (See Fig. 9).

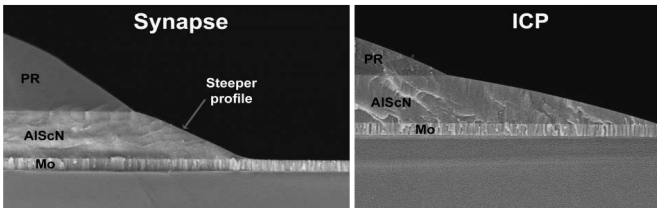

Fig 9. Comparison of etch profile ScAlN in high density plasma source & standard ICP

End-point control is essential to stop the etch at the required point, when etching the top electrode to the piezo layer or the stopping on the bottom electrode. In both scenarios, OES Optical emission spectroscopy can be employed to monitor the light emitting species of the plasma. End-point detection control improves wafer-to-wafer repeatability and help manage variations in layers thickness or etching rate - see Fig 10.

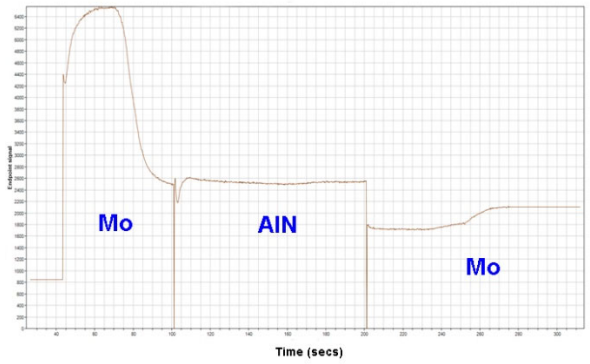

Fig 10. OES end-point trace for Mo/AlN/Mo stack etch

## CONCLUSIONS

ScAlN films with Sc content up to 30at% present a significant challenge to the BAW filter device manufacturer. Here we have presented solutions for the problems of $Sc_{30at\%}AlN$ deposition, namely control of WIW and WTW stress variation, thickness non-uniformity and growth of crystal defects, using the innovative Crossbow system.

A high-density plasma source offers significant advantages over a standard ICP reactor when etching for BAW manufacturing, in terms of productivity, selectivity and profile control for the AlN/ScAlN and lower electrode materials. The physical nature of the etch process is hugely beneficial as the trend for increased scandium content for emerging 5G applications continues, and where ICP will not be viable in the future.

## REFERENCES

[1] Soumya Yandrapalli et al, "Thin Film Devices for 5G Communications", IEEE MEMS 2021, pp 450 - 453

[2] Yokoyama et al, "Highly Piezoelectric Co-doped AlN Films for Wideband FBAR Applications", IEEE Trans. Ultrason. Ferroelectr. Freq. Contr. 62, pp. 1007-1015, 2015.

[3] V. V. Felmetsger and M. K. Mikhov, "Reactive magnetron sputtering of piezoelectric Cr-doped AlN thin films" 2011 IEEE International Ultrasonics Symposium, Orlando, FL, USA, 2011, pp. 835-839.

[4] Mayrhofer et al, "Microstructure and Piezoelectric Response of $Y_xAl_{1-x}N$ Thin Films", Acta Materialia 100 (2015), pp 81 - 89

[5] Umeda et al, "Piezoelectric Properties of ScAlN Thin Films for Piezo-MEMS Devices", IEEE MEMS 2013, pp 733 - 736

[6] R. Aigner, "Bringing BAW Technology into Volume Production: : The Ten commandments and the seven deadly sins", IEEE Int. Symp. Acoust. Wave. Dev. for Future Mobile Communication Syst. 2007.

# Developing production process for high performance piezoelectrics in MEMS applications

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**Keywords: Aluminium Scandium Nitride, BAW, piezoelectric MEMS**

**Abstract**

**The technical challenges in the deposition of $Al_{1-x}Sc_xN$ films are discussed, with specific focus on the manufacturing of bulk-acoustic-wave (BAW) resonator-based filters for radio frequency (RF) communications. The advances in physical vapour deposition (PVD) techniques are introduced. Besides of enlarging the sputter target, the use of a DC+RF source allows us to achieve stress levels of less than ±50 MPa over the whole wafer surface (up to 5mm edge exclusion). Misoriented grain density has reached satisfactory levels of ~0.1 µm² over 2.5×5 µm² area for $Al_{0.7}Sc_{0.3}N$ thin films. An example of stress engineering of free-standing cantilever is also presented.**

## Introduction

The huge interest in increasing the operating frequency and bandwidth of the RF filters driven by the 5G wireless technology demands new materials with enhanced electromechanical coupling coefficient. Not any more satisfied with AlN thin films for BAW RF filters, material scientists have devoted considerable efforts to improve the its properties by exploring the effects of statistical substitution of Al with other elements in the periodic table. It is in this context that Akyiama and his co-workers [1] reported a dramatic increase in the piezoelectric coefficient when Sc atoms replace Al ones up to approximately 43% in 2009.

Within the frame of $Al_{1-x}Sc_xN$ thin films, extending BAW technology to higher frequencies requires the use of thinner films and higher levels of Sc dopants to keep the coupling coefficients at the largest level dictated by bandwidth requirements. However, high Sc doping level also poses new challenges for $Al_{1-x}Sc_xN$ thin film deposition. This includes the alloyed target manufacturing, the stricter requirement for stress range and more difficult control over the textured film growth.

In this paper, we discuss the challenges for $Al_{1-x}Sc_xN$ thin film processing and our approaches to achieve highly uniform $Al_{1-x}Sc_xN$ films with stress range under 100 MPa. In the end, we demonstrate with an example how to achieve free-standing cantilevers for bimorph structures.

## Technical Challenges for $AL_{1-x}SC_xN$ thin film processing

When it comes to the production of $Al_{1-x}Sc_xN$ thin films for the industry, three challenges have to be solved:

- How to introduce Sc into AlN lattice efficiently;
- How to control the stress and thickness uniformity of the $Al_{1-x}Sc_xN$ film across the wafer;
- How to maintain the AlN Wurtzite textured lattice growth with a certain Sc doping level.

While other deposition techniques like metal-organic chemcial vapor phase deposition and pulsed laser deposition start to emerge in this field of application, sputter deposition is still the mainstream technique to deposite $Al_{1-x}Sc_xN$ films.

A versatile approach to deposite $Al_{1-x}Sc_xN$ thin films is co-sputtering, where Al and Sc targets are sputtered independently and simultaneously in the same chamber. The Sc concentration can be adjusted by changing the power ratio of the two targets. Flexible and ideal for process development, this approach is not ideal for mass production, as it is very challenging to ensure adequate stress control (more about this topic later) and to achieve high levels of productivity. Therefore, this technique is mainly used for research purposes and played a very important role in the early stage of $Al_{1-x}Sc_xN$ exploration.

The preferred solution is therefore to use the same proven configuration already existing for high volume fabrication of RF filters with a single wide target. To do this, we need an $Al_{1-x}Sc_x$ alloyed target with the same dimension. Though difficult due the complexity of Al-Sc bianry alloy system [2], fabrication of such a target is nevertheless feasible. The business case represented by opportunities in 5G communication has stimulated target manufacturers to make significant investments, resulting in remarkable improvements throughout a whole range of Al-Sc compositions in the recent years. It is now possible to produce high-quality, high-Sc content targets (up to 40%Sc), which enables the mass production of $Al_{1-x}Sc_xN$ throughout the whole piezoelectric range of the phase diagram.

The Sc content is not the only parameter which influences $k_t^2$, as the piezoelectric response is also influenced significantly by the film stress (see Fig. 1.). Extremely accurate stress control within the wafer surface and from wafer to wafer in any production process is then essential for the successful production of RF filters of bandwidth precision dictated by the wireless communication standards. For Sc contents of about 30%, only deviations of ± 50 MPa are tolerated: an extremely small value for thin film depositions.

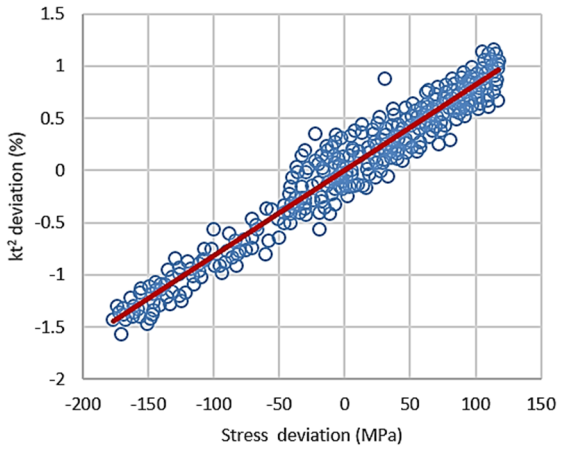


Fig. 1. Electromechanical coupling coefficient variation as a function of the stress variation for $Al_{0.7}Sc_{0.3}N$ based resonators. The two physical quantities are linked linearly. The steepness of the line increases with the Sc concentration.

For high Sc content $Al_{1-x}Sc_xN$ films, another obstacle is the tendency of these materials to show abnormally thick, misoriented crystallites or grains [3]. The introduction of Sc into the AlN Wurtzite lattice creates instabilities in the lattice and very often misorientated grains grow during the film deposition. These grains grow at a faster pace than the textured grains and appear on the film surface as pyramid shaped structures. These grains are still in the Wurtzite phase, but their (0002) axis is not perpendicular to the wafer surface. The appearance of misoriented grains causes an obvious decrease of the piezoelectric coefficient, which becomes evident only when their density exceeds a critical threshold. An excessive amount of those grains can also negatively influence the dielectric loss and cause problems in post-processing due to the very high film roughness, as these grains can be tens of nanometers taller than the film surface. Thus high Sc content $Al_{1-x}Sc_xN$ films are applicable only when the density of misoriented grains is below a certain level.

## Recent advances in $Al_{1-x}Sc_xN$ thin film processing

The efforts in the process development for $Al_{1-x}Sc_xN$ thin filmes are mainly dedicated to improving the thickness uniformity, narrowing down the stress range and enhancing the textured film growth.

A simple approach to achieve better compromises between stress and thickness uniformities is to employ an enlarged target diameter. This allows us to reduce the strength of the magnetic field at the wafer edge and/or to enhance the target-to-substrate distance for a given thickness distribution. Under both circumstances, the inhomogeneity of the ion bombardment over the wafer surface is reduced, thus favoring a more uniform stress distribution. Fig. 2. shows an example of 1 µm AlN deposition using an enlarged Al target ($\Phi$ = 340mm). Excellent thickness uniformity and stress range up to 5 mm edge exclusion can be easily achieved.

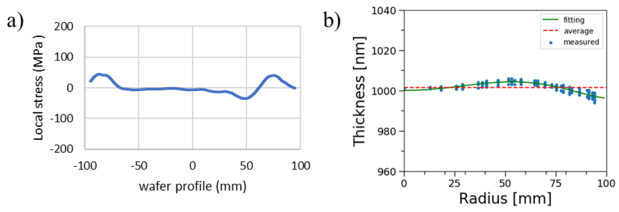


Fig. 2. The a) stress and b) thickness profiles of 1µm AlN film deposited using an enlarged Al target (340 mm). The stress range can be easily controlled under 100 MPa and the thickness uniformity (1σ) is under 0.3%. Measurement edge exclusion: 5 mm.

On the downside however, this approach worsens the cost of ownership figure as it implies a bigger vacuum chamber, larger cleanroom footprints, and, most importantly, a much higher target cost per wafer (if it is at all possible to get manufactures able to go beyond the usual target sizes for $Al_{1-x}Sc_x$ alloyed targets). An alternative way to deal with the issue is to manipulate the stress distribution while keeping the optimized magnetron configuration and target to substrate distance for ideal thickness distribution. This is possible with DC+RF technology.

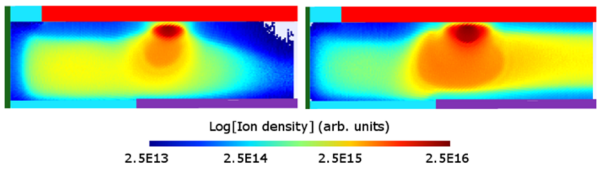


Fig. 3. Plasma density distribution simulations for a DC+RF chamber. The pictures refer to a cross section with radial symmetry (a mirror plane condition has been imposed at the right-hand side of the graph). The change in the distribution between the left and the right picture is only due to a different phase shift between the RF signal applied to the target and the one applied to the substrate. This can be then used to modulate the ion bombardment, and, in turn, the stress distribution.

The DC+RF sputtering superimposes the DC power with an RF power on the cathode. It still enables the sputtering in the DC mode, as the RF power serves mainly to discharge the target surface in a reactive process. Therefore, the good thickness uniformity from DC sputtering is preserved. Additionally, the RF power applied to the target can be sychronised to the RF power to the chuck for wafer biasing. Each time we have multiple RF signals applied to the same plasma, we can shape it if we influence the relative amplitude of the signals and the phase shift between them. As we can see from Fig. 3, the plasma intensity in a reacto can be changed locally by several orders of magnitude for different RF settings.

The combination of DC+RF is also commonly used in a variety of applications for other advantages which are offered by this technique. The transfer of this mature technology to $Al_{1-x}Sc_xN$ depositions allowed us to achieve very narrow stress distributions up to the wafer edge, and satisfy the ± 50 MPa limit requirement dictated by large amount of scandium substitution while keeping the thickness distribution easily trimmable (< 0.5% sigma/mean) and target dimensions to the conventional ones (about 300mm diameter), as seen in Fig. 4.

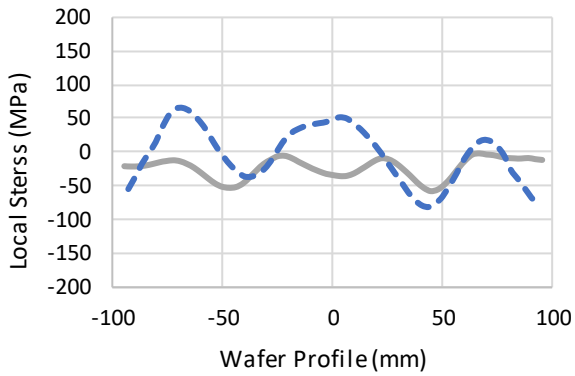


Fig. 4. Comparison between stress profile with DC-pulsed process (dashed line) and DC+RF (solid line). Thanks to the additional process parameter which influences mainly the plasma distribution over the wafer surface, we achieve high levels of stress uniformity. Measurement edge exclusion: 5 mm.

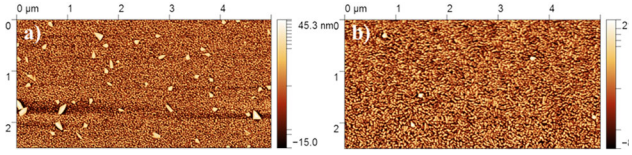


Fig. 5. AFM pictograms of $Al_{0.7}Sc_{0.3}N$ thin films obtained under identical conditions on two different types of bottom electrodes. A significant reduction of the unwanted grain density can be achieved with a pre-treatment of the electrode before the piezoelectric thin film deposition.

The misoriented grains related to high Sc content $Al_{1-x}Sc_xN$ films have been intensively studied in the past years. As demonstrated by Sandu *et al.* [3], the presence of these abnormal grains can be associated with an excess of Sc at the grain boundaries. Target manufacturing and processing conditions can therefore significantly influence the presence of these grains. Process conditions that enhance the ion bombardment inhibit the growth of misoriented grains. Nevertheless, other requirements in terms of thickness and stress distribution give us very limited freedom in the choice of the process conditions, especially the requirement of having neutral or slightly tensile films. If we produce too compressive films, the benefit of high Sc content in the Wurtzite structure is lost by the loss of coupling coefficient given by the stress state (see again Fig. 1.). For a given target and processing condition, the number of misoriented grains can also change drastically from substrate to substrate type. On W bottom electrode it is relatively easy to grow smooth films, while the number of misoriented grains is increased if we switch to Mo electrode or bare Si. The lattice mismatch between the film and the substrate seems not to be the root cause, however, as the processing conditions of the electrodes have a big influence, as we can see in Fig. 5.

## STRESS ENGINEERING FOR FREE STANDING BI-MORPH CANTILEVERS

Different from the growth of metallic films, $Al_{1-x}Sc_xN$ film is a reactive process and releases heat during the formation of $Al_{1-x}Sc_xN$ compound. As a consequence, the wafer temperature rises up during deposition to a much larger extent than metal depositions. This leads to an extensive stress gradient along the thickness of $Al_{1-x}Sc_xN$ films, which limits the introduction of $Al_{1-x}Sc_xN$ film for applications where free-standing microstructures are required. However, if there is sufficient thermal contact between the wafer and chuck, the temperature rise of the wafer during deposition will be damped and thus the stress gradient will be reduced. This can be realized with electrostatic chucking solution. The wafer is gripped by electrostatic force on the chuck, while underneath the wafer, a gas pressure is maintained between the wafer and the chuck. This gas pressure enhances the thermal transport between the wafer and chuck, thus minimizing the temperature variation on the wafer during deposition. Additionally, the deposition is still full-face, as there is no need for mechanical clamping.

With the reduced film stress gradient, it is possible to compensate the bending moment and achieve flat structures with careful stress engineering. Fig. 6. shows one example of stress gradient compensation for a freestanding bimorph structure. The in-plane stress for every 100 nm thickness is plotted against its distance to the corresponding electrodes for

the first and second piezoelectric films in Fig. 6 c) and d). As one can see, there exists a large stress gradient in the first 200 nm of the as deposited film. Without any stress compensation, the stress gradient will cause a bending moment when the cantilever is released:

$$M = \int_{-t_f}^{t_f} \sigma(t) \cdot t dt = \int_{-t_f}^{0} \sigma(t) \cdot t dt + \int_{0}^{t_f} \sigma(t) \cdot t dt$$

where M is the bending moment, σ(t) is the in-plane stress at the distance of t to the middle electrode. Since the electrode layer is usually very thin and free from stress gradient, we can consider component from $-t_f$ to 0 as the contribution from the first piezoelectric film and 0 to $t_f$ from the second piezoelectric film. In order to keep the freestanding cantilever flat, we have to ensure the total bending moment to be zero. Of course, the most straightforward way to achieve this is to keep σ(t) as a constant through the whole cantilever. However, in reality, this requires extensive *in-situ* stress tuning during the deposition, which is not easily manageable. One other approach is to ensure the sum of the two bending contributions from the two films to be zero. The most convenient way is to compensate the bending moment by changing the stress of the top 100 nm layer of the second piezoelectric film, which is the finishing layer of the deposition, as indicated by the green triangle in Fig. 6. d). With this approach, we managed to bring down the deflection of cantilever dramatically after release, seen in Fig. 6. b).

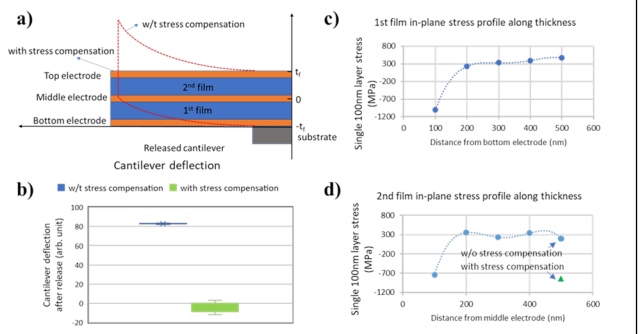


Fig. 6. a) Illustration of a bimorph freestanding cantilever with and without stress compensation; the in-plane film stress for every 100nm is plotted against its distance to the corresponding electrode planes for the first c) and second d) piezoelectric films. The top 100nm film stress with stress compensation for the second film is highlighted in green dot. b) The bow of the released cantilever without and with stress compensation. The deflection values are plotted with a scaling factor.

## Conclusions

The introduction of $Al_{1-x}Sc_xN$ technology represents a leap forward in the piezo-MEMS industry. The limits of pure AlN with its relatively small piezoelectric activity can be overcome. This allows significant improvement in the performance of devices such as piezoelectric microphones and pMUTs which can still be integrated in a CMOS chip or production line. The enhancement of the electromechanical coupling coefficient allows extended application range of BAW-based RF filters to broadband communication, which would not have been accessible with pure AlN only.

The integration of $Al_{1-x}Sc_xN$ films poses however several challenges. The historic difficulties in target manufacturing represented a significant hurdle in the productization of such a technology for a long time and limited users to cosputtering setups for relatively high Sc concentrations. However targets of 12 inches in diameter are now available for almost all the Sc concentration range of interest. The stress dependency of the electromechanical coupling coefficient is enhanced as Sc content gets higher. As a consequence, in order to achieve high yield figures on each wafer, advanced plasma shaping techniques are necessary. At Evatec we employ a DC+RF technology to finely adjust the plasma distribution over the wafer surface. This technique allows us to reach stress distribution over the wafer surface less than ±50 MPa up to 5mm edge exclusion and well within the range required for application in high performance RF applications. The existence of misoriented grains for high Sc content $Al_{1-x}Sc_xN$ films may currently put some refrains for the industry to increase the Sc content to the limit. But with improving techniques of target manufacturing, proper wafer substrate choice and treatment, and optimization of process hardwares and conditions, $Al_{1-x}Sc_xN$ continues to be the dominating material in the field of piezo-MEMS and 5G wireless communication applications.

## Acknowledgements

The authors would like to thank the Evatec colleagues and collaborators for carrying out experiments and collecting results.

## References

[1] M. Akiyama, K. Kano, and A. Teshigahara, Appl. Phys. Lett. **95**, 162107 (2009).
[2] M. O. Shevchenko *et al.*, Powder Metall Met Ceram **53**, 243 (2014).
[3] C. S. Sandu *et al.*, Phys. Status Solidi A **216**, 1800569 (2019).

## Acronyms

BAW: Bulk Acoustic Wave
MEMS: Microelectromechanical System
RF: Radio Frequency
PVD: Physical Vapor Phase Deposition
DC: Direct Current

# Continual Improvement of Cumulative Yield in GaAs Wafer Fabrication

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***Keywords: MAX Precision Excellence (MPE™), Benchmarking, Engineering Best Practices, Statistical Process Control (SPC), Process Capability (Cp, Cpk), Process Yield, Cumulative Yield, Predictive Yield Model, Scaled Estimates***

## ABSTRACT

Improvement of corporate level profit margin is a continual theme within all production operations. Those operations commonly target high quality and reliability while reducing manufacturing costs through management of wafers processed, cycle time, process yield and product yield. Implementation and acceleration (12 months) of continual improvement in these metrics are accomplished through benchmarking and implementation of best process engineering practices. This paper discusses improvements accomplished in process yield, quality process control, and product yield made during a recent joint project between MAX I.E.G. LLC and a GaAs Wafer manufacturer client.

## INTRODUCTION

"If left to themselves, machines do not stay adjusted … a stable stationary state is an unnatural one and its approximate achievement requires a hard and continuous fight." [1]

The arduous effort of continual improvement requires measuring what is to improve, and trending what is measured. Establishing aggressive but achievable goals for each measured characteristic is equally as important as the quality skills and tools available to the engineering teams. An upward trend is the obvious desired effect however long term reduction in variation and stabilization at newly improved levels are the ultimate proof that the "fight" is won.

This paper showcases the method and result of a structured implementation of the MAX Precision Engineering (MPE™) business process. Wafer fab operational gains were achieved through immersive implementation of best practices in continual improvement and statistical process control methods. Quantitative gains are achieved in both in-line production quality and end-of-line test yield.

## METHODOLOGY

A MAX lead-in assessment identified the following MPE business process components for which the client agreed to engage for an accelerated implementation:

- Client to internally revisit/refresh product based process FMEA's (results not included here-in)
- Engineering SPC best practices; assess, teach and mentor 31 topics in 10 categories
- Critical chart classification for reliability, function and process; ensure alignment of in-line charts to cumulative yield without impairing client customer quality
- In-line SPC chart set-up maturity; assess and ensure five basic aspects of chart set-up
- Continually improve critical in-line SPC process capabilities; Cpk's to ≥ 1.33, for implied later yield gain
- Implement SPC practices for end-of-line electronic test characteristics and correlate to in-line variation

The immersive application of these quality skills and tools resulted in a more cohesive process control system, reducing in-line excursions/escapes and enabling more highly correlated feedback from end-of-line test to enable interactive continual improvement in production. MAX Precision Engineering defines a path to best-in-class objectives and measures progress of team execution to goal. (Table 1)

| Key Performance Objective | KPI Measure / Goal |
|---|---|
| ▪ Product based PFMEA | Performed by client, excluded here |
| ▪ Engineering Best Practices | Qualitative best-in-class behaviors |
| ▪ Critical chart classifications | Align In-line to End-of-line yield |
| ▪ SPC Chart Set-up Maturity | Score ≥ 8 of 10 for all critical charts |
| ▪ Continually Improve Cp/Cpk | 100% of critical charts ≥ 1.33 Cpk |
| ▪ OE Test Monitor Chart Set-up | Identify Fab & Tester instabilities |
| ▪ Continually Improve Test Yield | Yield goal varies by product |

Table. 1: Key aspects and goal setting for teaming success

RESULTS

Engineering Best Practices

One major aspect of the joint project is to teach, mentor and transform the engineering mind set to use documented best practices (quality skills and tools) as the new default. Client engineering practices were assessed on a quarterly basis throughout the implementation and, in most cases, improved to industry benchmarked levels. (Fig. 1)

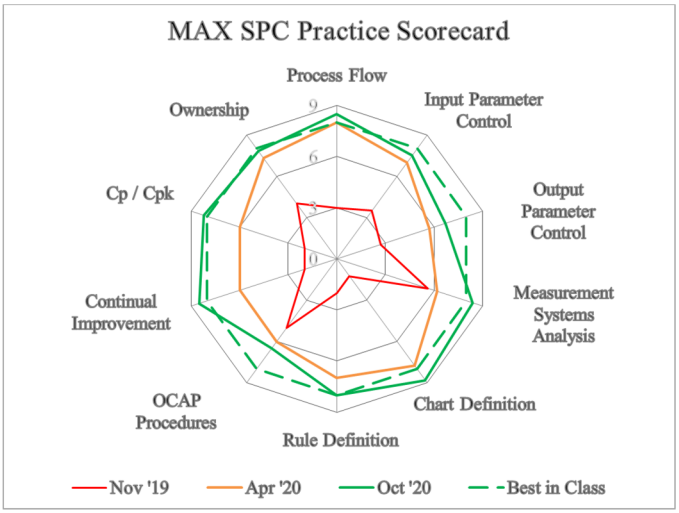


Fig. 1: Measured qualitative improvements in 10 categories of engineering best practices in statistical process control

The criteria supporting each of the 10 practice categories are well defined in many quality control publications, however some pragmatic assumptions were made in order accelerate implementation. For instance, the initial application of WECO rules was limited to alert at an "appropriate level" and gradually increased to allow focus on the most significant concerns as we simultaneously tightened control limits. Also, the Input and Output Parameter categories were defined from a product-lot-perspective in order to emphasize a feedback network between in-line and end-of-line performance.

As many other Fabs, the client's team already had good SPC practices in several categories including; measurement systems, a control plan from design timeframe, placement of control plan charts within product routings and out-of-control action plans. Categories to improve included; chart ownership, chart definition, rule definition and continual improvement of process capabilities. So the implementation focused first to drive SPC chart set-up maturity, then continual improvement of process capability.

SPC Chart Setup Maturity

Maturity of existing charts was assessed against five basic set-up criteria. A metric was devised with a goal to accelerate completion of four aspects and to initiate a continual improvement process for the fifth aspect. A score card was established and pressed for completion. Early setup issues where identified and systematically addressed, including:

- Chart type gaps
- Control limit calculation method
- Inadequate application of WECO Rules
- MES chart setup gaps

Scoring criteria and final result histogram are shown in Fig 2.

| M-score Criteria for chart maturity (48 charts) | Value |
|---|---|
| 1. Is SPC chart in use in real time? | 2 pts |
| 2. Is OCAP in place for OOC / OOS? | 2 pts |
| 3. Are Control Limits statistically determined? | 2 pts |
| 4. Are adequate WECO rules turned on? | 2 pts |
| 5. Is CPk ≥ 1.33? (Goal = 100% | 2 pts |
| M-score maximum per chart | 10 pts |

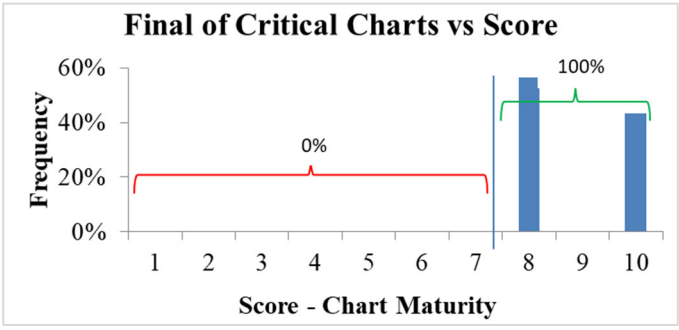


Figure 2. Chart set-up criteria and final score card

Process Capability Maturity

The fifth aspect of chart maturity is process capability which is normally addressed longer term with continual improvement teaming strategy. The client process engineering team once again committed to an aggressive goal and schedule. A continuous improvement team involving all process area section managers was kicked off as soon as the chart setup goals were achieved. Membership successfully ensured priority and acceleration of implementation.

MAX also joined by-area engineering chart reviews which were occurring prior to the start of the project. All SPC meetings and follow up discussions became opportunities to teach, mentor and demonstrate the best practices described above.

Deeper dive actions were needed after resolving the early limitations. A bulk listing of individual factors limiting process capabilities was provided to create a high-level view of the increasingly difficult improvement opportunities. Cpk is a function of distribution shape, centering and control limit settings. The later and more difficult phase of process capability improvement was made more navigable by mapping each factor for each chart needing attention. A final wave of Cpk issues was prioritized by potential gain and degree of difficulty and driven to the goal through team actions. The final

and most difficult opportunities involved slightly misshapen distributions as shown using Skew in the map in Table 2.

MSA gauge capability / fitness did not require much attention during the joint implementation. P/T Ratios are included in Table 2, showing minimal negative contribution in the last wave of chart improvements.

| Process Group | | GRR/SPEC Tolerance | | Sep 2020 Skew | # STDs off target | Calculated Control Range Vs Fixed Range |
|---|---|---|---|---|---|---|
| 1 | | | | | | |
| 1 | | | | | | |
| 1 | | | | | | |
| 1 | | | | | | |
| 1 | | | | | | |
| 2 | | | | | | |
| 2 | | | | | | |
| 2 | | | | | | |
| 2 | | | | | | |
| 3 | | | | | | |
| 3 | | | | | | |
| 3 | | | | | | |

Table 2. Map of Cpk issues in the last layer of improvement (Numbers are removed to protect client's data)

The process capability score card in Figure 3 reflects monthly results throughout the continuous improvement teaming activity. The changes in slope of the data trend clearly show the initial easier gains, the tapering off of easy gains, and the more difficult period (staying linear in final phase) aided by revelations from the monthly opportunity maps.

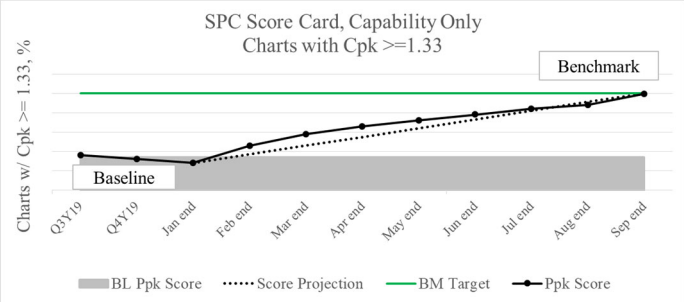


Fig. 3: Percentage of Critical Charts with Cpk >=1.33

The process capability gains above were thought to be a huge challenge by management and team members, especially within the set one year time period. Introduction of best practices, concise performance metrics, and drill-down continual improvement tools allowed the team to exceed expectations and in several cases to reset the MAX best-in-class engineering behavior levels. (Refer back to the spider chart in Figure 1 above.)

Wafer Process Yield

MAX joined existing client activities in the area of process yield loss reduction. As many other GaAs wafer manufacturers, wafer scrap is identified as a top cause of process yield loss and a key detractor from cumulative yield goals. The existing effort was reconstituted with the introduction of benchmark best practices for teaming and continual improvement which were practiced over time. Better analysis tools were provided to help accelerate results.

Strategies were implemented to ensure the new teams were setup to succeed:

- Priority was established and vertically aligned throughout the organization, from Fab manager to front line operator
- Clear trending indicator was devised to track improvements in wafer-loss count and to translate the losses into a more relatable loss-value metric
- All loss categories were redefined within the MES to enable use of multi-level Pareto analyses
- A stand-alone data display tool was extended to show the MES extracted process yield loss data in real-time in a multi-level Pareto, drill-down, format
- Owners were identified and empowered to work with cross functional resources in each major category using the improved drill-down analysis tool
- Periodic management reviews were modified to emphasize and expect improving trends in multiple Pareto drill-down categories, (enabling 12 total simultaneous continual improvement activities within the top 4 loss categories.

Wafer scrap during fabrication of not only GaAs-based manufacturing but many other Compound Semiconductors is very much aggravated by substrate brittleness. As such it was a top loss category and the first demonstration of success in continual improvement of process yield. Real root causes and solutions were contributed exactly as the vertically aligned priorities intended. Process, equipment and operations personnel came together on the factory floor and in working sessions to identify and implement lasting solutions. Internal data continues to verify permanence of each solution.

There were two cycles of improvement and stabilization effected by continual improvement efforts:

- Manual data analyses; non-standard across user base and shallow dives, drove a 60% reduction in lost value to the Fab
- Best practices in place; Real-time three-level Pareto analyses standardized for all users enabling structured deep dives, drove an additional 71% or 89% cumulative reduction in lost value to the Fab

Both periods were effective in reducing mean and variation due to good team effort however it is clear that aggressive priorities, expectations, and better continual improvement tools empower the teams to effect and maintain more dramatic gains.

Electronic Product Yield

G. Box et.al. [1] describe two types of variation as permanent and transitory and how the former may corrupt correlations and attempts to predict end-of-line yield using the transitory manufacturing data.

"(An example of a permanent component is) when any procedure in manufacturing is slightly changed in a manner not regarded as important, or perhaps not even consciously realized or remembered. The accumulation of undetected permanent components of the noise produces "nonstationarity". … "Nonstationarity reflects the steady increase of entropy (disorganization) that occurs in any uncontrolled (portion of a) system. … The aggregated permanent components produce a continuous increase in entropy. The purpose of quality control is to reduce or possibly nullify th(is) effect…" [2]

Pyzdek (1990) was credited for this concept in the Box publication. "… every deviation must be caused by something and what is called a special cause and what is called a common cause entirely depend on the level of what we choose to call residual noise. If this can be reduced, more "special causes" will become evident."

The author takes poetic licence to alter the intent of Box's original focus. The client found that attempts to model the impact of in-line variation on electronic device performance were mostly inconclusive due to the aggregation of noise from other known unavoidable causes of variation within the production line. A prime example is the impact from known minor variations of incoming substrate characteristics on electronic performance.

Another critical activity in this project was the set up of sequential Least Squares Regression models to quantify and filter out the aggregated permanent noise from the Fab database and identify new transitory causes. These models were owned and sustained by the client. Secondary SPC treatments of the normalized scaled estimates provided a time-based trending of the model's individual term coefficients. These secondary control charts clearly indicated new transitory variations in electronic performance that could then be correlated back to specific in-line process steps. As claimed by Box and Pyzdek, reducing aggregated permanent noise within the predictive yield model made it easier to discover other assignable in-line causes.

The early efforts did connect several process control issues to product yield losses and contribute to achievement of the cumulative yield goal, see Table 3. However, as of the end of the joint effort we were unable to fully translate the in-line process capability gains to the end-of-line product yield gains.

| Product | Metric | % Improvement |
|---|---|---|
| High Runner 1 | Cumulative Yield | 17.6% |
| High Runner 2 | Cumulative Yield | 5.7% |
| Development 1 | Parametric Test Yield | 11.4% |
| Development 2 | Cumulative Yield | 180% |

Table 3: Quantitative gains in cumulative yield

The client has committed post project resources to continue refinement of the critical feed-forward / feed-back of predictive yield information

## CONCLUSION

The MAX Group was chartered to drive process and product yield objectives in a GaAs-based wafer fabrication facility. The charter was fulfilled through joint implementation of a MAX business process which teaches, mentors and practices excellence in precision engineering through industry benchmarking of process engineering and quality process control best practices. Qualitative best practice categories were committed to the client including; continual improvement, process and equipment sustaining (especially long down events), process and yield management, and SPC for process and product. All best practices were addressed through immersion to coach existing engineering efforts. The SPC and cumulative yield categories were addressed with a much more quantitative program, throughout the duration of the project.

The project resulted in improvements in cumulative yield of 6%, 11%, 18% and 180% for four respective product lines. Guided continual improvement activities achieved significant improvements in process yield, quality process control, and product final test yields.

## REFERENCES

[1]Box, G., Luceño, A., Paniagua-Quiñones, C. M. d. *Statistical Control by Monitoring and Adjustment*. Wiley 2009.

## ABBREVIATIONS

I.E.G.: International Engineering Group
SPC: Statistical Process Control
MES: Manufacturing Execution System

# Benzocyclobutene (BCB) Process Development and Optimization for High-Speed GaAs VCSELs and Photodetectors

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**Keywords: Benzocyclobutene, Reactive Ion Etching**

**Abstract**

**The RIE dry etching of Benzocyclobutene are studied to develop a compatible process for high-speed VCSEL and PD fabrications. SF6, O2 and N2 are selected as the process gases with their functions in the dry etching process explained. Optimal gas ratio of SF6 to O2 is 1:4. Controlled experiments are performed to identify the optimal power and pressure configurations for a new RIE system. The main problem is pointed out to be excessive physical sputtering from experiments. A clean etching recipe is finally developed to produce ideal etching results.**

## INTRODUCTION

Benzocyclobutene (BCB) based polymers are commonly used in microelectronic processing as dielectric materials for their low dielectric constant, negligible RF loss and high DC resistivity. In that case, a dry etching process to selectively remove BCB is necessary to shape the device structure such as opening vias for metal interconnect. A well-calibrated etching process is expected to create a smooth etch surface with minimum residue. BCB plasma etching is more complicated than common polymer or semiconductor etching in that BCB based polymer contains both organic materials and Si. Both must be removed simultaneously to achieve a smooth etching surface. In this work, we start from a recently implemented and unfamiliar RIE tool and design experiments to develop RIE etching process to improve the BCB surface morphology. Experimental results are shown to illustrate the effects of temperature, pressure, gas ratio in the process of polymer plasma etching.

## EXPERIMENT TARGETS

The BCB etching process of this work is developed for high-speed GaAs vertical-cavity surface-emitting lasers (VCSEL) [1] and photodetectors (PD). The epitaxial materials of VCSELs and PDs are first grown with MOCVD or MBE tools to pre-define the P-i-N diode structure. And the following fabrication process mainly focuses on shaping the physical device structure. It usually starts with an ICP/RIE etching process to define the mesa structure and exposed the

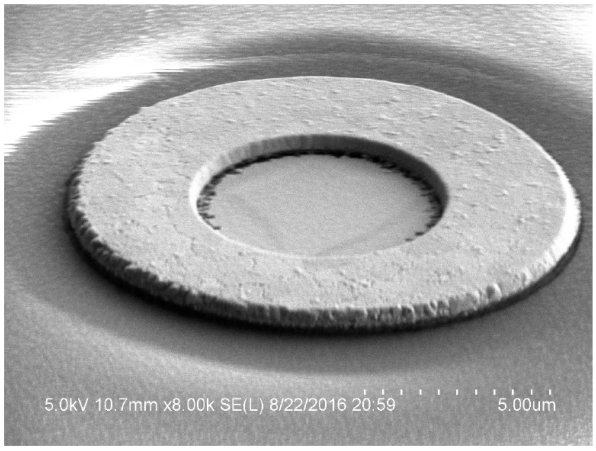


Fig. 1. VCSEL devices with BCB residue covering the aperture.

N-doped semiconductor layer. Contact metal is subsequently deposited onto the P- and N-doped layers. The samples are then planarized with BCB before selectively removing the BCB to reveal N- and P- contact. The last step is to deposit top metal contact which forms tapered GSG or GS waveguide. The BCB in this process has three main functions: planarization, DC isolation and RF signal carrying. VCSELs commonly have around 20 pairs of P-DBR structure in the P-doped region to confine the optical field. This will result in a height difference of up to 4 μm after defining the mesa structure. To allow for good interconnect to the large probing pad, the device must be planarized first. Apart from planarization, the co-planar waveguide structure to couple the RF signal into/out of the devices requires a low-loss dielectric to isolate DC coupling and carry the RF signals. Absence of dielectric material beneath the metal pads of the waveguide will cause the RF signal to leak into the substrate before reaching the devices. BCB is an ideal dielectric material for having high breakdown voltage, small dissipation factor and dielectric constant.

The experiments discussed in this work are focused on two major goals to be compatible to the fabrication process. The first target is to expose a clean semiconductor aperture in

the BCB etch-back process so that optical output uniformity is not affected by the BCB residue of random shapes and sizes as shown in Fig. 1 [2]. The second target is to ensure the smoothness of the BCB surfaces after etching to maximize adhesion to the top metal contact layer. Poor adhesion may result in metal peeling off during probe testing and wire bonding.

## Reactive Ion Etching Process of BCB

The BCB-based resin discussed in this work are Dow CYCLOTENE™ 3022 series resins which contains silicon in its backbone polymer. It is a common practice to selectively removed BCB material through reactive ion etching (RIE). An RIE process chamber consists of a grounded shower head and a bottom electrode with negative self-bias. Plasma is generated in the process chamber and reactive ions species are attracted to the bottom electrode where processing wafers are placed. The etching is realized with both chemical reaction and physical sputtering.

Process gases used for BCB plasma etching are SF6, O2 and N2 [3]. Fluorine ions in SF6 are aimed to remove Si and O2 serves as the main reactant to burn away other organic polymers. Insufficient SF6 will results in the formation of SiO2 in a O2 rich environment. The nonvolatile product SiO2 can only be removed through further reactions with fluorine ions. It is more likely to accumulate in random shapes and block further etching, producing in a rough etching surface. On the other hand, abundant SF6 will cause the lack of main reactant O2 and induce uniformity issues due to a slow etching rate. Previous works [3] have shown that the optimal ratio of SF6 to O2 is approximately 1:4 which should apply universally in most properly designed RIE systems. The third process gas N2 does not react with either polymer or silicon. However, it will participate in the phsycial etching process instead of simply diluting the reactive process gases. It is theorized to remove silicon through physical bombardment and create active centers to assist in the reactive etching process. Consistent increase in the etching rate is observed in our experiments by adding a small amount of N2 in addition to SF6 and O2.

Besides gas ratios, the remaining factors affecting the dry etching process are mainly temperature, plasma power and pressure. Temperature is mostly a problem of process control. Lacking temperature control will let heat buildup on processing wafer, causing the drifting of the etching rate and surface profile. High temperature will also favor formation of SiO2 which may cause a similar case as lack of fluorine ions. Modern RIE system has helium backside cooling to assist in the temperature control. The plasma power will determine the bias between the grounded showerhead and the self-biased lower electrode which attracts the process ions. Higher power will induce stronger electric field and physical bombarding effect. Pressure affects the process in a similar mechanism. Molecules having longer mean free path under lower pressure accelerates for a longer period in the electric field. As a result, the ions will carry higher energy when bombarding the wafer. The optimal configurations of pressure, power and temperature could vary drastically with different designs and conditions of the process chamber. The following experiments will focus on methods to locate the optimal process windows of an unfamiliar RIE tool.

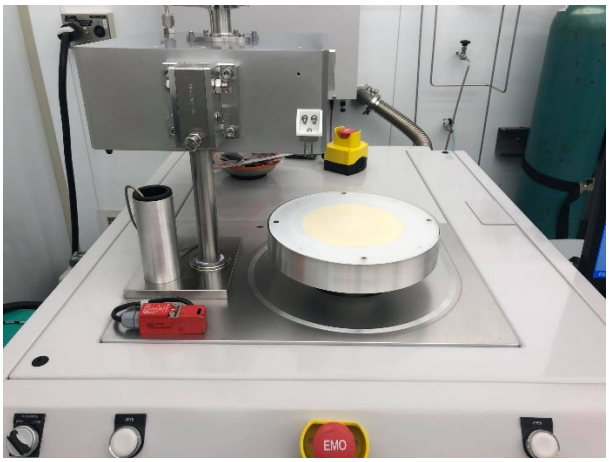


Fig. 2. Oxford PlasmaPro 80 RIE system with alumina carrier wafer installed on the lower electrode.

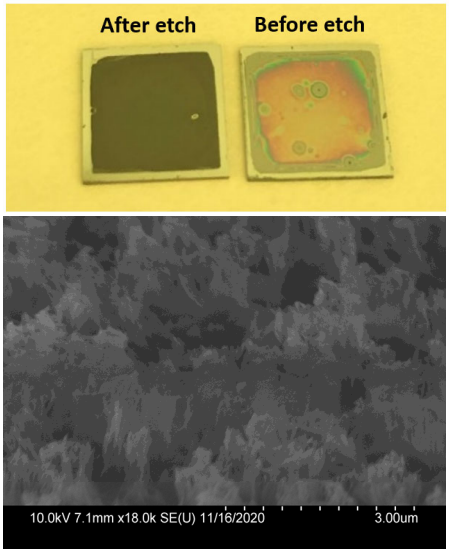


Fig. 3. (a) BCB sample before etching and after etching. (b) SEM picture of etched BCB surfaces with server roughness.

## Experimental Results & Analysis

Samples for experiments are prepared by spin coating BCB solvent (Dow CYCLOTENE™ 3022 series resins) on 1.2x1.2cm N-doped GaAs wafer pieces. The coated samples are then cured in oxygen free oven for three hours at 250 °C.

The solidified BCB thickness after cure is 3.1 µm. Etching experiments are carried out with Oxford PlasmaPro 80 RIE system as shown in Fig 2. while varying the setup and configurations. The RIE system is designed for whole wafer processing. For small wafer pieces in our case, 6-inch alumina wafers are initially chosen as the carrier wafer.

The experiments start with a recipe transferred from a different RIE tool. 10 sccm SF6 and 40 sccm O2 are used as the process gases. The RF power and pressure are set to be 60 W and 50 mT. The initial results are shown in Fig. 3. After a 2 µm BCB etch, the semi-transparent BCB thin film turns completely black, indicating a macroscopic roughness issue. In this case, MProbe can be used for quickly analysis. MProbe is a reflectance spectroscopy tool for thin film thickness measurement. A smooth thin film surface will reflect most of the light power back to the detector while a rough surface diffuses some of the light in random directions. A comparison is shown in Fig. 4(a) and 4(b). The light spot from an etched sample observable with naked eyes indicates beam diffusion from rough surfaces. The surface roughness can therefore be estimated based on the compression ratio of the measured spectrum as compared to the calculated results. An example is illustrated in Fig. 4(c) where the red measurement curve shows the measured spectrum, and the blue curve shows the theoretical calculations. The peak-to-peak amplitude can be used to characterize roughness while the alignment of peaks and valleys identifies the thin film thickness.

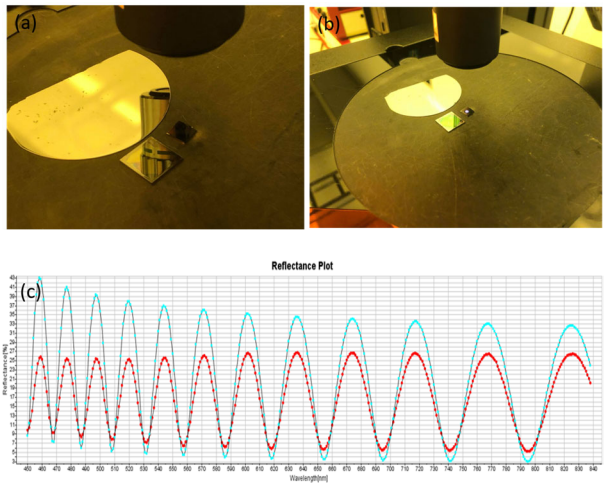


Fig. 4. (a) BCB surface before etching placed under light beam showing no light diffusion. (b) An etched BCB film diffuses light beam. (c) Measured reflectance spectrum of a thin film with rough surface.

The DOE experiments to improve surface condition starts from the tuning of RF power. After reducing the power from 60 W to 20 W, the etching surface condition improves significantly. The reflectance measurement can no longer detect any roughness. However, nano-scale residues remain if observing using scanning electron microscopy (SEM). The results are displayed in Fig. 5. The SEM picture focuses on the edge of a circular GaAs mesa structure resembling the case of a VCSEL device aperture. The mesa structure was originally covered with ~1 µm BCB. After etching to expose the circular mesa, dense residues are found on top of both the semiconductor and BCB surface. The residue size is measured to be 40-60 nm. Further reducing the RF power does not improve the residue condition which makes 20 W the optimized power setting.

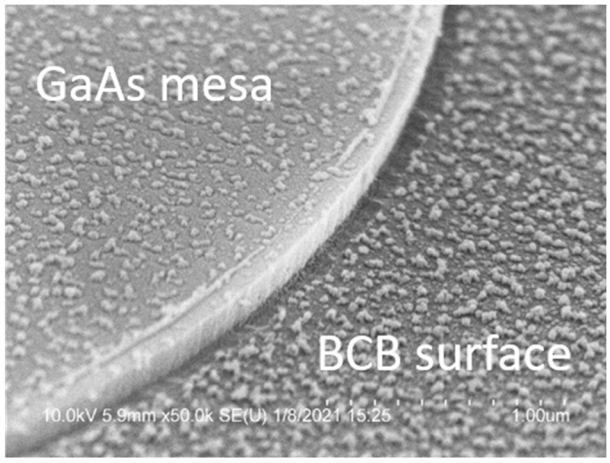


Fig. 5. Improvement from macroscopic roughness to nano-scale residues after reducing power from 60 W to 20 W.

We then start varying the chamber pressure while keeping the RF power constant at 20 W. 30 mT, 50 mT and 90 mT have been tried separately to etch 1.4 µm BCB. The results are observed with SEM and the residue scales are measured at 200K magnification. As shown in Fig. 6, 50 mT process produces dense 40-60 nm residues. Reducing the pressure to 30 mT will cause more sever intertwined residues while increasing the pressure to 90 mT reduces the residue sizes to 20-40 nm. The distribution of the residues is also sparser in comparison to the previous cases.

Since lower power and higher pressure both improves the surface condition, the roughness and residue are hypothesized to be caused by excessive physical sputtering. However, optimal RF power window has been determined and 90 mT pressure has reached the upper limit supported by the turbo pump. To further reduce the sputtering effect and residues, a 6-inch conducting silicon wafer is used in place of the insulating alumina wafer as the carrier. Small wafer pieces placed on top of insulating carrier may accumulate negative charges during process, resulting in higher local field and stronger sputtering effects. This is also supported by fact that the displayed DC bias increases from 33V to 44V with 20 W RF power after switching to the silicon carrier. It suggests the insulated process wafer surface potentially has a lower potential than the lower electrode. The expected improvement is displayed in Fig. 6 (d) where the particle size on BCB etching surfaces further reduces to < 20 nm.

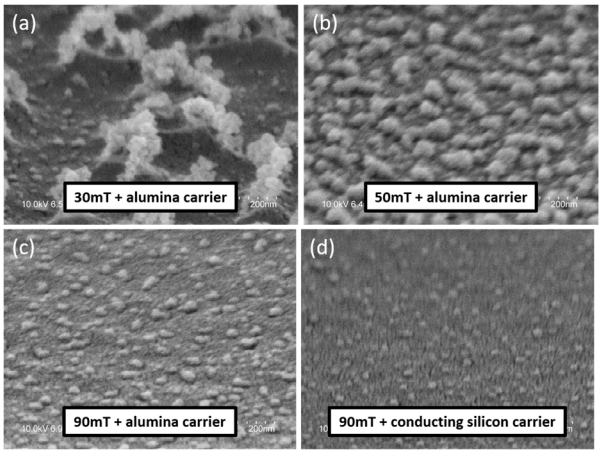


Fig. 6. (a)(b)(c) BCB surface under SEM at 200K magnification after 1.4 μm BCB etch down with 20 W RF power and pressure varying from 30 mT to 90 mT. Alumina wafer is used as the carrier (d) Improved surface condition after switching to a conducting silicon carrier.

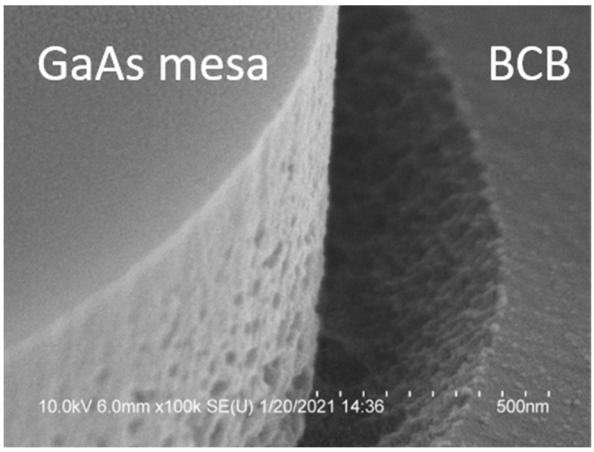


Fig. 7. Clean semiconductor mesa surface and smooth BCB surface after etching with optimized recipe.

The final optimized recipe is therefore set to be 20 W RF power, 90 mT pressure with conducting silicon wafer carrier. Gas ratio of SF6 to O2 is kept being 1:4. The mesa sample etching results are shown in Fig. 7. Compared to results in Fig. 5, a clean semiconductor surface and a smooth BCB surface are simultaneously achieved.

## CONCLUSIONS

A BCB RIE dry etching process is developed for high-speed VCSEL and PD fabrications. The theory of etching BCB is first explained and DOEs are discussed in detail to identify the optimal process window of an RIE system. The optimized recipe produces smooth etching surfaces with minimum residue.

## ACKNOWLEDGEMENTS

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## REFERENCE

[1] M. Liu, C. Y. Wang, M. Feng, and N. Holonyak, Jr. "Advanced development of 850 nm oxide-confined VCSELs with 57 Gb/s error-free data transmission," in Proc. GOMACTech, Mar. 2016.

[2] J. Qiu, H. L. Wang, C. Y. L. Wang, X. Yu, and M. Feng, "40 Gb/s VCSELs test data collection, analysis, and process problem identification," CS MANTECH 2017.

[3] M. R. Baklanov, S. Vanhaelemeersch, H. Bender, and K. Maex, "Effects of oxygen and fluorine on the dry etch characteristics of organic low-k dielectrics," AVS, 01-Mar-1999.

## ACRONYMS

VCSEL: Vertical Cavity Surface Emission Laser
BCB: Benzocyclobutene
SEM: Scanning Electron Microscopy

# Standing Wave Engineering for Mode Control in Single-Mode Oxide-Confined Vertical-Cavity Surface-Emitting Lasers

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**Keywords: Vertical-cavity surface-emitting lasers, single fundamental mode, anti-phase optical coating**

**Single transverse mode operation in vertical-cavity surface-emitting lasers (VCSELs) is desired over multimode operation in a number of applications. This work presents a method of achieving single-mode operation by depositing an annulus-shaped semiconductor coating atop an 850 nm oxide-confined VCSEL to modify the standing wave of the optical field in the laser cavity. The devices are benchmarked for single-mode performance as well as optical output power via optical spectra and light-current-voltage (L-I-V) measurements respectively.**

## INTRODUCTION

Due to the inherent properties of vertical-cavity surface-emitting lasers such as a circular beam shape, small footprint, and low manufacturing cost, VCSELs are becoming ubiquitous across several applications. This includes laser printing and optical mice to new and emerging applications in 3-D facial recognition, light detection and ranging (LIDAR), and short-haul optical communication systems utilizing pulse amplitude modulation (PAM-4). These emerging systems are also pushing existing VCSELs to their performance limits in terms of optical power and emission range over which single-mode operation is achieved. This necessitates the development of methods for ensuring single fundamental mode operation while maximizing power output. Standard methods of mode-control in VCSELs include surface-etch relief [1] and photonic crystals [2] which reduce the power reflectance of the top distributed Bragg-reflector (DBR) and in turn raise the threshold modal gain of the device, making it more difficult to lase. However, these methods face several challenges as they require extensive control over the dry etch process. Even with in-situ monitoring, etch uniformity can vary greatly over the surface of a wafer that makes etch depth difficult to control. Furthermore, any etch induced roughness can significantly degrade the reflectivity of the top DBR. To alleviate these issues, a semiconductor anti-phase coating is proposed. The finer control of deposition thickness and uniformity from modern PVD sputtering systems over dry etching techniques makes the semiconductor anti-phase coating more manufacturable and easier to implement for optical mode-control in VCSELs.

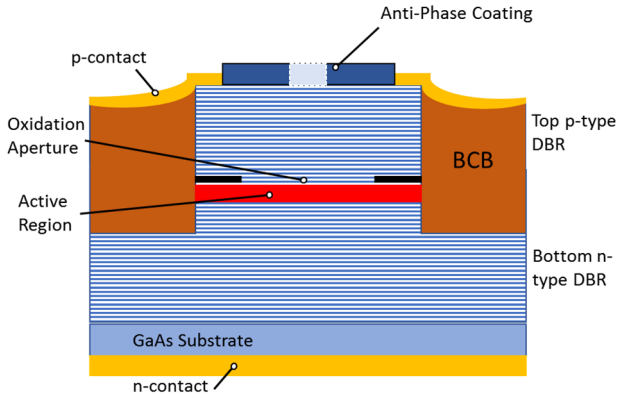


**Fig. 1** VCSEL cross-sectional schematic with anti-phase coating and oxide-confined active region. Anti-phase coating is in the shape of an annulus (hollow center, lighter blue).

## ANTI-PHASE COATING

The cross-section of a VCSEL with the anti-phase coating is shown in Fig. 1. The mechanism behind the effectiveness of the anti-phase coating is the spatial controllability of the threshold modal gain ($g_{th}$ in Eq. 1)

$$\Gamma g_{th} = \alpha_i - \frac{1}{2L}\ln(R_1 R_2) \qquad \text{(Eq. 1)}$$

across the top plane of the VCSEL. In Eq.1, $\alpha_i$ is the total intrinsic absorption loss in the material, $L$ is the length of the optical cavity, and $R_1$ and $R_2$ are the power reflectivities of the top and bottom DBR mirrors, respectively. The transverse mode profile of VCSEL consists of the fundamental mode (the desired lasing mode) lying in the center of the device while higher-order modes lie radially further away. By

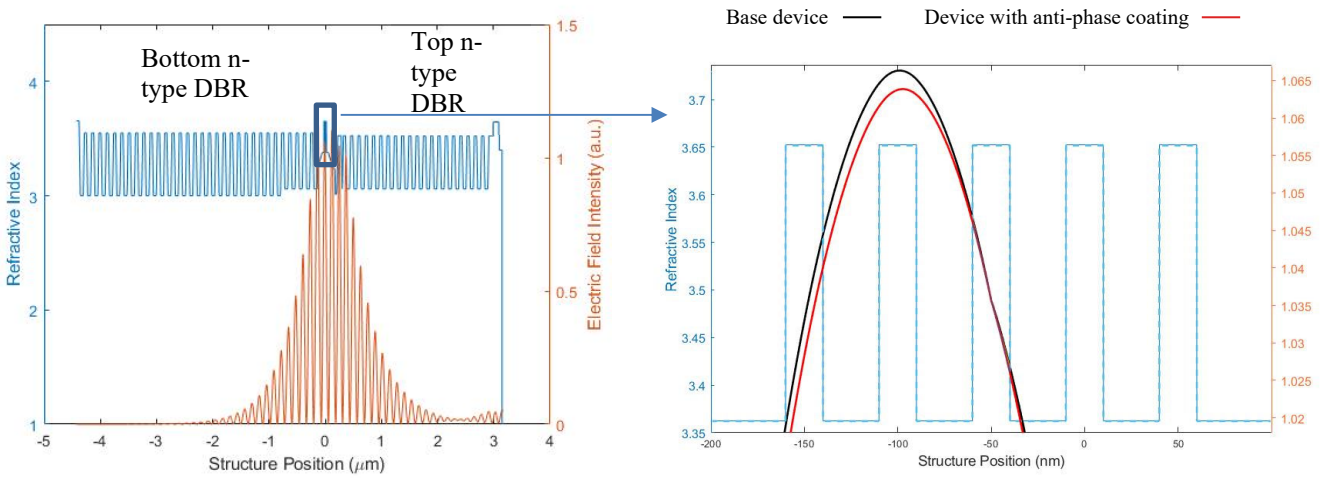


**Fig. 2** Standing wave pattern in a VCSEL superimposed with the refractive index of the structure. The wave pattern in the mode-controlled device (left) contains ripples near the surface and a shift in the wave pattern in the active region (right).

depositing a silicon thin film atop of the device, a phase mismatch is introduced into the electric field standing wave pattern. This shift misaligns the peak electric field with the quantum-wells in the gain region and leads to a reduced confinement factor and consequently increased threshold modal gain. If this is done only on the outer region of the device by depositing the silicon anti-phase coating in the shape of an annulus, fundamental mode operation can be ensured by suppressing the higher order modes and without significantly impacting the threshold modal gain of the fundamental mode. Previous work on VCSEL filters [4,5] were designed for VCSEL structures with incomplete top mirrors intended for inverted surface relief devices. This required a multilayered dielectric coating to account for and correct the incomplete mirror design. It was found that utilizing an epitaxial structure with a complete mirror allowed the design of a single layer rather than multiple that moreover achieves superior results. It was determined through threshold modal gain calculations that if a higher refractive index material, such as silicon, is used rather than a dielectric material, the phase mismatch in the top DBR can be maximized and create the greatest threshold modal gain difference between the center and the outer regions.

The electric field standing wave pattern of this VCSEL structure can be seen in Fig. 2, where the wave pattern is in orange and the index of refraction of the structure is in blue (surface of VCSEL is at 3 μm mark). When the anti-phase coating is added to the device (Fig. 2, left), the standing wave is shifted such that destructive interference occurs at the surface of the device and manifests as ripples due to the phase mismatch. This destructive interference reduces the field amplitude in the quantum well active region from 1.066 to 1.061 (Fig. 2, right), lowering the confinement factor and raising the threshold modal gain from 26 $cm^{-1}$ to 245 $cm^{-1}$. This effect can be seen in Fig. 3 (left), where the blue curve represents the GaAs cap layer that minimizes the threshold gain of the device (100 nm mark) and the red curve represents the Si layer that is maximized at the 150 nm mark. This determined the thickness of the Si annulus to be 50 nm in order to maximize the threshold gain for the higher order modes of the VCSEL. As mentioned earlier, Si was used over a dielectric material such as $TiO_2$ because of its higher refractive index and the advantages can be seen by comparing the graphs in Figure 3. The peak threshold modal gain achieved via a $TiO_2$ coating is 120 $cm^{-1}$ at a thickness of 80 nm, whereas the peak modal gain achieved via a Si coating increases in value by 104% to 245 $cm^{-1}$ at a thickness of 50 nm. By increasing this peak threshold modal gain value and designing the coating in the shape of an annulus, greater higher-order mode suppression can be obtained.

## DEVICE FABRICATION & CHARACTERIZATION

The epitaxial design of the VCSEL presented in this work was specifically designed for high power operation. The structure from top to bottom is follows: a 100 nm GaAs cap layer, 20 top p-type $Al_xGa_{1-x}As$ DBR pairs, 5 $In_xGa_{1-x}As$ quantum wells, 32 bottom n-type $Al_xGa_{1-x}As$/AlAs DBR pairs and an n-type GaAs substrate. A single high-aluminum content AlGaAs layer is inserted above the active region for selective oxidation during the fabrication process. The choice of InGaAs quantum-wells is designed to provide increased differential gain, $dg/dn$, compared to traditional AlGaAs quantum-wells. The insertion of binary AlAs into the bottom DBR allows for a higher thermal conductivity from the active region to the substrate. Fabrication of the VCSEL begins with depositing a PECVD $SiN_x$ film that is lithographically patterned to serve as a dielectric hard mask. The VCSEL mesas are then formed by using a $BCl_3/Cl_2/Ar$ ICP-RIE dry etch monitored in-situ by a laser interferometer. The devices are then loaded into a wet furnace at 430ºC to form the oxidation aperture. The diameter of the oxidation aperture is

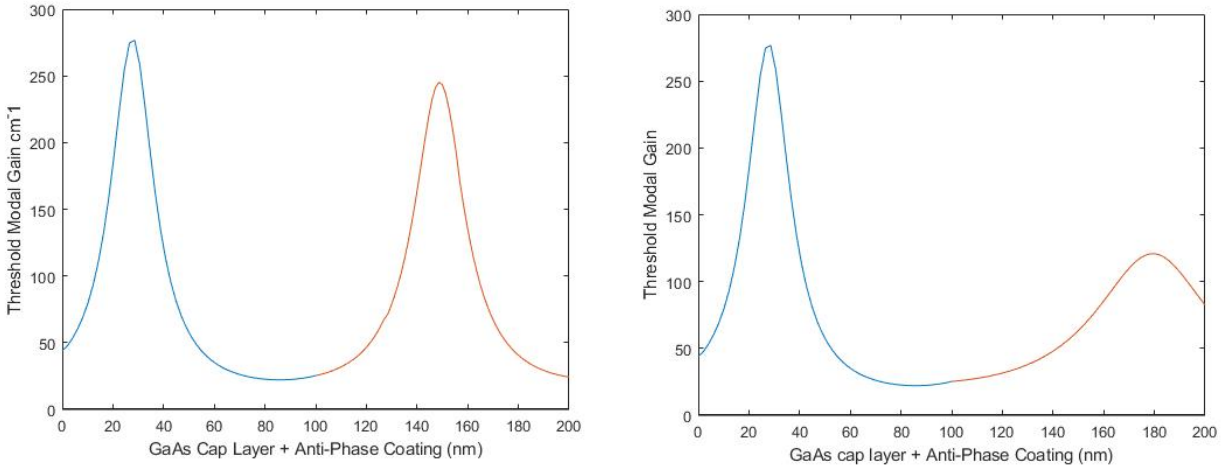


**Fig. 3** Threshold modal gain of VCSEL. Modal gain with GaAs cap layer (blue curve) is minimized at 100 nm and maximized with a Si coating at 50 nm (left graph, red curve) and with a $TiO_2$ coating at 80 nm (right graph, red curve).

verified through infrared imaging. Next, the devices are planarized and electrically isolated using spin-on curable polymer, benzocyclobutene (BCB). The BCB is then etched back to expose the VCSEL mesas and a BCB via etch is done to expose the bottom DBR. Afterwards a n-type ohmic metal stack consisting of AuGe/Ni/Au can be deposited via electron beam evaporation and patterned via a liftoff process. Following this a Ti/Pt/Au top side ohmic p-contact is formed using a similar process. Next, preliminary characterization data is taken to measure the threshold current, optical power, and spectra. Following this, the anti-phase coating is created by Si deposition via e-beam evaporation and photolithographic patterning. Finally, the VCSELs are recharacterized to measure single-mode operation and improvements in fundamental mode output power and optical spectra.

## CONCLUSION

Mode-control in oxide-confined VCSELs via an anti-phase filter enables single-mode operation, allowing for enhanced performance for emerging applications well-suited to VCSELs and their inherent properties over other lasers. By manipulating the shape of an anti-phase filter, this can be achieved by selectively lasing the fundamental mode while suppressing higher-order modes.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] Unold, Heiko J., et al. "Large-area single-mode VCSELs and the self-aligned surface relief." IEEE Journal of Selected Topics in Quantum Electronics 7.2 (2001): 386-392.

[2] Song, Dae-Sung, et al. "Single-fundamental-mode photonic-crystal vertical-cavity surface-emitting lasers." Applied Physics Letters 80.21 (2002): 3901-3903.

[3] Chuang, Shun Lien. *Physics of photonic devices*. Vol. 80. John Wiley & Sons, 2012.

[4] Kesler, Benjamin, Thomas O'brien, and John M. Dallesasse. "Transverse mode control in proton-implanted and oxide-confined VCSELs via patterned dielectric anti-phase filters." Vertical-Cavity Surface-Emitting Lasers XXI. Vol. 10122. International Society for Optics and Photonics, 2017.

[5] Kesler, Benjamin A. Mode control in VCSELs using patterned dielectric anti-phase filters. Diss. University of Illinois at Urbana-Champaign, 2017.

## ACRONYMS

VCSEL: Vertical-Cavity Surface-Emitting Laser
DBR: Distributed Bragg Reflector

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