Improving Root Cause Analysis Accuracy Using Advanced Sensor Trace Analytics

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Abstract

One of the key responsibilities for engineers working in a semiconductor fab is to resolve wafer yield issues for improving and maintaining production yield. The traditional approach in root cause analysis requires multiple software tools, multiple steps, and multiple domain resources. The amount of time to solve a wafer yield issue could require days or weeks. To address this, engineers have started leveraging advanced data analytic software solutions to gain better insights and to help expedite the root cause analysis process. In this paper, the advantages of using a trace analytics software tool for root cause analysis is illustrated through an actual use case.

BACKGROUND

Wafer yield loss events are costly to a fab operation. Depending on the severity of the yield loss, revenue impact could potentially be hundreds of thousands to millions of dollars, depending on the product. Therefore, it is extremely critical for the engineers to find root causes of yield-impacting issues and remedy these situations as quickly as possible. Unfortunately, wafer defect signals do not always provide a clear indicator for the engineer to easily identify the root cause. The traditional root cause analysis process is very time consuming and requires deep domain knowledge of the process. The lengthy time-to-root-cause-identification does not only prolong production of poor-quality products, it directly affects the manufacturer's bottom line.

WAFER EDGE LOW YIELD CASE STUDY

In this case study, the manufacturer experienced unusually high yield loss in three wafer lots. Over 30% of the wafers suffered from low yield patches at the 5 and 11 o'clock positions on the wafer edge. Yield loss was up to 11% on each affected wafer (see Fig. #1).

THE INITIAL INVESTIGATION

In the first step of analysis, chamber commonality was performed using an existing YMS analytic software tool. The software tool analyzed the process data against the yield patterns and suggested that the issue was isolated to a process step in the left chamber of an etch tool. In Fig. #2, fallout

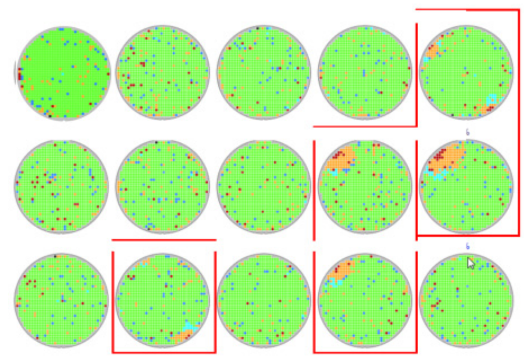

Fig. #1 – Examples of Wafer Edge Patch Defect Pattern at 5 and 11 o'clock positions

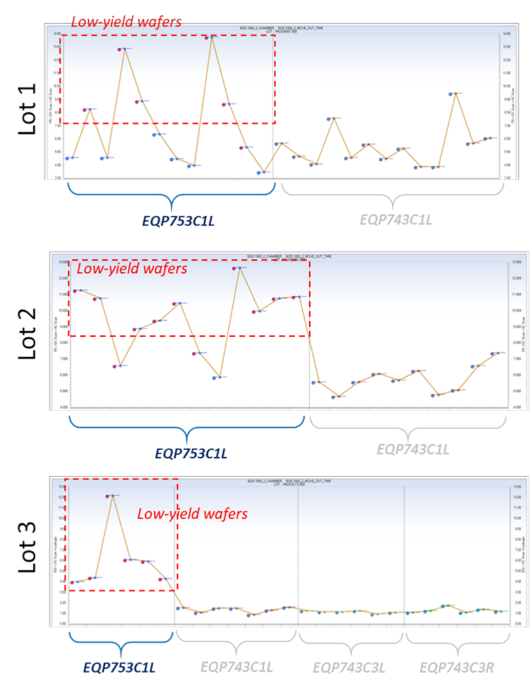

Fig. #2 – As shown in the Power Short/DC Scan fallout chart, partitioned by tool/chamber, all low-yield wafers were processed through the same etch tool and chamber charts from the YMS software show that all low-yield wafers with this specific yield pattern were processed through the same chamber of the same tool (Left chamber 1 of etch tool 753).

Further correlation analysis using the available inline quality data (Defect Inspection, Metrology, and Electrical Test) against the yield data was also manually performed, but no additional insights were found. However, through domain experience, the engineer recognized this failure mode to be similar to a past issue related to a defective Electrostatic Chuck (ESC) which had created an arcing issue. The issue caused improper de-chucking of wafers resulting in similar defects on the edges of the affected wafers.

VALIDATION OF INITIAL ASSESSMENT

In attempt to confirm the suspicion of an arcing issue, a comprehensive failure analysis (FA) was performed on one of the affected wafers. The FA process included the following steps and findings:

1) Electrical analysis on a failed die to validate leakage with IV curve against a good die – Result: significantly high leakage was observed

2) EMMI emission fault isolation to localize the defect location within the die – Result: Failure hot spots identified

3) Physical deconstruction of the affected die down to the contact layer – Result: No anomalies observed on the metal layers

4) AFP nanoprobing analysis on "transistor" level – Result: Confirmed Poly to N+ leakage at EMMI hot spot locations (see Fig. #3)

5) High Beam Contrast inspection to confirm leaky poly – Result: No anomalies observed

6) Cross-sectional TEM examination of the leaky poly – Result: Identified silicide migration towards gate oxide (see Fig. #4)

Silicide migration is a symptom of Electrical Overstress (EOS) which could suggest arcing during the manufacturing process. With this information, the engineer became more confident in the hypothesis.

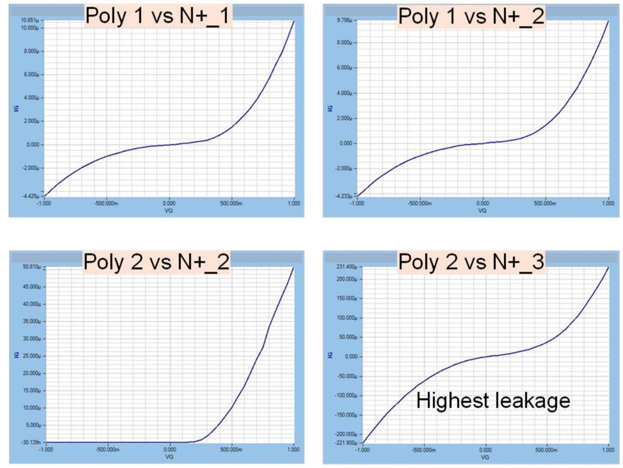

Fig. #3 – AFP analysis confirmed poly to N+ leakage at EMMI hot spot location

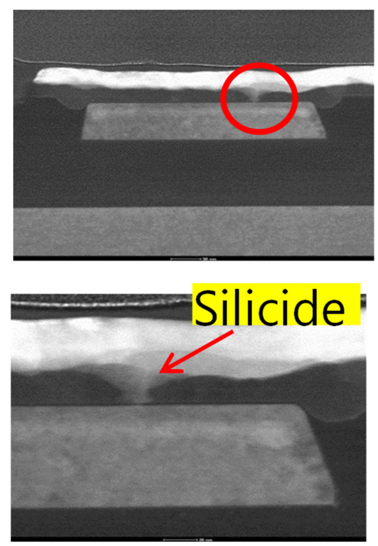

Fig. #4 – XTEM analysis clearly showed the presence of silicide migration which is a common symptom of an Electrical Overstress (EOS) issue

ROOT CAUSE ANALYSIS

Even though the preliminary investigation helped to narrow the issue down to the offending process step, tool, and chamber, the engineer must pinpoint the root cause, so the appropriate corrective actions can be taken to prevent future occurrences. Understanding that a more in-depth analysis could be a long and challenging process using the traditional root cause analysis approach, the engineer elected to leverage a data analytic software solution to aid with root cause analysis and expediting the process. The software solution chosen has the capability to pull in all relevant data types (process, yield, metrology, etc.) and to automatically perform comprehensive analysis of all data down to the recipe step level using trace analytics. This allows the engineer to get accurate parameter-level root cause results in a fraction of the time required if the process were to be done manually.

Traditional Root Cause Analysis

A traditional approach in root cause analysis requires manual manipulation and examination of all process sensor data to find abnormalities during the manufacturing process. This could be a daunting task, even in cases where the issue has been isolated to a specific chamber and process step. Depending on the issue, multiple engineering teams (yield, equipment, and process engineering) will likely need to be involved to perform a deep dive analysis based on their respective domain expertise. In many cases, because of the volume and complexity of the data, engineers would only focus on critical parameters to reduce the scope of the task. This could potentially result in mis-detection, particularly in cases where the issue is subtle or hidden. Due to the laborious nature of this approach, the time to identify root cause could take days to weeks.

Root Cause Analysis Using Trace Analytics

Leveraging a trace analytic software solution for root cause analysis provides several advantages. First, the solution helps in simplifying the process of pulling in all parameter types including process, quality, and test data, eliminating a laborious step of gathering and managing data manually. Once the data is gathered, the solution can automatically analyze and correlate all relevant data to quickly identify abnormalities that might contribute to yield loss. Because the solution examines full sensor traces, all subtle issues (i.e.: drifts, spikes, ramp rate changes, etc.) can be detected, big or small. These subtle signals are often missed by analysis using summary data or manual examination of the trace data (see Fig. 5). Since the trace analysis is performed on the full trace, the solution can accurately pinpoint the issue down to the recipe step level. The complete analysis can be done by a single engineer, eliminating the need to get multiple teams involved in the process. When using a trace analytic software solution, time-to-root-cause is shortened from days/weeks to minutes/hours.

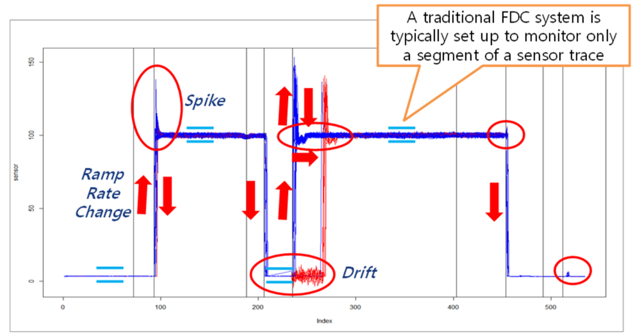

Fig. #5 – Trace Analytics captures all subtle details of a trace to comprehensively detect issues

The Result

With the help of the trace analytic software solution, the engineer was able to effortlessly analyze all sensor traces and identified a list of potential candidates (at the parameter level) as possible root causes within minutes. After examining some of the top candidates, the engineer identified the Helium (He) Leakage parameter to be the main root cause indicator of the problem. This parameter measures the level of Helium that is present between the wafer and the Electrostatic Chuck (ESC) platform. The engineer noticed that the measurements of this specific parameter from the low yield wafers were consistently lower than those from the high yield wafers during the last step of the etch process (see Fig #6). This indicates the wafers were not properly decoupled from the ESC platform at the end of the etch process which likely resulted in Plasma Induced Defects (see Fig #7).

In addition, upon closer examination of the rest of the potential root cause candidates, the engineer discovered another parameter (an unmonitored parameter by FDC) with indicators which correlated strongly with the low-yield wafers. This parameter specifically measures the ESC Current Leakage, and the data from the low-yield wafers all showed a subtle spike at the end of the trace which indicates abnormalities at the end of the etch process (see Fig. #8). Under normal operation, this parameter should remain at zero at the end of the etch process. This subtle spike confirms the arcing suspicion supported by the early findings.

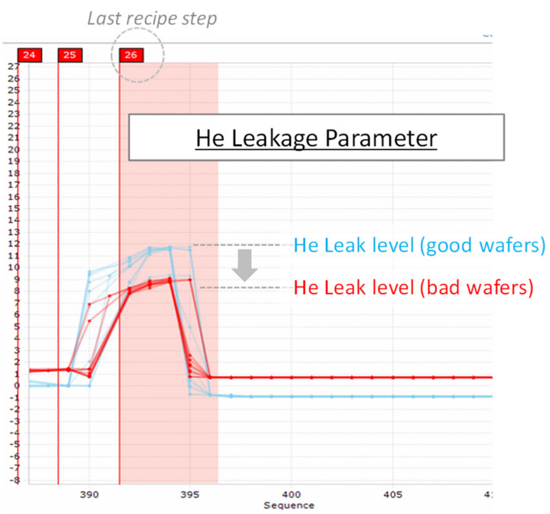

Fig. #6 – Trace Analytic software shows that Helium Leakage level at the last recipe step to be lower for low-yield wafers

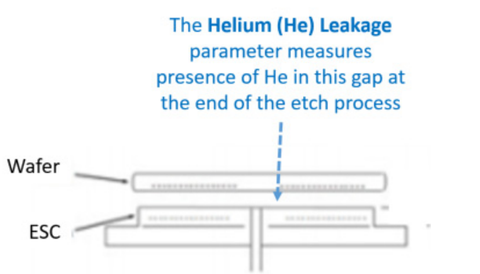

Fig. #7 – Low He Leakage detection signals improper de-chucking which could cause Plasma Induced Defects (PID)

Fig. #8 – The ESC Current Leakage data also supported the suspicion of an arcing issue

With the confirmed root cause of a problematic ESC, the failed unit was replaced to correct the issue. More importantly, both parameters are now included as part of the critical parameter list in FDC for monitoring, which should prevent the re-occurrence of the same issue.

CONCLUSION

By utilizing a trace analytics software solution, the engineer was able to quickly and accurately pinpoint the root cause of the yield loss at the wafer edge. The shortened time for performing root cause analysis enabled timely corrective actions and minimized further yield loss. In addition, the solution empowers the engineer to include a parameter which was previously unmonitored into the list of monitored critical parameters in FDC. Lastly, with a tool that can automatically pull in and analyze all available sensor trace data in one place without the involvement of additional engineering resources (i.e.: the equipment or the process engineer), the root cause analysis process was greatly simplified, resulting in increased productivity for all teams involved.