Demonstration of GaN-on-silicon material system operating up to 3 kilovolts with reduced trapping effects

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Keywords: GaN power devices, trapping, high voltage

We report on the first demonstration of low trapping effects up to 3000 V within GaN-on-silicon epitaxial layers using a local substrate removal (LSR) followed by a thick backside ultra-wide-bandgap AlN deposition. The fabricated AlGaN/GaN devices deliver low specific on-resistance below 10 mΩcm^2 together with unprecedented 3-terminal blocking voltage while substrate ramp measurements show reduced hysteresis up to 3000 V. These results pave the way for beyond 1200 V applications using large wafer diameter GaN-on-Si high electron mobility transistors.

INTRODUCTION

GaN-on-Silicon high electron mobility transistors (HEMTs) offer the potential to revolutionize power electronics by enabling important energy savings and new flexibility for advanced power circuits [1]. However, GaN-on-Si transistors suffer from poor critical electrical field strength of the Si substrate together with a parasitic conduction at the buffer/substrate interface leading to device breakdown [2]. That is why, applications requiring voltage operation of 1200 V and above cannot currently be covered by GaN-on-Si HEMTs, although thicker buffers with high associated material quality have been developed [3].

A solution to suppress the parasitic conduction phenomenon and thus enhance the breakdown voltage (BV) is to remove the Si substrate, which was proposed in 2010 [4, 5]. Indeed, the Si substrate removal around the drain electrode enabled electrical isolation of the gate and source contacts from the drain across the buffer layer/Si interface. Using this approach, we reported GaN-on-Si based transistors with a significantly improved blocking voltage of 3000 V [6]. Recently, we have demonstrated GaN-on-Si metal insulator semiconductor HEMTs (MISHEMTs) with LSR under the entire device followed by a backside deposition of the ultra-wide bandgap AlN material [7]. The use of an in-situ SiN gate dielectric under the gate and local substrate removal (LSR) technique combined with 15 µm thick AlN layer enabled state-of-the-art GaN based HEMTs with remarkably low off-state leakage current (<1 µA/mm) up to 3000 V. On the other hand, a key figure of merit for GaN power devices is the current collapse that hindered for instance the commercialization of 650V-rated GaN-on-Si devices.

In this work, we demonstrate for the first time the possibility to benefit from low electron trapping up to 3000 V on lateral GaN-on-Si based transistors while delivering excellent electrical characteristics. The results are attributed to the improvement of the epitaxial stack quality associated to an optimized LSR technique filled in with physical vapor deposited (PVD) low temperature AlN. This indicates that beyond the drastic blocking voltage improvement provided by the LSR approach, no trade-off in terms of current collapse is observed up to 3000 V and most probably above.

DEVICE FABRICATION

The AlGaN/GaN heterostructure has been grown (Enkris Semiconductor, Inc.) by metalorganic chemical vapor deposition (MOCVD) on a 6-inch Si (111) substrate. The HEMT structure consists in a 5 µm buffer thickness, a 310 nm undoped GaN channel followed by a 24 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and an 11 nm in situ Si_3N_4 cap layer (Fig. 1). Ohmic contacts were formed directly on top of the AlGaN barrier by alloying Ti/Al/Ni/Au stack using an 875°C rapid thermal annealing resulting in contact resistances of 0.3 Ω.mm. Device isolation was achieved by N_2 implantation. Hall measurements reveal a sheet carrier concentration of 0.9×10^{13} cm^{-2} with a mobility of 2100 cm^2/Vs, and a sheet resistivity of 330 Ω/□. Metal-insulator-semiconductor (MIS) gate structure was employed by depositing Ni/Au metal stack inside the in-situ Si_3N_4 cap layer without any additional field-plate. A 200-nm thick SiN film was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) as extra passivation. Once the front-side processing was completed, the Si substrate was locally etched up to the AlN nucleation layer around the entire device, as shown in Fig. 2. It is important to note that our mask design consists of devices with and without LSR patterns, which eliminates any processing or epi variation during the device characterization (Fig. 2). Then, 15 µm thick AlN was deposited on the backside by PVD at 300°C. The AlN film delivers a high breakdown field well-above 4 MV/cm despite the low temperature deposition as check through vertical measurements on reference doped silicon wafers. Finally, 2 µm of Cu is deposited. Hall measurements

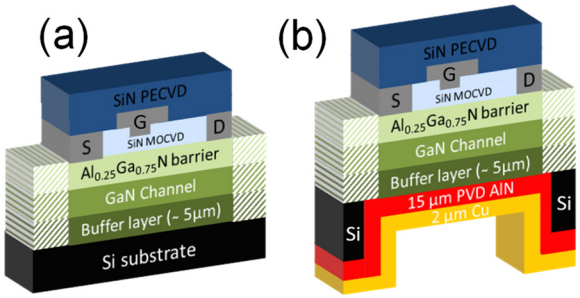

Fig. 1. Schematic cross-section of AlGaN/GaN MISHEMT after (a) the front side process, (b) the LSR technique + 15µm thick PVD AlN deposition, and 2µm Cu deposition on the back-side

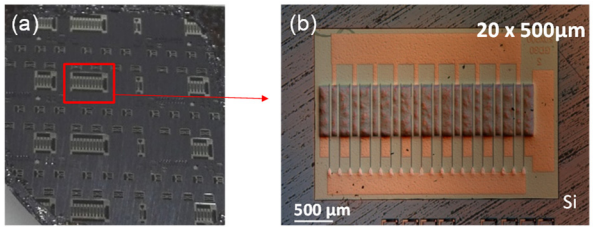

Fig. 2. Optical back-side image of (a) the wafer with and without LSR removal patterns, (b) 20×500µm AlGaN/GaN MISHEMT after LSR

remains identical after full backside processing and subsequent AlN and metal depositions.

Results and Discussions

As expected, the vertical leakage current measurements conducted on isolated patterns with LSR show a remarkable increase from 1000 V to above 3000 V (limitation of our set-up) as compared to patterns without LSR (Fig. 3). This confirms the suppression of the substrate conduction

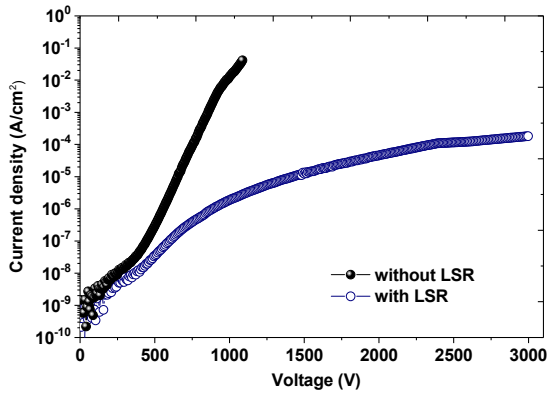

Fig. 3. Room temperature vertical leakage characteristics of the AlGaN/GaN epitaxial structure with and without LSR

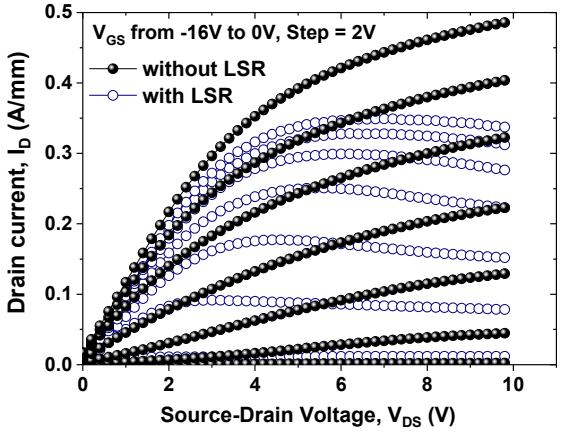

Fig. 4. I_D-V_{DS} characteristics of AlGaN/GaN MISHEMTs (L_{GD} of 5 µm) with and without LSR

phenomena and effectiveness of the AlN dielectric thick film.

DC characterizations were carried out on devices with gate width/length = 50 µm / 2 µm and various gate-to-drain spacing (L_{GD}) with and without LSR on the same wafer. Maximum current density at V_{DS}=4V and V_{GS}=0V decreased from 350 to 315 mA/mm after the Si substrate removal under the active region due to self-heating (Fig. 4). It can be pointed out that a significant recovery of the maximum current density occurs after the Cu deposition, which in turn enables to reduce the self-heating. Consequently, a thicker Cu heat sink (> 10 µm) is expected to mitigate the current density reduction. Nevertheless, the extracted static specific on-resistance ($R_{ON\text{-}STATIC}$) values are found to be rather close with for instance 8.5 against 8.7 mΩ/cm² for devices with L_{GD} = 30 µm, without and with LSR, respectively (Fig. 5). The corresponding transfer characteristics of AlGaN/GaN MISHEMTs with L_{GD} of 5 µm are shown in Fig. 6. Despite a slight shift of the threshold voltage, it appears that the off-state leakage currents with and without LSR are similar and well-below 0.1 µA/mm at low drain bias.

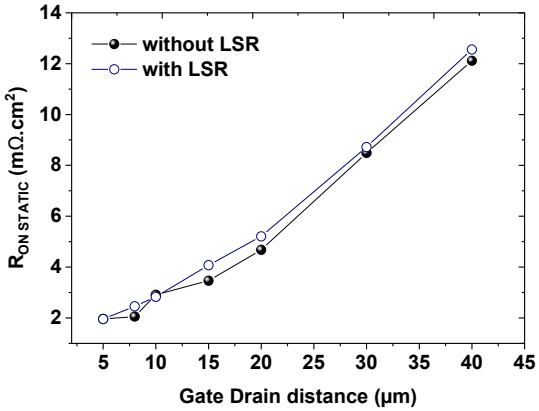

Fig. 5. Specific DC on-resistance of AlGaN/GaN MISHEMTs as a function of the gate-drain distance with and without LSR

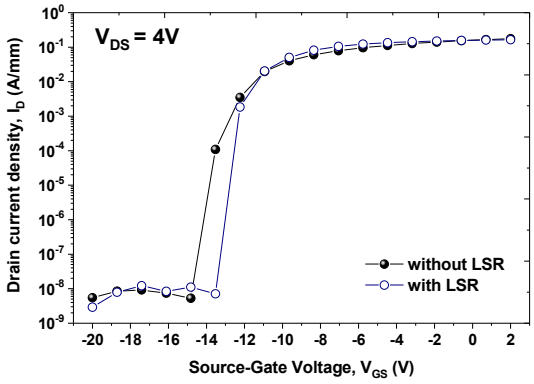

Fig. 6. DC transfer characteristics of AlGaN/GaN MISHEMTs (L_{GD} of 5 µm) with and without LSR

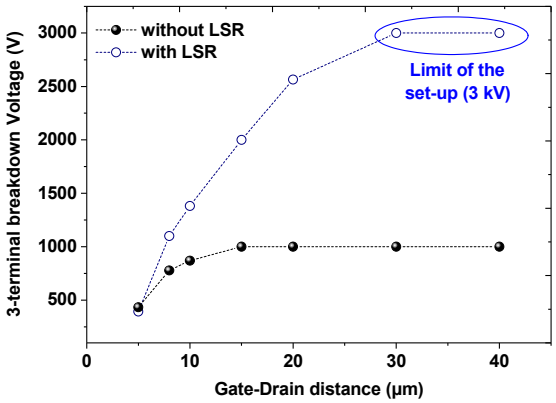

Fig. 7. Evolution of L_{GD}-dependent 3-terminal breakdown voltage of AlGaN/GaN MISHEMTs with and without LSR

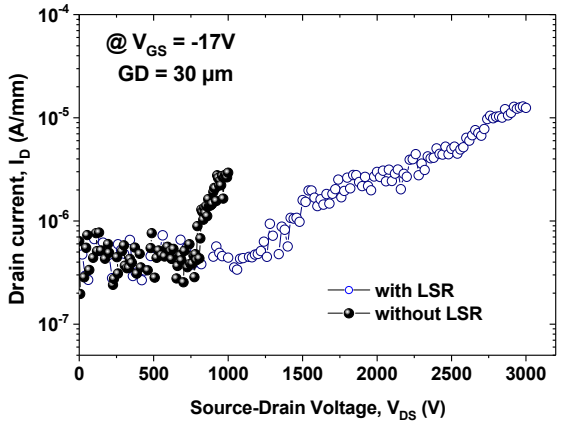

Fig. 8. Room temperature off-state leakage current characteristics of AlGaN/GaN MISHEMTs (L_{GD} of 30 µm) with and without LSR

The three-terminal off-state leakage characteristics of the AlGaN/GaN MISHEMTs are plotted as a function of L_{GD} in Fig. 7. The one with a large design (L_{GD} = 30 µm) appears in Fig. 8. The devices without LSR show a BV plateau around 1000 V due to the buffer thickness limitation. For devices with LSR, the BV versus gate-drain distance increases almost linearly reaching more than 3000 V for large designs (L_{GD} > 30 µm). In the same way, lateral breakdown voltage conducted on isolated patterns as a function of the contact distance with and without LSR show an outstanding improvement from 1900 V to well above 3000 V with a

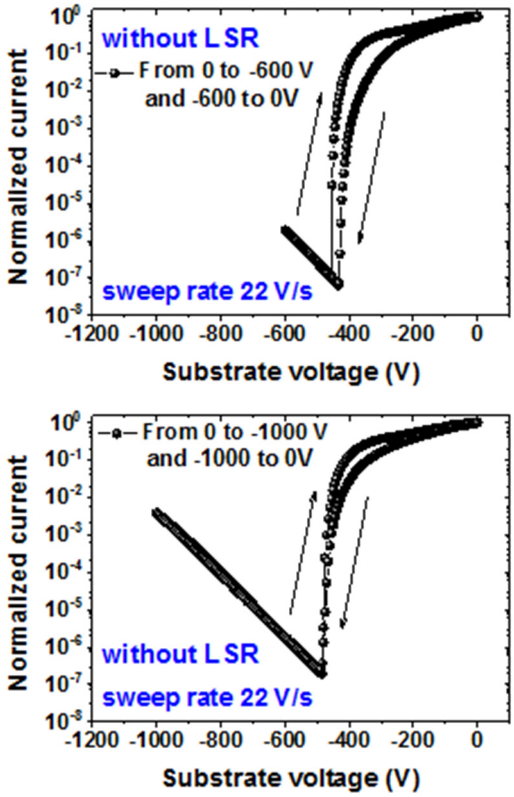

Fig. 9. Substrate ramps at 600 V and 1000 V for the AlGaN/GaN epitaxial structure without LSR

reduction of the leakage current, confirming the suppression of the substrate conductive path contribution.

The substrate bias ramp technique has been shown to be very efficient in order to highlight the trapping effects and related current collapse in GaN-on-Si power switching transistors [8]. As a matter of fact, in properly passivated structures, buffer charge storage is the main source of dynamic on-resistance [9-11]. Substrate bias measurements have been performed on a Keysight B1505A Power Device Analyzer. Two Ohmic contacts with a spacing of 20 µm have been used and the bias is set at 1 V. By ramping the substrate to a high (negative) potential, mimicking the off-state operation under the drain contact in a transistor, any charge redistribution in the buffer upon reverse bias will change the electric field. As such, the buffer charge trapping

or storage will be visible in the substrate ramp characteristic. This approach is surface insensitive and applies a 1-D vertical field. The sweep rate was set to 22 V/s. The devices without LSR reveals low hysteresis in the various ramps (Fig. 9) performed up to 1000 V (close to the breakdown voltage). This reflects the excellent material quality and the low charge storage within the heterostructure. Interestingly, the devices with LSR also show low hysteresis and thus reduced charge storage all the way to 3000 V (Fig. 10). This means that the substrate removal followed by the additional thick AlN deposition do not induce charge trapping. The integrity of a trap-free buffer is thus not affected by the substrate removal approach while extended significantly the bias operation capability.

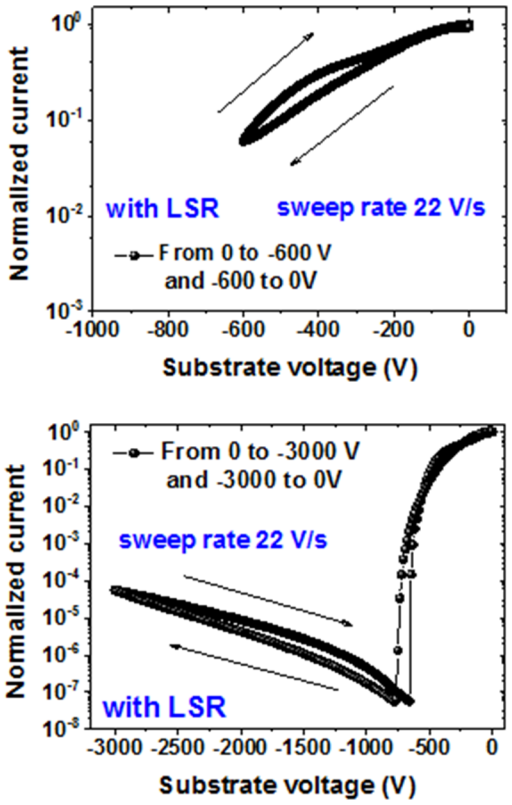

Fig. 10. Substrate ramps at 600 V and 3000 V for the AlGaN/GaN epitaxial structure with LSR

Conclusions

This work demonstrates for the first time that the substrate removal approach not only enable to extend drastically the operation voltage capabilities of GaN-on-Silicon HEMTs to 1200 V and above with low R_{ON} but also does not induce additional trapping affecting the dynamic behavior of power switching transistors. The thermal penalty resulting from the silicon removal can be largely overcome by implementing a proper heat sink. The process is applicable to large devices (delivering > 20 A) and therefore highly manufacturable. These results show that power applications above 1000 V covered currently by SiC and silicon based devices could benefit from the high electron mobility offered by GaN-on-silicon heterostructures enabling much lower R_{ON}.

Acknowledgements

This work is supported by the French RENATECH network and ANR project DESTINEE (ANR-16-CE05-0022). This project has partly received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 720527 (Inrel-NPower). The authors would also like to acknowledge the company Kyma for the thick PVD AlN deposition.

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