Process Development Enabling Lateral GaN JFET Devices for Robust Power Switching on 200 mm Engineered Substrates

Travis J. Anderson[1], James C. Gallagher[2], Geoffrey M. Foster[2], Andrew D. Koehler[1], Marko J. Tadjer[1], Ozgur Aktas[3], Vladimir Odnoblyudov[3], Cem Basceri[3], Karl D. Hobart[1]

[1]U.S. Naval Research Laboratory, Washington DC 20375, United States, travis.anderson@nrl.navy.mil
[2]American Society for Engineering Education, Washington, DC (post-doc residing at NRL)
[3]Qromis, Inc., Santa Clara, CA

Keywords: GaN, JFET, power switch, avalanche breakdown, engineered substrate

Abstract

Lateral GaN-based p-n junction gated field effect transistor (LJFET) devices on large area substrates were evaluated as candidate power switching devices. An advantage of this device over commercial high electron mobility transistor (HEMT) switches is the potential for avalanche capability with proper design, enabling robust power switching. The maximum current density was 200 mA/mm and threshold voltage was -30V. Large gate width devices (40mm) exhibited >1A current. The devices have blocking capability to 800V and low dynamic R_{ON}.

Introduction

GaN-based power switching devices are of significant interest for high efficiency power conversion circuits in medium voltage applications. However, widespread adoption is limited as commercial enhancement mode high electron mobility transistors (HEMTs) are limited in voltage capability and do not exhibit avalanche capability for robust operation, and high performance vertical devices are still experimental with relatively high manufacturing cost due the small wafer diameter [1-5]. Recently, Qromis, Inc. has developed commercial substrates designated QST™ that are engineered to be thermally matched to GaN, enabling thick epitaxial layers of comparable quality to HVPE GaN suitable for a >1kV class of devices. QST™ substrate comprises a core CTE-matched to GaN, a series of thin films encapsulating the core, and an epi-ready Si (111) surface for GaN epi. As the technology is easily scalable to 200 mm diameter wafers with low bow and standard thickness, the technology is suitable for fabrication in a CMOS facility [6].

In this work we present a GaN-based lateral junction gate field effect transistor (LJFET) device structure for power switching applications. This type of device has previously been evaluated for RF applications, but it presents a unique advantage as a robust power switch [7]. The p-GaN gate functions to collect secondary holes while a second buried p-GaN blocking layer is implemented to pull the electric field below the surface as in a reduced surface field (RESURF) structure, enabling the potential for a lateral GaN device with improved reliability and avalanche-capability which may enable GaN devices in the > 1200V range and, with further analysis, provide insights to improve the reliability of GaN HEMT based switches [8]. In this work we present the analysis of a prototype device with high current density, low dynamic ON-resistance (R_{ON}), and high breakdown voltage utilizing a foundry-compatible processes.

Experimental Procedure

The device structure was grown by metal organic chemical vapor deposition (MOCVD) on standard thickness (725 µm) 200mm QST™ wafers using a commercial vendor. Following typical nucleation processes, the layer structure consisted of a 6µm semi-insulating GaN buffer layer formed by carbon compensation, a 1200nm n- GaN channel layer ($4x10^{16}$ cm^{-3}), a p- GaN ($1x10^{18}$ cm^{-3}) layer for electric field control, a p+ GaN layer ($1x10^{19}$ cm^{-3}) for gate control, and a thin heavily doped p++ GaN layer (>$1x19^{19}$ cm^{-3}) to facilitate ohmic contact. LJFET devices with 3µm gate length, 100µm-40mm gate width, and 15µm gate-drain gap were fabricated on these structures. As the device layout was annular, no mesa isolation was required. The device fabrication process consisted of an etch to expose the buried channel layer using Cl_2-based inductively coupled plasma (ICP), followed by ohmic metal on the source/drain regions (Ti/Al/Ni/Au alloyed at 800 °C in N_2). The gate metal was a non-alloyed Pd/Au deposited by e-beam evaporation and lift-off, and then a second Cl_2 ICP etch was used to remove the p+ GaN layer in the access regions. A cross section of the device is shown in Figure 1.

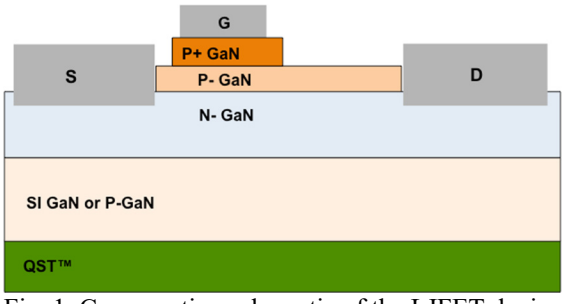

Fig. 1. Cross section schematic of the LJFET device

RESULTS AND DISCUSSION

Following device fabrication, the channel layer was characterized by measurements of a circular transmission line method (CTLM) structure. The device structure was characterized by C-V on a quasi-vertical diode, and the FET devices were characterized for DC I-V behavior, blocking capability, and dynamic R_{ON}. The design space has been previously evaluated to identify the proper channel thickness and doping range to achieve high current density while preserving the ability to modulate the channel [9]. In the optimized device reported here, excellent current density values of 180 mA/mm were observed, as shown in Figure 2. The threshold voltage (V_T) is highly negative (-27V) as targeted by device design goals. The OFF-state leakage was low and largely dominated by gate current.

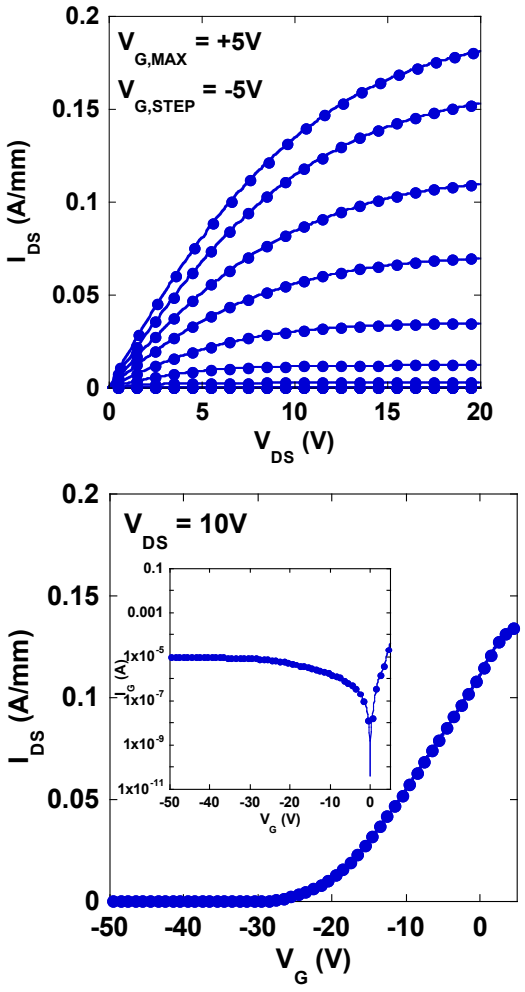

Fig. 2. Output characteristics (I_{DS}-V_{DS}) and FET transfer characteristics of the LJFET device. Gate leakage is shown as inset.

The FET breakdown voltage was evaluated using three terminal forward blocking measurements with fluorinert, shown in Figure 3. The breakdown measurements were performed on small annular devices with 340µm gate width in order to manage leakage current at high voltage. The devices were held in the OFF-state at V_T-5V while the drain voltage was increased at a rate of 10V/s. Multiple devices were tested to study repeatability across the sample. All three devices shown had a breakdown voltage ranging from 750-800V while maintaining low leakage current up to the breakdown point. Note that the breakdown behavior was catastrophic, which is to be expected as the current design utilizes a semi-insulating buffer rather than the p-GaN RESURF structure previously described.

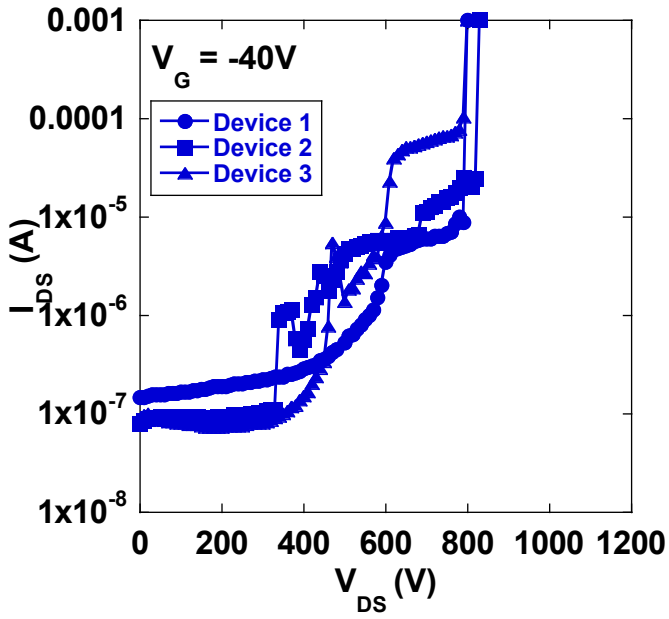

Fig. 3. Forward blocking measurements

Capacitance-voltage profiling of the epi-structure was performed using quasi-vertical p-n diode test diodes with 290 um diameter. As can be seen from Figure 4, the channel doping density is consistent with design specifications and the depth of the non-depleted channel indicates that the C-doped buffer is resulting in depletion of the channel from the bottom as is required for proper channel pinch-off and cut-off. At the same time, from this analysis it becomes clear that an electrical contact (ground) needs to be provided to back-side to avoid uncontrollable charging effects. In a next generation of this device the C-doped buffer will be replaced by a p-GaN buffer and a p+ GaN back-contact providing a low-resistance back-gate which will eliminate the charging effects as well as provide a built-in body diode which will support internal clamping.

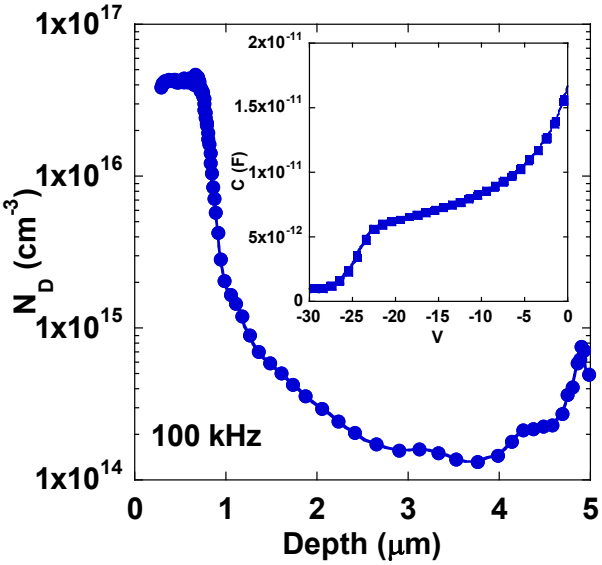

Fig. 4. Extracted doping profile from C-V analysis. Raw C-V curve is shown as inset.

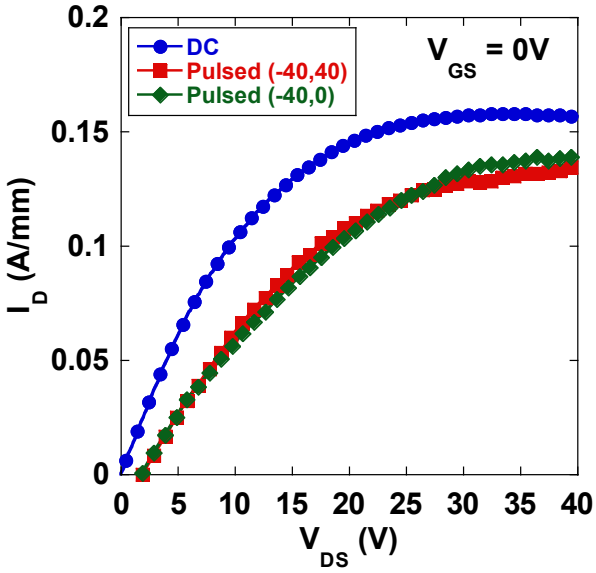

Fig. 5. Pulsed vs static I-V curve at varying pulse conditions

The static and dynamic characteristics of a 100 μm wide GaN LJFETs were characterized using a Keithley 4200-SCS semiconductor parameter analyzer with 4225-PMU ultra-fast pulse measurement unit with a 4225-RPM remote preamplifier/switch module. The quiescent state is held for one second and then pulsed measurements occur over a pulse width of 500μs with a 0.5μs rise and fall time. As shown in Figure 5, the stressed pulsed I-V where the LJFET was biased in off-state (V_{GQ} = -40 V) with high voltage drain stress (V_{DQ} = 40 V) shows signs of increased dynamic on-resistance or current collapse. However, a similar degree current collapse is observed under gate stress alone (V_{GQ} = -40V, V_{DQ} = 0V). This indicates that the high reverse gate voltage required to turn off the device is the primary trapping mechanism. Therefore we expect that dynamic R_{ON} can be minimized by engineering the device structure to achieve a more reasonable V_T in addition to implementing an optimized highly-resistive buffer or a p-GaN buffer.

CONCLUSIONS

A conceptual protoype for a LJFET was demonstrated. A series of experiments were performed using a wide range of channel doping, resulting in experimental verification of useful channel doping range. The 200mA/mm current density is indicative of good channel mobility, but further determination will require Hall-effect measurements. The C-V measurements reveals the role of the C-doped buffer in creating a depletion region at the back of the channel, clarifying the need for a p-GaN buffer and back contact.

ACKNOWLEDGEMENTS

J.C. Gallagher and G.M. Foster acknowledge support from the American Society for Engineering Education (ASEE) postdoctoral fellow program. The authors are sincerely grateful to the following NRL Staff: Anthony Boyd, Walter Spratt, and Dean St. Amand for cleanroom equipment support.

REFERENCES

[1] I.C. Kizilyalli, P. Bui-Quang, D. Disney, H. Bhatia, O. Aktas "Reliability studies of vertical GaN devices based on bulk GaN substrates" *Microelectron. Reliab.* **55** 1654-1661 (2015)

[2] G. Xie, E. Xu, B. Zhang, W.T. Ng "Study of the breakdown failure mechanisms for power AlGaN/GaN HEMTs implemented using a RF compatible process" *Microelectron. Reliab.* **52**, 964-968 (2012)

[3] S. Chowdhury and U. K. Mishra, "Lateral and Vertical Transistors Using the AlGaN/GaN Heterostructure," *IEEE Trans. Electron Devices* **60**, 3060–3066 (2013)

[4] T. Oka, T. Ina, Y. Ueno, and J. Nishii, “1.8 mΩ·cm 2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation,” *Appl. Phys. Express* **8**, 054101 (2015)

[5] D. Ji, A. Agarwal, H. Li, W. Li, S. Keller and S. Chowdhury, "880 V/2.7 mΩ-cm^2 MIS Gate Trench CAVET on Bulk GaN Substrates," *IEEE Electron Device Lett.,* **39**, 863-865 (2018)

[6] T. J. Anderson, A.D. Koehler, M.J. Tadjer, J.K. Hite, A. Nath, N.A. Mahadik, O. Aktas, V. Odnoblyudov, C. Basceri, K.D. Hobart, F.J. Kub “Electrothermal evaluation of thick GaN epitaxial layers and AlGaN/GaN high electron mobility transistors on large-area engineered substrates” *Appl. Phys. Express* **10**, 126501 (2017)

[7] L. Zhang, L.F. Lester, A.G. Baca, R.J. Shul, P.C. Chang, C.G. Wilson, U.K. Mishra, S.P. Denbaaars, J.C. Zolper “Epitaxially-Grown GaN Junction Field Effect Transistors” *IEEE Trans. Electron Devices* **47** (3), 507-511 (2000)

[8] J.A. Appels, H.M.J. Vaes, “High Voltage Thin Layer Devices (RESURF Devices)” IEDM Tech. Dig.,1979, pp. 238-241

[9] T.J. Anderson, L.E. Luna, A.D. Koehler, M.J. Tadjer, K.D. Hobart, F.J. Kub, O. Aktas, V. Odnoblyudov, C. Basceri. “Lateral GaN JFET Devices on 200 mm Engineered Substrates for Power Switching Applications” 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications Conference Proceedings