

Low Interface Noise of p-GaN Gate Normally-off HEMT with Microwave Ohmic Annealing Process

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Keywords: p-GaN gate HEMTs, Enhancement mode, Mg out-diffusion, microwave annealing (MWA), Ohmic contacts

Abstract

In this work, a high-performance AlGaIn/GaN normally-off p-gallium nitride (GaN) gate high electron mobility transistor (HEMT) was fabricated through low-temperature microwave annealing (MWA) in an ohmic metal alloy process. Compared with the conventional high-temperature rapid thermal annealing (RTA) process, MWA results in simultaneously superior ohmic contact and wafer sheet resistance because of the superior surface morphology of ohmic metal alloys. Moreover, Mg out-diffusion can be prevented through low-temperature MWA processes. The MWA p-GaN gate HEMT exhibited a maximum drain current density (I_{Dmax}) of 363 mA/mm with a threshold voltage (V_{TH}) of +1.6 V, a low subthreshold swing slope of 85 mV/dec, and a static on-resistance (R_{ON}) of 10.2 $\Omega \cdot mm$. The low frequency noise (LFN) and pulsed I-V indicated suppression of Mg out-diffusion, which could have induced extra traps in the device channel had it not been suppressed.

INTRODUCTION

Wide-bandgap GaN-based semiconductor materials are attracting a great deal of interest for high-power, high-frequency, and high-temperature applications [1]. Notably, normally-off device operation with a positive threshold voltage can avoid power dissipation. Several approaches for fabricating normally-off AlGaIn/GaN high electron mobility transistors (HEMTs) have been reported, such as gate-recessed structures [2], fluoride-based plasma treatment [3], selective AlGaIn barrier layer oxidation [4], and p-type GaN (p-GaN) gates [5]–[7]. Currently, the only commercially available devices are normally-off GaN HEMTs with p-GaN gates; they are also the most promising devices. In typical studies, p-GaN gate HEMT samples with the Mg-doped GaN cap layer have been activated at approximately 700 °C; typically, Mg out-diffusion increased with active temperature. However, conventional high-temperature (>800 °C) rapid thermal annealing (RTA) processes in the ohmic alloys of p-GaN gate HEMTs not only suffer from high thermal budgets but also tend to exacerbate the out-diffusion of Mg into the AlGaIn barrier and GaN channel [8], [9]. This phenomenon

tends to create extra trap centers that reduce drain current. Due to Ni–Al alloy aggregation behavior, some balling-up of Ti/Al/Ni/Au ohmic metal was observed on the device surface after RTA [10]. Therefore, this study produced smooth ohmic contacts on an AlGaIn/GaN heterostructure by employing microwave annealing (MWA) that allowed low-temperature (450 °C–550 °C) ohmic contact formation [11].

In this study, Mg atom out-diffusion from the p-GaN layer was suppressed under ohmic annealing of the MWA p-GaN gate HEMT. Compared with p-GaN gate HEMTs fabricated through conventional RTA processes, devices fabricated through this MWA process achieved lower sheet resistance and fewer traps in the channel because of the low-temperature process environment.

EXPERIMENTAL PROCEDURES

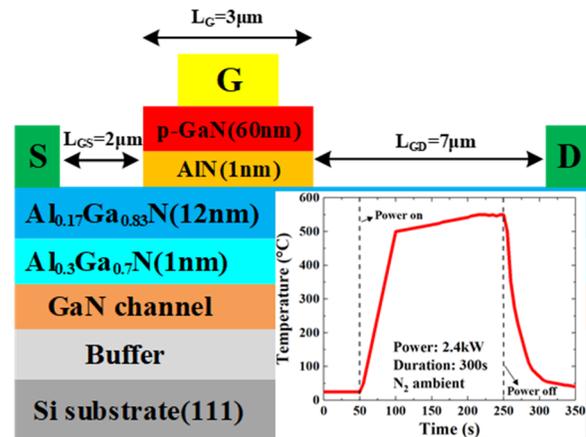


Fig. 1. Cross-sectional schematic of the p-GaN gate HEMT and temperature profile of the MWA process.

Fig. 1 shows a cross-sectional schematic of the p-GaN gate HEMT structure deposited through metal-organic chemical vapor deposition (MOCVD) on a 6-in Si (111) substrate. An undoped GaN channel layer was grown on a 4- μm -thick buffer transition layer. An undoped composite barrier (1-nm-AlN/12-nm-Al_{0.17}Ga_{0.83}N/1-nm-Al_{0.3}Ga_{0.7}N) layer having a thickness of 14 nm was sandwiched between a GaN channel layer and a 60-nm p-type GaN cap layer [12]. The device

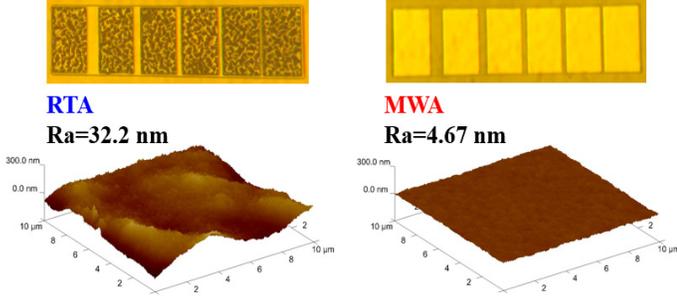


Fig. 2 Optical image and 3-D AFM image of ohmic contacts fabricated through (a) RTA and (b) MWA.

fabrication started from defining the mesa area through reactive ion etching (RIE). The p-GaN island was formed by N_2O oxidation/HCl cyclic etching [13]. Ohmic contacts were prepared through the electron beam evaporation of multilayer Ti/Al/Ni/Au (25/130/25/80 nm) in a traditional lift-off process. For the RTA-HEMT, the sample was annealed at 875 °C for 35 s under nitrogen-rich ambient conditions. For the MWA-HEMT, the sample was annealed at an RF power of 2.4 kW with a frequency of 6 GHz for 300 s under N_2 atmosphere. The temperature profile of the MWA process at 2.4 kW is also shown in Fig. 1. The peak temperature was 550 °C; it was evaluated using a thermocouple during MWA for 300 seconds in an N_2 -rich environment. Figure 2 shows optical photographs and high-resolution atomic force microscopy (AFM) images for samples fabricated on the ohmic contact surfaces of the transmission-line method (TLM) structure to evaluate the surface morphology of both devices after the annealing process. Results indicated that the ohmic contact surface of the RTA p-GaN gate HEMT exhibited a reacted appearance, whereas the surface was uniform and flat in the MWA device. Moreover, the average roughness (Ra) of the p-GaN gate HEMT developed through RTA increased to 32.2 nm, and this value was 4.67 nm that developed through MWA owing to Ni metal balling-up in a high-temperature atmosphere. The contact resistance values of the RTA-HEMT and MWA-HEMT were 1.15×10^{-6} and $1.01 \times 10^{-6} \Omega \cdot \text{cm}^2$, respectively. The corresponding channel sheet resistance values were 536 and 452 Ω/\square , respectively, which were measured using a TLM test structure after annealing. After the gate region of the Ni/Au (25/120 nm) metal layer had been deposited, a 200-nm-thick SiO_2 surface passivation layer was deposited with a e-beam evaporator. The lengths of gate-to-source (L_{GS}), gate (L_G), and gate-to-drain (L_{GD}) were 2, 3, and 7 μm , respectively. The width of the device (W) was 50 μm .

RESULTS AND DISCUSSION

To accurately observe the material out-diffusion in the device after w/o annealing, RTA, and MWA, secondary-ion mass spectrometry (SIMS) was performed. The results are shown in Fig. 3; they suggest that Mg atoms diffused into channel after RTA, which worsened the 2-DEG confinement for RTA p-GaN HEMTs. In other words, the Mg out-diffusion

effect of the p-GaN gate HEMTs under ohmic annealing was suppressed by MWA process.

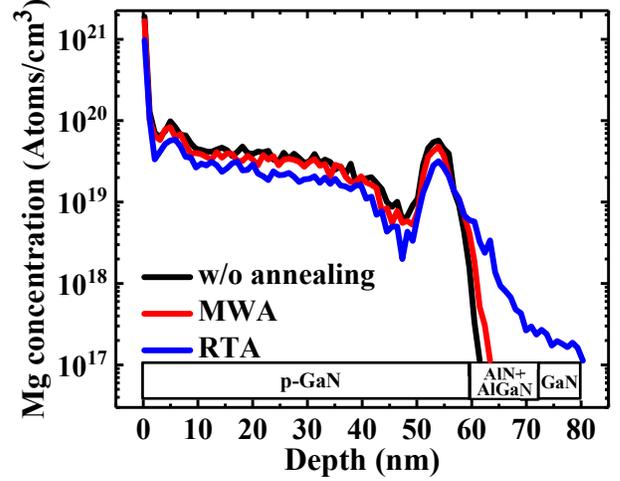


Fig. 3. Mg concentration profile (SIMS) of the p-GaN gate HEMT fabricated w/o annealing and through MWA and RTA.

Figure 4 displays the log-scale $I_{DS}-V_{GS}$ transfer characteristics and $I_{DS}-V_{DS}$ outputs of both devices at $V_{DS} = 10$ V. The threshold voltage (V_{TH}) values of RTA-HEMT and MWA-HEMT were 1.7 and 1.6 V (defined by the $I_{DS} = 1$ mA/mm), respectively. The corresponding maximum drain current density (I_{Dmax}) values were 272 and 363 mA/mm, respectively. The I_{Dmax} value was 25% higher for the MWA-HEMT because of this device's low sheet resistance and excellent 2DEG carrier confinement, achieved through the low-temperature annealing procedure. For the MWA-HEMT, reduction in the off-state I_{DS} leakage current increased the magnitude of the ON/OFF drain current ratio by approximately two orders of magnitude. The subthreshold swing slope (S.S) of the MWA-HEMT was improved from 98 to 85 mV/dec compared with that of the RTA-HEMT. Figure 4 displays appropriate DC output characteristics for both devices; the static R_{ON} values for the RTA-HEMT and MWA-HEMT were 14.6 and 10.2 $\Omega \cdot \text{mm}$ at $V_{GS} = 8$ V, respectively.

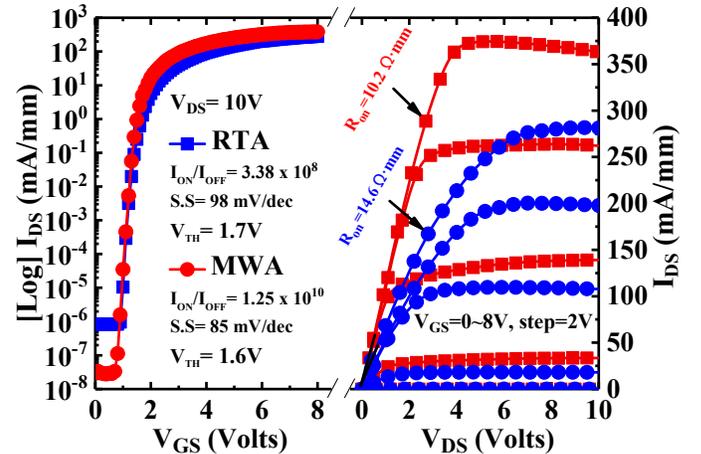


Fig. 4 Log-scale $I_{DS}-V_{GS}$ transfer and $I_{DS}-V_{DS}$ output characteristics with RTA and MWA.

The three-terminal breakdown voltages (V_{BR}) of devices with gate-to-drain spacing (7 μm) were measured using an Agilent B1505A measurement system, and the Si substrate was floating during the measurement. The three terminal OFF-state breakdown voltage characteristics of both devices are shown in Fig. 5, and the reverse gate leakages are also illustrated in the inset. The reverse gate leakage current levels of the RTA-HEMT and MWA-HEMT were 6.29×10^{-7} and 2.61×10^{-8} at $V_{GS} = -10$ V, respectively. The measurement breakdown voltage can be improved more than 127 V compared with the RTA-HEMT by off-state leakage lower than one order of magnitude in the MWA-HEMT.

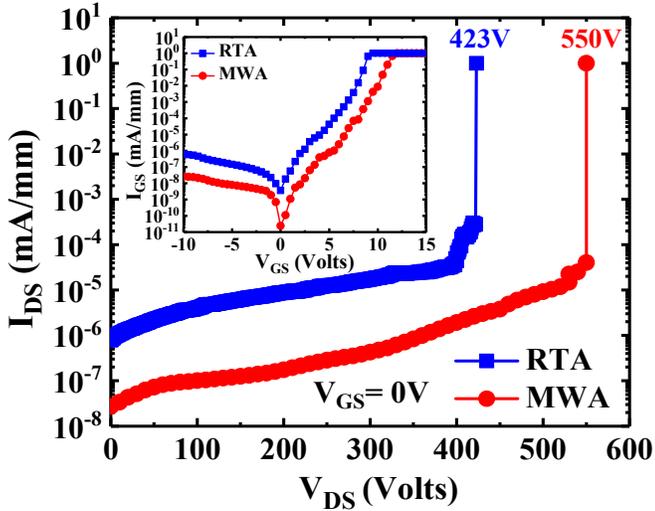


Fig. 5 Typical OFF-state breakdown characteristics measured at $V_{GS} = 0$ V and reverse gate leakage for both devices.

To further study the traps in the channel layer of both devices, low frequency noise (LFN) spectra with various gate overdrive bias voltages were measured. The $1/f$ noise measurements were performed using an HP4142 power supply, an Agilent E3611a control unit, and an Agilent 35670A dynamic signal analyzer. In Fig. 6, Hooge's parameter α_H can give a measure of the total number of active

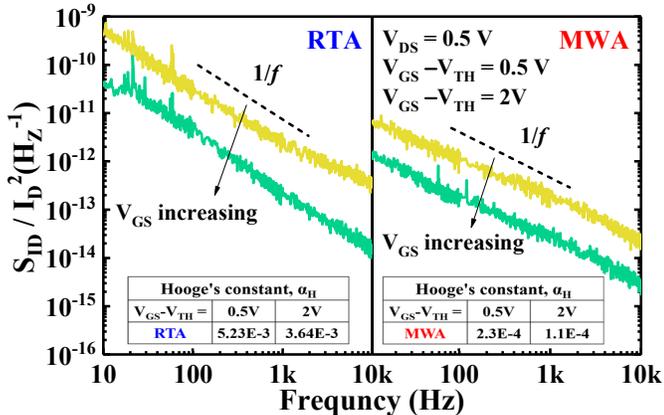


Fig. 6 LFN spectra characteristics and Hooge's constant with various V_{GS} overdrive values for both devices.

traps, which caused noise and can be used as a rough figure of merit to characterize these devices. The α_H value for the MWA-HEMT was on the order of 10^{-4} . This value was 10^{-3} for the RTA-HEMT. The evidence clearly suggests that the MWA-HEMT can be attributed to the suppression of Mg out-diffusion inducing extra trap centers at the AlGaIn/GaN interface.

Figure 7 shows the pulsed I-V characteristics of both devices switched from the off state with a V_{DSQ} of 0 V and V_{GSQ} ranged from 0 to -20 V with a voltage step of -5 V at room temperature with an on-state gate bias of 6 V [14]. The device was switched with 1- μs pulse width and a 10- μs period. Clearly, the degradation of I_{DS} was improved by approximately 17% in the MWA-HEMT at a V_{DS} of 10 V, which implied the channel defect trap density was lower than that of the RTA-HEMT.

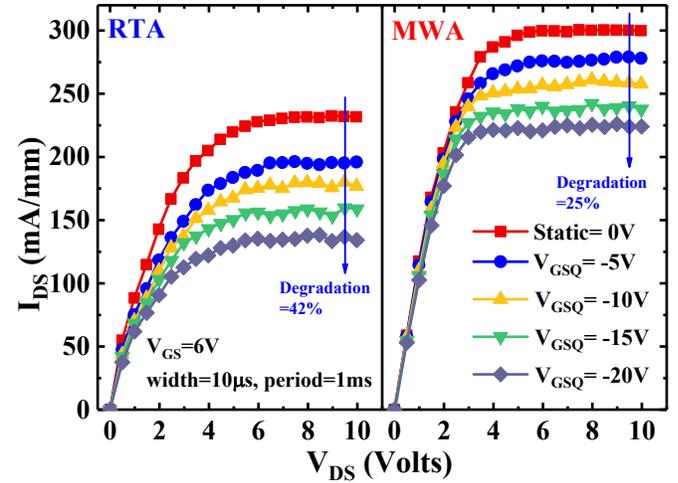


Fig. 7 Pulsed I_{DS} - V_{DS} characteristics from quiescent gate bias (V_{DSQ}) point of 0 V with 10 μs pulse width and 1 ms pulse period. Afterward, the quiescent drain bias (V_{GSQ}) was swept from 0 to -20 V (in -5 V increments).

CONCLUSIONS

In this letter, the MWA method was adopted to form the ohmic contacts of a p-GaN gate HEMT. Use of the low-temperature MWA technique resulted in comparatively excellent electrical characteristics and a surface much smoother than that of an RTA device. The MWA-HEMT exhibited a leakage current level as low as 10^{-8} mA/mm, which was approximately two orders of magnitude lower than that of the RTA-HEMT. An extremely high ON/OFF drain current ratio of up to 1.25×10^{10} was obtained. Moreover, the SIMS analysis indicated severe Mg out-diffusion in the conventional RTA method. The low-temperature MWA process can suppress Mg out-diffusion. The experimental results imply that the MWA technique is a promising method for fabricating high-performance normally-off p-(Al)GaIn/AlGaIn/GaN HEMTs.

REFERENCES

- [1] J. Das, et al., “A 96% efficient high-frequency DC–DC converter using E-mode GaN DHFETs on Si,” *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1370–1372, Oct. 2011.
- [2] M. Kanamura, et al., “Enhancement-mode GaN MIS-HEMTs with n-GaN/i-AlN/n-GaN triple cap layer and high-k gate dielectrics,” *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 189–191, Mar. 2010.
- [3] W. Chen, et al., “Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters,” in *Proc. IEEE IEDM*, pp. 1–4, Dec. 2008.
- [4] H.-C. Chiu, et al., “Characterization of enhancement-mode AlGaIn/GaN high electron mobility transistor using N₂O plasma oxidation technology,” *Appl. Phys. Lett.*, vol. 99, no. 15, pp. 153508-1–153508-3, Oct. 2011.
- [5] L.-Y. Su et al., “Enhancement-mode GaN-based high electron mobility transistors on the Si substrate with a P-type GaN cap layer,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 460–465, Feb. 2014.
- [6] I. Hwang et al., “p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current,” *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 202–204, Feb. 2013.
- [7] Y. Uemoto, et al., “Gate injection transistor (GIT)—A normally-off AlGaIn/GaN power transistor using conductivity modulation,” *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007.
- [8] K. Köhler, et al., “Diffusion of Mg dopant in metal-organic vaporphase epitaxy grown GaN and Al_xGa_{1-x}N,” *Journal of Applied Physics*, Vol. 113, p. 073514, 2013.
- [9] N. E. Posthuma, et al., “Impact of Mg out-diffusion and activation on the p-GaN gate HEMT device performance,” *ISPSD*, pp. 95-98, 2016.
- [10] R. Gong, et al., “Analysis of surface roughness in Ti/Al/Ni/Au Ohmic contact to AlGaIn/GaN high electron mobility transistors,” *Appl. Phys. Lett.*, vol. 97, no. 6, pp. 062115-062117, Aug. 2010.
- [11] L.-Q. Zhang et al., “Low temperature ohmic contact formation in GaN high electron mobility transistor using microwave annealing,” *IEEE Trans. Electron Devices*, vol. 36, no. 9, Sep 2015.
- [12] H.-C. Chiu, et al., “High-Performance Normally-off p-GaN Gate HEMT with Composite AlN/Al_{0.17}Ga_{0.83}N/Al_{0.3}Ga_{0.7}N Barrier Layers Design” *IEEE J. Electron Devices Soc.*, vol. 6, issue.1 pp. 201–206, 2018.
- [13] H.-C. Chiu, et al., “High Uniformity Normally-OFF p-GaN Gate HEMT Using Self-Terminated Digital Etching Technique,” *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4820–4825, Feb. 2018.
- [14] N. Ramanan, et al., “Device Modeling for Understanding AlGaIn/GaN HEMT Gate-Lag”, *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2012–2018, Jun. 2014.

ACRONYMS

HEMT: High Electron Mobility Transistor
 2DEG: Two-Dimensional Electron Gas
 MWA: Microwave annealing
 RTA: Rapid Thermal Annealing
 LFN: Low Frequency Noise