Development of Advanced Lift-Off Processes for 5G and VCSEL Applications

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Abstract

Trends such as VCSEL implementation for facial recognition in smartphones or 5G deployment are gaining momentum. These technologies rely heavily on compound semiconductors to provide the best performance. As the performance requirements evolve, manufacturers will need to increasingly rely on the Metal Lift-Off (MLO) process to pattern the metal layers and form the devices. In an MLO process, a wafer is coated with photoresist, exposed and developed to form the design, deposited with desired metal, and then submerged into a resist remover chemistry to strip the sacrificial photoresist/excess metal. MLO processes are used if the metal to be patterned is not easily etched with plasma or if there is a concern regarding substrate damage. A successful MLO process is a function of the incoming photoresist profile, the incoming metal deposition profile, and the stripping process. A collaboration between vendors provides integration between these processes and guarantees repeatable results, high throughput, and low cost of ownership. Silicon wafers demonstrating each of these optimized processes and experimental results are given below.

INTRODUCTION

The purpose of this paper is to demonstrate how appropriate photoresist selection, optimized metallization parameters, appropriate resist remover selection, and an optimized metal lift-off process can decrease defects, increase throughput, and lower cost. A brief introduction to each process (photolithography, metallization, lift-off) is provided, followed by a summary of experimental results demonstrating the benefits of integrated processes and vendor collaboration.

Photolithography

As More-Than-Moore applications continue to mature and expand in complexity so does the need to extend lift-off capabilities to finer geometries, improve process consistency, and provide a stable manufacturing process. To accomplish these goals, a simple, robust lift-off process to pattern metals is needed. An important consideration in this process is the photoresist. The correct photoresist can make the process simpler, cheaper, more stable, and robust.

AZ® nLOF series i-line resists meet such requirements. They are engineered for MLO applications to replace complex image reversal and multi-layer lift-off lithography processes. Ideal lift-off patterns are achieved using a standard expose/post-expose bake/develop process flow. AZ® nLOF series photoresists are fast and printed features are thermally stable to > 200°C. These resists are developable in standard TMAH-based developers. AZ® nLOF 2000 series i-line resists can single coat to thicknesses from 2.0 µm to > 10 µm. AZ® nLOF 5510 i-line photoresist is a 2^{nd} generation MLO resist designed for resolution to 0.25 µm. Given these performance characteristics, AZ® nLOF 2070 and AZ® nLOF 5510 were chosen for the experiments to determine the MLO performance with various line/space geometries.

Metallization

The metal deposition process will affect the shape and position of the metal within the defined pattern and the ease of lift-off. Electron beam evaporation can provide a normal angle of incidence for the deposition as compared with sputter deposition with diffuse transport that results in sidewall coverage. As wafer sizes increase, it becomes more challenging for the system design to maintain the proper wafer alignment along with film uniformity, deposition rate, and cost of ownership. The unique design of the UEFC6100 HULA (High Uniformity Lift-off Assembly) and substrate motion results in highly uniform films (~1%), efficient material collection (>20%), and high wafer capacity (25-200mm wafers) [1].

For 200mm wafers, the throw distance, or source radius (SR), increases to maintain the angle of incidence within 5 degrees off normal from center to edge. The work in this study takes a closer look at the metal deposition across the wafer and orientation in the system as it compares with the theoretical model. The shape and position of the metal as deposited within the photoresist lift-off structure illustrates the benefits of the UEFC6100 system design.

Lift-off – Resist Remover Selection

Another important consideration for the MLO process is the resist remover selection for stripping the photoresist. Ideally, the resist remover should clean the resist quickly and consistently while not etching sensitive metals or substrates. A resist remover that meets these criteria would lead to higher wafer throughput, lower rework rates, lower defectivity levels, and better electrical performance. Single solvents (Ex: NMP, DMSO) are often used for MLO processes. While they do lift the resist in many applications, complete dissolution is typically not achieved, especially with negative-tone resists. Undissolved resist can lead to higher defectivity levels, higher chemical consumption, shorter bath life, and shorter filter lifetime. Consequently, a resist remover that can dissolve the resist has many advantages which result in an overall lower cost of ownership for the process.

To achieve complete dissolution of the resist, it is important to match the resist remover chemistry with the photoresist being used. AZ® Remover 910 effectively dissolves AZ® nLOF series resists and has low etch rates on many commonly used metals. Experiments were conducted with this product to determine its ability to perform MLO on a variety of AZ® nLOF resists and metal stacks.

Lift-off – Tool Selection

Choosing the correct lift-off tool is critical to process repeatability. Veeco's WaferStorm® solvent-based platform with ImmJET™ technology allows for higher throughput and lower cost of ownership compared to conventional wet bench or single wafer spray tools. ImmJET™ technology provides a batch immersion and single wafer spray system. Through automated handling and advanced software, the process ensures each wafer is immersed and sprayed for the same amount of time, guaranteeing wafer to wafer repeatability. Utilizing a batch immersion process reduces the spray time per wafer, resulting in increased throughput. WaferStorm® also recirculates used chemistry, passing it through multiple filters, lowering the overall cost of ownership.

EXPERIMENTAL SETUP

Wafer Patterning

Experiments were conducted using 6" silicon wafers that were patterned using 2 different photomasks in order to achieve different line/space geometries. A first mask, 50DL, was used for 0.50 µm line/spaces using AZ® nLOF 5510. Wafers were coated on a TEL CleanTrack™ Mark 8 and spun at 2850 rpm followed by a softbake of 90ºC/60sec to achieve a film thickness of ~1µm. A post-exposure bake (PEB) was then performed at 110ºC for 60 seconds.

A second mask, 10-50LS, was used for 10-50 µm line/spaces using AZ® nLOF 2070. Wafers were coated on a TEL CleanTrack™ Mark 8 and spun at 2940 rpm followed by a softbake of 110ºC/90sec to achieve a film thickness of 7µm. A post PEB was then done at 110ºC for 90 seconds. Both wafers were developed using AZ® 300MIF Developer prior to metal deposition.

Metallization

The metal deposition in the UEFC6100 utilized a Temescal STIH-270-3CK PopTop six-pocket electron beam gun with 25cc pockets. This gun design is ideal for minimizing cross-pocket contamination by sealing the unused pockets while the active pocket is evaporating material. The metal purity for these tests was 99.99% to 99.999%. The power to the electron beam gun was delivered by a 10kV CV-12SLX solid-state power supply.

The titanium deposition rate for all the samples was 5 Å/s. The platinum was deposited at a rate of 1 Å/s. The gold, copper and AlCu films were all deposited at rates of 10 Å/s. The AlCu was evaporated straight from the water-cooled copper crucible while the gold and copper evaporations utilized lanthanated-tungsten liners to achieve the desired rate at lower powers. The deposition conditions were chosen to ensure good control of the average thickness and thickness uniformity, as well as limit stress and particle defects. The deposition power levels ranged from near or just under 1kW for the gold and copper to powers around 5kW for the AlCu. The combination of the electron beam gun and system designs leads to limited substrate heating with peak monitored system temperatures of 70°C and substrate carrier temperatures below 50°C during these process runs. To make sure that the full range of deposition angles that are experienced by 200mm wafers were included on the 6" wafers, the wafers were mounted in adapters which placed them at the equivalent position of the edge of a 200mm wafer before being loaded into the UEFC6100.

TABLE 1. EXPERIMENTAL VARIABLES AND PARAMETERS

Photoresist	Line/Space (um)	Metals	Metal Thickness (nm)	Source Radius (inch)
AZ® nLOF 5510	0.50	Ti/Pt/Au	100/100/200	46"
AZ® nLOF 5510	0.50	Ti/AlCu	100/300	46"
AZ® nLOF 5510	0.50	Ti/AlCu	100/300	35.5"
AZ® nLOF 2070	10-50	Ti/Cu	100/3900	46"
AZ® nLOF 2070	10-50	Ti/Cu	100/3900	35.5"

Metal Lift-off Process

After wafer patterning and metal deposition, the wafers were processed using AZ® Remover 910 for lift-off of the resist/metal. AZ® Remover 910 is an acidic, solvent-based remover capable of dissolving negative-tone resists such as the AZ® nLOF series. The solvent is able to penetrate and swell the resist while the acidic component is able to further break down and enable the dissolution of the resist. In addition, AZ® Remover 910 is REACH compliant, meaning that it does not contain NMP, DMSO or any other solvents known to cause adverse health effects. It also has low etch rates on most common metals and is water soluble, eliminating the need for an intermediate rinse.

The wafers were processed in a Veeco WaferStorm® metal lift-off system. Veeco's WaferStorm® is an automated, dry-in/dry-out tool that ensures consistent wafer-to-wafer MLO processing. The first step in that process is for the automated robot to remove a wafer from the front opening unified pod (FOUP) or cassette and transfer it to the immersion station. The immersion station can hold multiple wafers, whereas the spray station processed one wafer at a time. Veeco's advanced software controls the timing of wafers taken from the FOUP or cassette and placement into the immersion and spray stations, ensuring each wafer is processed with identical process times.

Each wafer was soaked in a heated immersion tank of AZ® Remover 910 at 80°C. This allowed the solvent to swell the photoresist and made the lift-off faster and more efficient. The immersion time for both types of photoresist was 15 minutes. After soaking, the wafers were transported to a different station and high-pressure chemical (HPC) fan sprayed at 1500 psi for one minute. A lower spray pressure of 500 psi was evaluated but did not completely remove the lifted resist and metal. The AZ® Remover 910 is dispensed through a rectangular opening in the nozzle, which creates an approximately 1.5" long fan spray on the wafer surface (Figure 1). This fan spray removed the lifted photoresist and excess metal from the wafer surface. To ensure a pristine surface, each wafer was transferred from the chemical spray station to a separate spray station, where it was rinsed with DI water and spun dry.

Figure 1. Spray station (left) and high-pressure chemical (HPC) fan spray (right).

Table 2. Process flow for metal lift-off on silicon wafers

Step	Process	Chemical	Time	Speed (rpm)
1	Wafer immersion	AZ® Remover 910	15 minutes	N/A
2	HPC Fan Spray	AZ® Remover 910	1 minute	200
3	Rinse	DI Water	15 seconds	200
4	Dry	N/A	45 seconds	1500

Results

Complete metal lift-off was achieved on all wafer types. The below microscope and SEM images (Figures 2-4) show features on the wafer surface before and after the lift-off process.

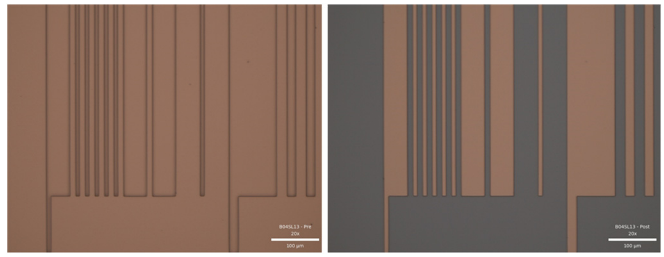

Figure 2. Microscope image at 20X before (left) and after (right) lift-off using 10-50LS Mask design with Ti/Cu (100nm/3900nm)

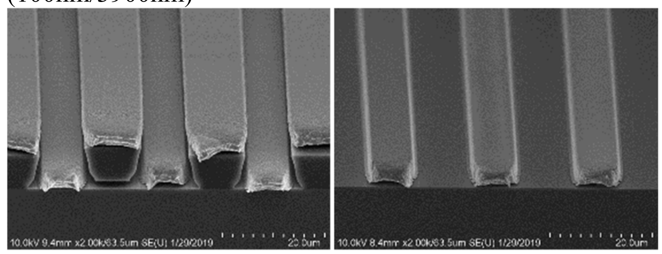

Figure 3. SEM image at 2kX before (left) and after (right) lift-off using 10-50LS Mask design with Ti/Cu (100nm/3900nm).

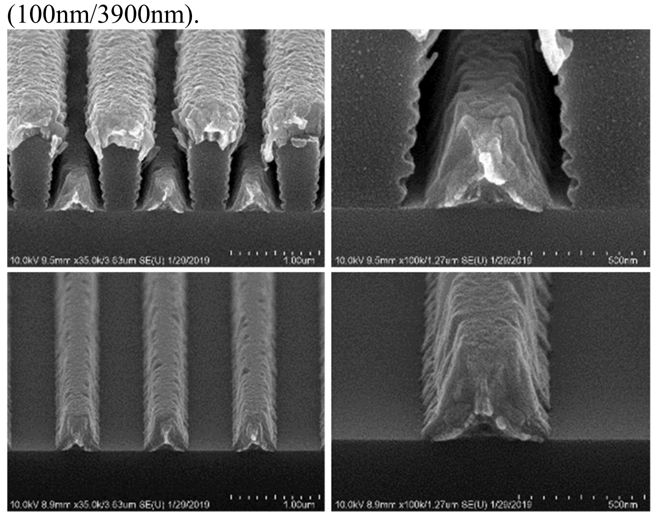

Figure 4. SEM images before (top row) and after (bottom row) lift-off at 35kX magnification (left column) and 100kX magnification (right column) using 50DL Mask design with Ti/AlCu (100nm/300nm)

Conclusion

Photolithography

One critical element for a good MLO process is the resist sidewall profile. The sidewall of the nLOF resist pattern in this study was not covered in metal (Figure 5, right column), due in part to the retrograde angle of the sidewall. A test wafer using AZ® 15nXT, a photoresist for etching and electroplating applications, was metallized to demonstrate an unoptimized process with incorrect photoresist selection.

The vertical sidewall was clearly coated, preventing the solvent from penetrating the metal to dissolve the photoresist. This photoresist would be challenging to remove, thereby increasing process times and decreasing throughput. The AZ nLOF photoresist series is specifically designed for MLO and is the correct photoresist for an optimized process.

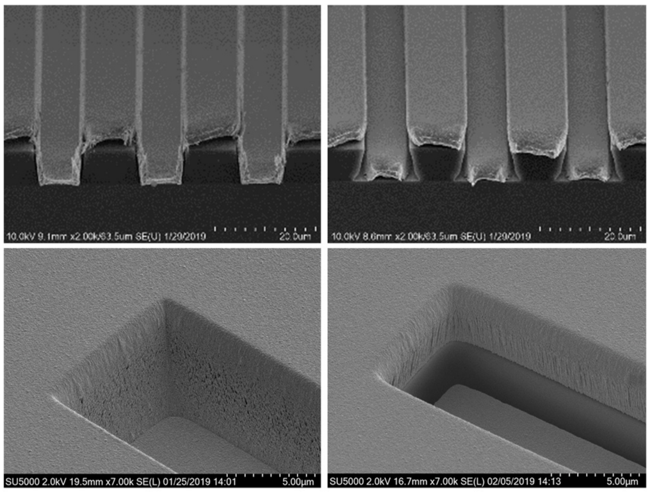

Figure 5. SEM images comparing sidewall metallization with incorrect photoresist selection (left- AZ 15 nXT) and correct photoresist selection (right -AZ nLOF).

Metallization

The experimental results show excellent agreement with the theoretical model as illustrated in the images below. These SEM images were taken at the edge of the wafer and demonstrate the changes in metal cross-section with throw distance from the source. As predicted by the model (see Fig. 6), the horizontal lines show a larger shift to the left for the shorter 35.5” throw distance. For the vertically oriented lines there is no difference (Figure 6).

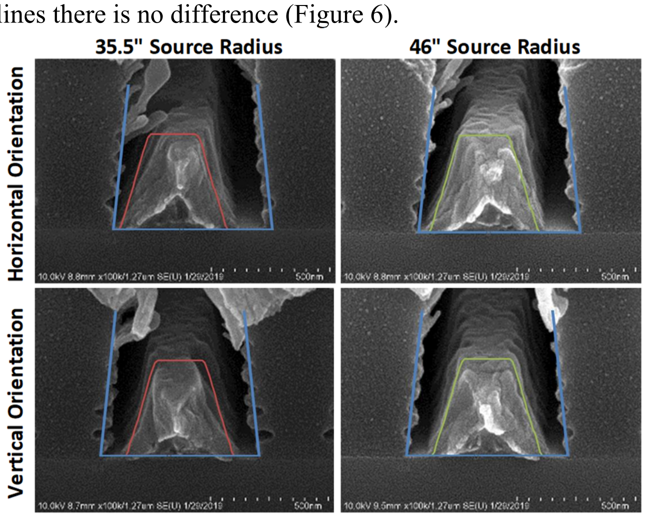

Figure 6. SEM Images and model results of Ti/AlCu metal deposition near the edge of a 200mm wafer for structures in two different orientations on the wafer. Blue lines are the modeled resist location, red lines are modeled metal deposition at 35.5” and green lines are modeled metal deposition at 46”.

The UEFC6100 system design provides a more robust metallization capability and minimizes sidewall deposition as the photoresist structure varies. The reduced positional shift in the metal near the edge of the wafer relative to underlying features also can become critical as feature size decreases.

Lift-off – Resist Remover Selection

AZ® Remover 910 is an organic solvent-based, acidic product that was designed to lift and dissolve negative-tone, chemically amplified crosslinked resist. The data shown in this study demonstrate that even for small line/space geometries down to 0.5 µm, the chemistry is able to penetrate and dissolve the resist in short process times, i.e. soak times (15min). It is also able to dissolve positive-tone resists such as DNQ/Novolac, making it a versatile chemistry that can be used with various resist types. It does not contain NMP or DMSO, two solvents that are increasingly being replaced due to their adverse health effects. AZ® Remover 910 is REACH compliant, a European regulation regarding safe working environments.

Lift-off – Tool Selection

Veeco’s WaferStorm® platform with ImmJET™ technology provides an ideal solution for high throughput MLO processes. The above data demonstrate that WaferStorm® can lift-off metal smaller than one-micron line/space and thick metal for larger dimensions, leading the way for future 5G and VCSEL applications. Chemistry is passed through multiple filters, thereby lowering the cost of ownership. Veeco’s advanced software allows the end user to customize and optimize every aspect of the process.

Veeco's compact three chamber tool (M3303), utilizing only 33 square feet, can provide up to 41 wafers per hour (WPH) using the above process. A five-chamber high volume manufacturing tool (M3305) can reach up to 81 WPH with the above process times. Multiple tool configurations provide the end user with flexibility to suit their processing needs.

The above results demonstrate that collaboration between vendors can provide optimized and established processes, so customers can more easily and quickly develop new products. High throughput and low cost of ownership is possible due to these optimized processes.

References

[1] G. Wallace, “Electron-beam Lift-off: Collection efficiency & Paths to improvement”, Compound Semiconductor, V. 19, March 2013

Acronyms

VCSEL: Vertical Cavity Surface Emitting Laser