Backside Processing of RF GaN-on-GaN HEMTs Considering Thermal Management

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Abstract

In this study, we developed a method for backside processing of GaN substrates for thermal management of RF GaN-on-GaN high-electron-mobility transistors (HEMTs). We optimized the thermal management of GaN-on-GaN using thermal simulation and found that the temperature rise was minimum at a substrate thickness of 100 μm. In addition, we confirmed that by increasing heat source spacing to more than 40 μm, the temperature rise of GaN-on-GaN was lower than that of GaN-on-SiC. From these results, we developed a method for backside processing of GaN-on-GaN. We bonded a 2-inch GaN substrate to a 4-inch supporting carrier with an adhesive material and ground it from the N-polar surface side. By backgrinding, the GaN substrate could be thinned to less than 150 μm. After chemical-mechanical polishing (CMP), an excellent surface morphology with an average surface roughness of less than 0.2 nm was obtained. Furthermore, we demonstrated that the thin GaN substrate could be cut within an average chipping of size 30 μm using normal blade dicing. However, we found that stealth dicing was more effective for GaN substrate.

INTRODUCTION

The use of gallium nitride (GaN) substrates for manufacturing high-frequency and high-power GaN high-electron-mobility transistors (GaN HEMTs) has drawn much attention because of the substrates potential to grow high-quality GaN epitaxial layers due to their extremely low dislocation density (10^4–10^6 cm^{-2}) [1]. Thus far, there have been several reports on improving the device performance, in terms of gate leakage, current collapse, reliability, and breakdown [2–5]. A GaN substrate exhibits a thermal conductivity (230 W/mK) lower than that of the widely used silicon carbide (SiC) substrate (420 W/mK) [6]. Killat *et al.* reported that GaN-on-GaN devices exhibit thermal resistance similar to as that of GaN-on-SiC devices because of the absence of a thermal boundary resistance [7]. With continuous wave operation in microwave heating, the heat dissipation of RF GaN HEMTs significantly affects the performance and reliability of the transistors. Therefore, it is important to thin the GaN substrate and dice it for optimum cooling efficiency. However, GaN substrates have lower hardness (11 GPa) compared to that of SiC substrates (25 GPa) [8]. In addition, GaN substrates grown using the void-assisted separation (VAS) method with hydride vapor phase epitaxy (HVPE) have almost the same hardness (22 GPa) as that of SiC substrates and the hardness depends on the low threading dislocation density [9].

In this study, we optimized the thermal management of GaN-on-GaN HEMTs using thermal simulation. We developed a method for backside processing of RF GaN-on-GaN HEMTs while considering thermal management.

OPTIMIZATION OF GAN-ON-GAN THERMAL MANAGEMENT

To optimize GaN-on-GaN thermal management, we used ANSYS Icepak for thermal simulation, and we evaluated the thermal conductivity of GaN substrate by periodic heating method. Moreover, VAS-grown conductive/semi-insulating GaN (0001) substrates with a dislocation density of less than 5×10^6 cm^{-2} (SCIOCS product) were used. Table I shows the measured thermal conductivities of conductive and semi-insulating GaN substrates; these were nearly the same as those in a previous report [6].

Fig. 1 shows the simulated structure, which consists of GaN epitaxial layer/substrate/AuSn/Cu. The thicknesses of GaN layer, AuSn, and Cu were 2, 25, and 1000 μm, respectively. The substrate thickness was varied from 10 to 300 μm. The chip size was 2×5 mm^2. The size of Cu heatsink was 10×10 mm^2. The individual power of each heat source was determined by assuming the output power density as 10 W/mm and the efficiency as 58.8%. Heat sources, each of them having a size of 0.5 × width (W_{gu}) × 0.1 μm^3, were placed on top of a GaN layer with a certain spacing between them (L_{gg}). The W_{gu} was varied from 100 μm to 200 μm. We decided the L_{gg} and the number of heat sources (n) such that they could fit inside the chip. The temperature rise was determined by finding the difference between the maximum temperature and Cu heatsink temperature.

Table II shows the thermal parameters used for the simulation. The thermal conductivity of GaN epitaxial layer

grown on SiC substrate was set to 130 W/mK because of its dislocation density of ~10^8 cm^{-2} [6]. Meanwhile, the thermal conductivity of GaN epitaxial layer grown on GaN substrate was set to be same as that of GaN substrate.

TABLE I MEASURED THERMAL CONDUCTIVITY OF VAS-GROWN GAN

	Thermal conductivity (W/mK)
Conductive GaN	212
Semi-insulating GaN	237

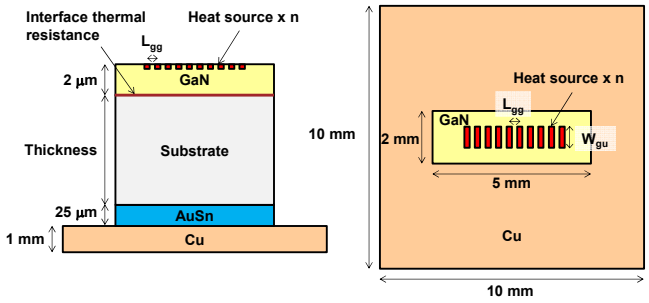

Fig. 1 Simulated structure with heat sources placed on top of a GaN epitaxial layer.

TABLE II THERMAL PARAMETERS USED FOR THERMAL SIMULATION

Parameters	GaN-on-SiC		GaN-on-GaN		AuSn	Cu
	GaN	SiC	GaN	GaN		
Thermal conductivity (W/mK)	130	420	230	230	57	385
Interface thermal resistance (m^2K/W)	2.5×10^{-8}		1×10^{-10}			

Fig. 2 shows a simulated comparison of substrate thickness dependence on temperature rise between GaN-on-GaN and GaN-on-SiC. The W_{gu} was varied (100, 150, and 200 μm), and L_{gg} was 30 μm. At W_{gu} of 100 μm and substrate thickness of 100 μm, the temperature rise of GaN-on-GaN was minimum and was nearly the same as that of GaN-on-SiC. However, as the W_{gu} increased, the temperature rise of GaN-on-GaN became larger than that of GaN-on-SiC, which indicates that the GaN-on-GaN device can easily be filled with heat.

Fig. 3 shows a simulated comparison of L_{gg} dependence on temperature rise between GaN-on-GaN and GaN-on-SiC. The substrate thickness was 100 μm. We adjusted the number of heat sources and the W_{gu} so that the total output power was fixed at 80 W. As a result, as the L_{gg} increased, the temperature rise of GaN-on-GaN decreased and became lower than that of GaN-on-SiC when L_{gg} was more than 40 μm. Although the thermal conductivity of GaN substrate is lower than that of SiC substrate, GaN-on-GaN has a higher potential of thermal management compared to GaN-on-SiC. The decrease of W_{gu} enables us to improve the high-frequency performance due to reduction in the phase rotation. On the other hand, the increase of n deteriorates high-frequency performance due to increasing of the phase shift. Therefore, it is important to design a device layout for both thermal property and high-frequency performance.

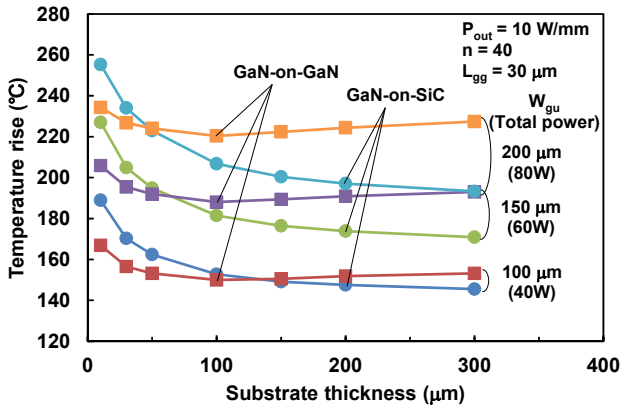

Fig. 2 Simulated comparison of substrate thickness dependence on temperature rise between GaN-on-GaN (■) and GaN-on-SiC (●) at various W_{gu}.

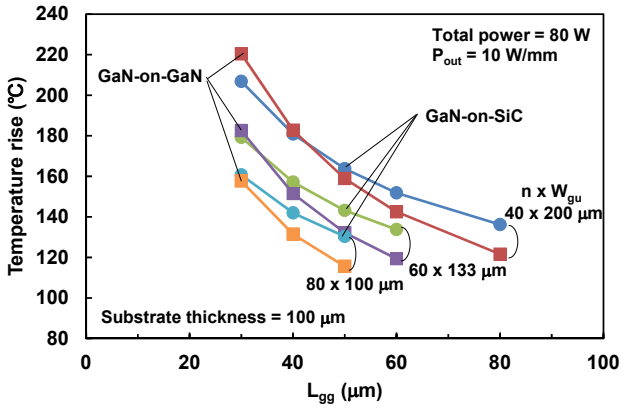

Fig. 3 Simulated comparison of heat source spacing distance dependence on temperature rise between GaN-on-GaN (■) and GaN-on-SiC (●) at various values of n × W_{gu}.

BACKGRINDING/CHEMICAL-MECHANICAL POLISHING OF GAN SUBSTRATE

Based on the above results, the target thickness of ground GaN substrate was set to less than 150 μm. When backgrinding GaN substrate, our developed SiC via-hole process was used [10]. First, a 2-inch GaN substrate was bonded to a 4-inch supporting carrier by thermoplastic

adhesion. Thereafter, the backside (N-polar side) of the GaN substrate was ground in two steps: with a coarse grinder and then with a fine grinder. After that, chemical-mechanical polishing (CMP) was performed for 2 hours using a silica-based slurry. The thickness of the GaN substrate was evaluated at five points in plane using a contact-type height gage. The average surface roughness was measured using atomic force microscopy (AFM).

Fig. 4 shows microscope images of GaN substrate after backgrinding and CMP. Table III summarizes the thickness uniformity of GaN substrate after backgrinding and CMP. A target thickness of 145 µm and an excellent thickness uniformity within ±0.6% was obtained after backgrinding. In addition, the processing controllability was stable with regard to the three processed wafers. However, the backgrinding resulted in cracks on the wafer edge as shown in Fig. 4 (a). In our previous experience with SiC backgrinding, such edge cracks did not appear; this is because SiC substrate is less brittle than GaN substrate, and the wafer edge became knife-shaped due to backgrinding as shown in Fig. 5.

After CMP, the GaN substrate was etched to 10 µm. Although the thickness uniformity deteriorated to some extent, the edge cracks disappeared as shown in Fig. 4 (b). This implies that the thickness at the edge was less than 10 µm. Consequently, an excellent surface morphology with an average surface roughness of less than 0.2 nm was obtained as shown in Fig. 6.

TABLE III THICKNESS UNIFORMITY OF A 2-INCH GAN SUBSTRATE AFTER BACKGRINDING AND CMP

Sample	After backgrinding		After CMP	
	Average (µm)	Uniformity (±%)	Average (µm)	Uniformity (±%)
#A	145.2	0.41	135.0	1.15
#B	144.9	0.55	134.5	1.08
#C	145.7	0.41	135.3	1.26

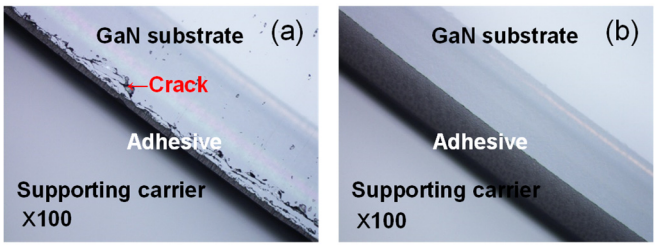

Fig. 4 Microscope images of GaN substrate: (a) after backgrinding and (b) after CMP.

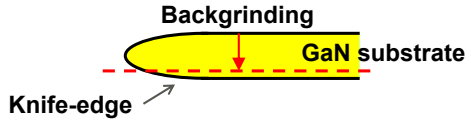

Fig. 5 Schematic cross-section of GaN substrate edge.

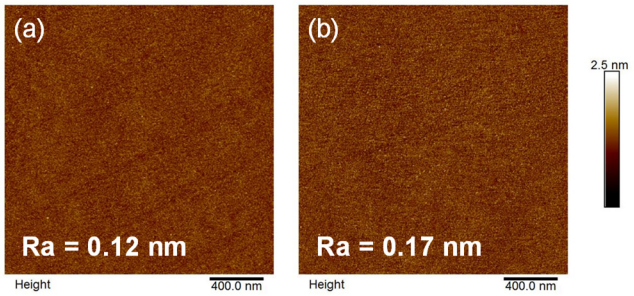

Fig. 6 AFM images of GaN substrate after CMP: (a) center and (b) top.

DICING OF GAN SUBSTRATE

After Ti/Au was deposited on the backside of the thinned GaN substrate by sputtering, dicing was performed. We compared normal vitrified bond blade dicing and ultrasonic-wave (US) blade dicing, which is effective for SiC substrate. The widths of the normal blade and US blade were 200 and 50 µm, respectively. A chip elongated along the <11–20> direction with a size of 5 mm × 2 mm was cut out as shown in Fig. 7. The chipping was evaluated using an optical microscope and scanning electron microscope (SEM).

Fig. 8 illustrates a comparison of normal blade dicing and US blade dicing for the GaN substrate. The result of the normal blade dicing was better than that of the US blade dicing. For normal blade dicing, an average chipping of within 30 µm was obtained. For US blade dicing, the vibration of the blade seemed to impact mechanical stress on the brittle GaN substrate. However, both dicing methods considerably wasted the expensive GaN substrate.

Therefore, we tried stealth dicing (DISCO Corporation), which involves damaging the crystal using laser, and then the crystal is expanded to separate the chips. Fig. 9 shows optical microscope and SEM photographs of 100 µm-thick GaN substrate without backside metal after stealth dicing. There was almost no chipping, and the cutting surface was smooth. Although the metal on the cutting line needs to be removed to separate the chips, stealth dicing is effective for GaN substrate.

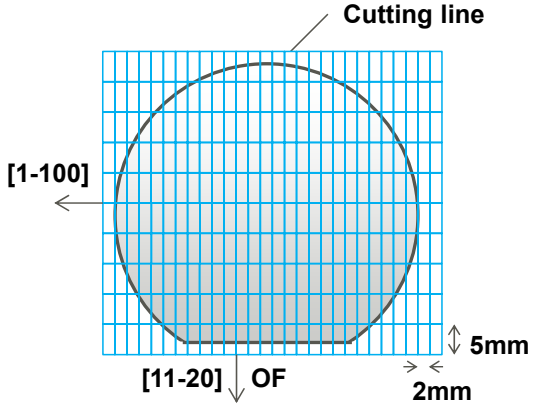

Fig. 7 Dicing map for GaN substrate.

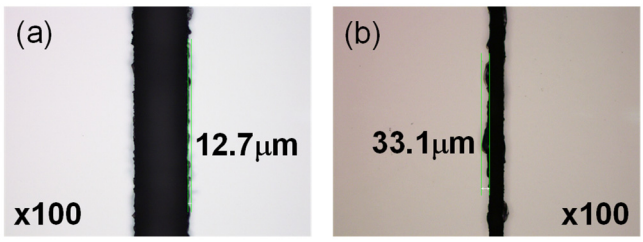

Fig. 8 Comparison of dicing methods for GaN substrate: (a) normal blade dicing and (b) US-blade dicing.

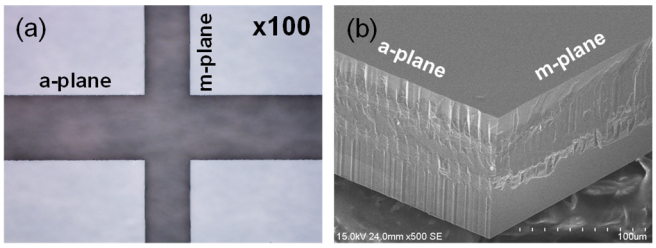

Fig. 9 Photographs of 100-μm thick GaN substrate without backside metal after stealth-dicing: (a) optical microscope and (b) SEM.

CONCLUSIONS

The authors optimized the thermal management of RF GaN-on-GaN HEMTs using thermal simulation. The temperature rise was found to be minimum at a substrate thickness of 100 μm. In addition, GaN-on-GaN has a higher potential of thermal management than GaN-on-SiC by increasing heat source spacing to more than 40 μm. From these results, we developed a method for backside processing of GaN-on-GaN. The utilized GaN substrate could be thinned to less than 150 μm by backgrinding, and an average surface roughness of less than 0.2 nm was obtained by CMP. Furthermore, the thin GaN substrate could be cut within an average chipping of size 30 μm using normal blade dicing, but stealth dicing was found to be more effective for GaN substrate.

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ACRONYMS

HVPE: Hydride vapor phase epitaxy
VAS: Void-assisted separation
CMP: Chemical-mechanical polishing
AFM: Atomic force microscopy
US: Ultrasonic-wave
SEM: Scanning electron microscope