The State-of-Art of GaN/Diamond HEMT Manufacturing Technology And Device Performance

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Abstract

This paper describes the progresses made in manufacturing technology of 4 inch GaN/Diamond HEMT wafers in a compound semiconductor foundry since data reported a year ago [1]. Wafer thickness uniformity and wafer flatness of starting GaN/Diamond wafers have improved greatly, which contributed to improved processing yields. By optimizing laser drilling techniques, a through-substrate-via process was successfully demonstrated, which is the last hurdle in GaN/Diamond manufacturing technology. To fully exploit diamond's superior thermal property for GaN/HEMT devices, an AlN containing barrier was included in the epi structure, in addition to conventional AlGaN barriers. On this wafer, an output power density of 22.5W/mm at Vds=100V was obtained from on-wafer load pull measurements. To our knowledge, this is among the highest output power densities ever reported for GaN HEMT devices at Vds =100V.

INTRODUCTION

GaN-based HEMT technology has been gaining momentum in various commercial and military applications. 50V CW applications with >10W/mm saturated output power density are fairly common. A >100V S-band 200W discrete transistor has been demonstrated recently [2]. With the increasing operating voltage and power, heat dissipation becomes the key technological barrier hindering further progress of GaN-based RF transistors. On the other hand, researchers have utilized recent advances in CVD diamond technology and successfully demonstrated enhanced thermal and RF performance on GaN/Diamond HEMT devices. For example, the operating junction temperature was reduced by 40-45% and the areal RF power density compared to GaN-on-SiC, was tripled [3]-[5].

With high volume commercial applications in mind, GCS and RFHIC set out to develop a manufacturing process using compatible, fully automated 4 inch tools to fabricate GaN/Diamond HEMT in a compound semiconductor production facility starting 2 years ago. This paper, will discuss progresses made on 4 inch GaN/diamond wafer manufacturing technology, including (1) improvements made on wafer flatness and thickness uniformity, (2) challenges and solutions in adoption of an AlN containing barrier in epi structure, and (3) through-substrate-via (TSV) process development and characterization. We will also report a record output power density result from on-wafer load pull measurement obtained from a sample GaN /Diamond wafer.

GAN/DIAMOND MANUFACTURING TECHNOLOGY PROGRESSES

A. Improved wafer flatness and thickness uniformity

In this work, GaN/Diamond epi wafers were provided by RFHIC and then processed at GCS using the existing 4 inch GaN/SiC and GaN/Si standard production line. Last year, typical diamond substrate thickness variation from 100 to 135 um was typical, additionally, wafer warpage can be several hundreds of microns to a few millimeters. This made wafer handling by automated fab tools very difficult and resulted in high wafer breakage rates. Wafer bowing and poor thickness uniformity presented extraordinary challenges to the steppers, especially at the gate lithography step where target CDs of 0.5um are required.

The CVD diamond team has since made significant improvements. The recent batches of GaN/Diamond wafers have shown thickness uniformity $\leq$ 15 um and wafer bowing < 100 um, which reduced handling related wafer breakage rate significantly. Examples of wafer thickness variation and wafer bowing measurement results and their impact on wafer processing yield will be discussed.

B. Challenges and solutions in adopting AlN containing barrier in epi structure

In order to fully exploit diamond substrate's superior thermal properties, an AlN containing barrier wafer was included, enabling higher current (and therefore power) density targets. However, the ohmic contact resistance obtained from the first trial using our standard ohmic process produced high contact resistance. To resolve the

issue, a separate ohmic optimization DOE samples were run on other AlN containing barrier wafers (on Si substrates). The optimized ohmic contact results are shown in Figure 1, where a recess etch was introduced before ohmic metallization. The optimized process was

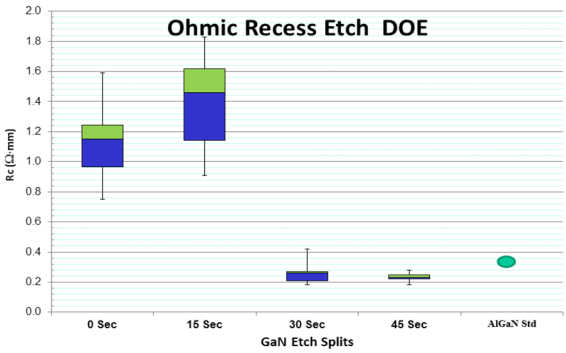


Fig. 1 Ohmic contact resistance (Rc) optimization DOE results from AlN barrier test wafers, where recess etch time was varied while standard ohmic metal was used.

then implemented on AlN containing barrier diamond wafers. Other parts of the process remained the same as standard AlGaN barrier wafers. Low contact resistance is one of the key factors for the excellent output power performance reported in the later sections.

C. Through-substrate-via (TSV) development

Laser drilling technique was used to make through-substrate-vias (TSVs) in diamond substrates. Optimization of laser power, drilling speed and drilling entry from front vs back of wafer, was critical in forming damage-free TSVs.

Subsequent metallization to form the ground connection in a through hole (with both ends open) represents unique challenges. A special photoresist coating process was needed to partially fill the through holes prior to seed metal sputtering and electroplating to insure proper ground connection to the back of the die.

In fact, to form proper ground connections in diamond substrates, the first attempt drilled 1/3 the distance down from the wafer front side and fill the drilled holes with thick plated metal. Then we would drill from backside and hoping to stop in the middle of the metal fill. This approach, however, was not successful due to the fact that laser drilling from backside was not able to stop in the middle of metal fill.

Our second attempt was to drill from backside and plate a thick metal from backside followed by front side patterning and air bridge formation. However, the rough backside surface not only caused alignment difficulties, but also caused excessive scattering of the laser light, producing inconsistent and unpredictable results.

The third attempt, drilled from the front side all the way through the substrate, followed by front side airbridge formation with thick metal plating. Once the front side metallization and though holes are formed, the backside metallization would just follow the standard process steps. With third method, with properly optimized laser intensity and drilling parameters, a successful TSV formation and fully functional multi-finger devices with internal slot vias on a GaN/ Diamond wafer was demonstrated. Figure 2 shows the schematics of the three different approaches that were attempted.

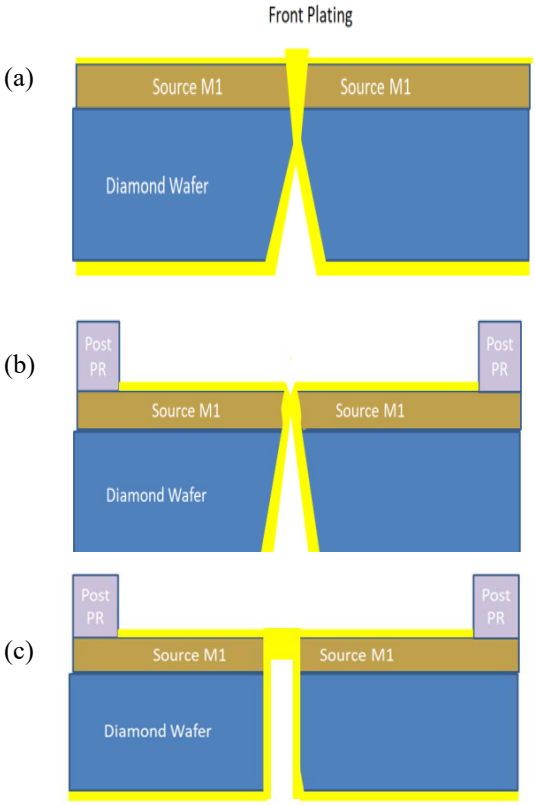
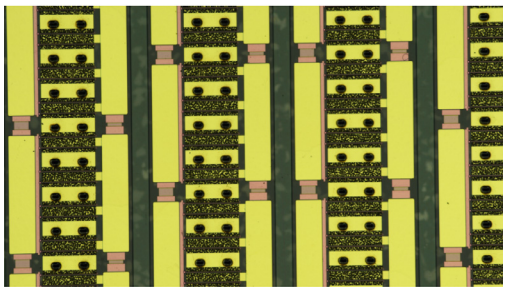


Fig. 2 Schematic diagram of 3 backside via approaches: (a) Drilling from both sides, (b) drilling from backside and (c) drilling from front side.

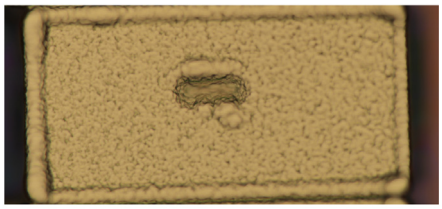
Figure 3 shows results of laser drilling from the backside where the roughness of diamond substrate back surface presented extrordinary difficulties.

Fig. 3. Results of laser drilling from the backside where the roughness of diamond substrate back surface is evident.

Figure 4 shows front side drilling results and subsequent Au plating filling the TSV while forming air bridges.



(a)



(b)

Fig. 4. (a) Front side drilling patterns and (b) subsequent Au plating filling the TSV while forming air bridges.

WAFER LEVEL DEVICE MEASUREMENT RESULTS

RF performance of GaN-on-Diamond was evaluated on wafer, using a Maury Microwave load pull station capable of pulsing both DC and RF signal. Pulsed characterization is used because on wafer testing cannot offer the same thermal dissipation of a proper package. In fact, the high thermal conductivity diamond substrate, is kept in contact with the chuck (heat sink) only by the suction force determined by vacuum, which can vary based on wafer flatness.

Figure 5 shows the output power, gain and power added efficiency at 2 GHz for a 2 finger 300um wide device. The bias is set at 100V and 15% Idss. Pulse width is 50us and duty cycle is 10%. A load pull was run before to find the optimal impedance point for the fundamental and second harmonic. In the aforementioned conditions, the power saturated at 41.3 dBm, corresponding to 22.5 W/mm in power density.

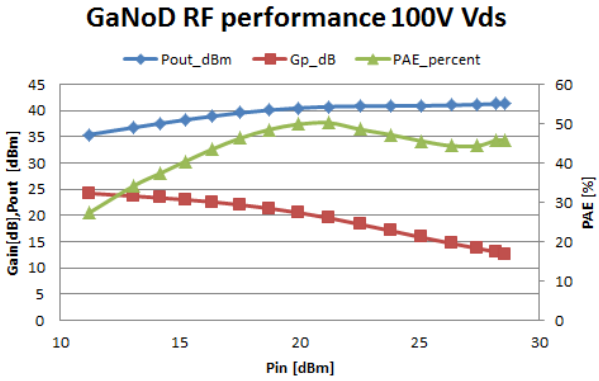


Fig. 5. Wafer level power sweep results from a 4 inch GaN/Diamond wafer measured at front side completion. Test condition: frequency 2GHz, Vds=100V, 15% Idss, 50µs pulsed width, 10% Duty Cycle, F0 and F2 load tuned for maximum power. DUT: 2x300um. Psat=41.3 dBm and power density is 22.5W/mm.

After back vias were drilled, devices with multiple fingers were tested. Figure 6 shows the output power, gain and power added efficiency at 2 GHz for a 10 finger 80um wide device. The measurement conditions were similar to the on wafer test, however, the impedance was tuned to maximize the output power of the new layout. Under this condition, a saturated power (Psat) of 40.6 dBm was measured, corresponding to a power density is 14.3W/mm.

Performance of the multi-finger device appears to be degraded somewhat compared to the 2x300 device. As mentioned above, this can be attributed to the heat produced by laser drilling of the vias, as well as laser energy scattered during the same process. Nevertheless, the considerable power density confirms that back vias have been formed for all fingers of the device, providing solid evidence of successful back via formation.

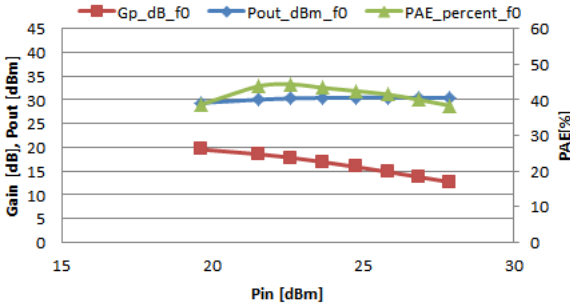


Fig. 6. Wafer level power sweep results from a 4 inch GaN/Diamond wafer measured on after back vias. Test condition: frequency 2GHz, Vds=100V, 15% Idss,50µs pulsed width, 10% Duty Cycle, F0 and F2 load tuned for maximum power. DUT 10x80um. Psat=40.6 dBm, power density is 14.3W/mm.

CONCLUSIONS

GCS-RFHIC team continued to make significant progresses in GaN/Diamond manufacturing technology, including improving diamond wafer thickness uniformity and flatness, completing development of backside via processes and demonstrating improved device performance. On a special epi wafer with AlN containing barrier, we obtained 41.3 dBm from a 2x300 um device under a 2 GHz wafer-level pulsed load-pull test when biased at 100V and 15% Idss, corresponding to an output power density of 22.5 W/mm. This is among the highest power densities ever reported for GaN HEMT devices in this Vds range underscoring the potential of GaN/Diamond technology for high power density applications.

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