3D Nanoprinting of Grayscale Features in GaN Devices to Reduce Peak Electric Fields

Andrew D. Koehler[1], Geoffrey M. Foster[2], James C. Gallagher[2], Joseph G. Tischler[1], Travis J. Anderson[1], Karl D. Hobart[1], Fritz J. Kub[1]

[1]U.S. Naval Research Laboratory, Washington DC 20375, USA, andrew.koehler@nrl.navy.mil 202-404-6788
[2]ASEE Postdoctoral Fellow Residing at NRL, Washington, DC 22310, USA

Keywords: GaN, 3D nanoprinting, junction termination extension, grayscale lithography

Abstract

3D nanoprinting by two-photon polymerization of photoresist is used to form grayscale features on GaN devices to mitigate electric field crowding. Reduction in electric field crowding and therefore reduction in peak electric field will result in increased breakdown voltages. An example is reducing the peak electric field at the semiconductor surface of vertical GaN devices using a bevel-edge junction termination extension (JTE). The bevel-edge JTE is formed by transferring a 3D nanoprinted resist profile into the GaN using Cl_2 inductively couple plasma (ICP) reactive ion etching (RIE). Bevel-edge JTEs on GaN PN diodes are performed using a negative termination schemes. Plasma damage from the ICP RIE on the etched beveled edges will be mitigated using various treatments, to produce a high quality surface on the bevel-edge JTE.

INTRODUCTION

GaN high power devices show promise for future highly efficient power converters, where 3.7 kV GaN PN diodes have already been shown [1]. However, the intrinsic benefits of GaN can be limited by high electric field regions in vertical GaN devices. This is due to electric field crowding, which reduces the breakdown voltage compared to the maximum theoretical value and ultimately limits the reliability of these devices. Conventional photolithography results in binary definition of features, where abrupt corners at the junction edge can result in electric field crowding. However, grayscale lithography can define sloped features in the photoresist, which can then be transferred to the device structure, thereby mitigating peak electric fields at the edges. Grayscale features have previously been demonstrated with a binary photomask separated from the sample with a spacer [2]. However, this process is challenging to reproduce and is difficult to customize the taper angles needed to achieve a correct bevel edge.

Maskless 3D nanoprinting lithography via a two-photon polymerization of photoresist process, allows for patterning of arbitrary 3D shapes into resist [3]. The Nanoscribe Photonic Professional GT enables 3D micro and nano structures to be patterned in resist based on the concept of "direct laser writing". The Nanoscribe will be used to for developing grayscale features to reduce peak electric fields in GaN PN diodes. A grayscale negative bevel termination, where the area of the junction increases when going from the highly doped side toward the lightly doped side, is used to reduce the peak surface field by extending the depletion region at the junction edge to reduce electric field crowing [4]. Conventional bevel-edge termination of SiC power devices is performed by using a dicing saw at an angle, which can result in significant damage [5]. The grayscale processing of bevel-edge JTE is a process that can result in significantly less crystal damage than sawing, and therefore improved performance. In addition, this process does not require device singulation to bevel the edges and makes homogeneous integration possible. Details on the process development and device results will be discussed.

EXPERIMENT

To demonstrate the potential of the 3D nanoprinting technology for vertical GaN power devices, GaN PN diode epitaxy is grown on native GaN substrates by metal organic chemical vapor deposition (MOCVD) on a freestanding

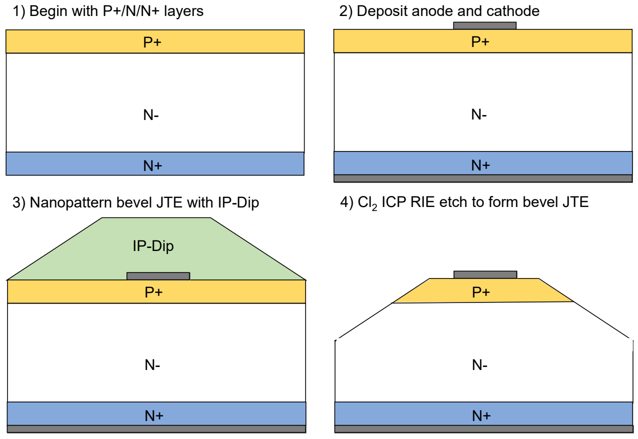

Fig. 1. Schematic cross-sections of the fabrication process to form bevel edge JTE using 3D nanopatterning to form the grayscale features.

hydride vapor phase epitaxy (HVPE) GaN wafer. The P-type region is doped to ~1x10^{18} cm^{-3} with a thickness of 400nm. The N-type region is doped to ~1x10^{16} cm^{-3} (measured by $1/C^2$ analysis) with a thickness of 10um.

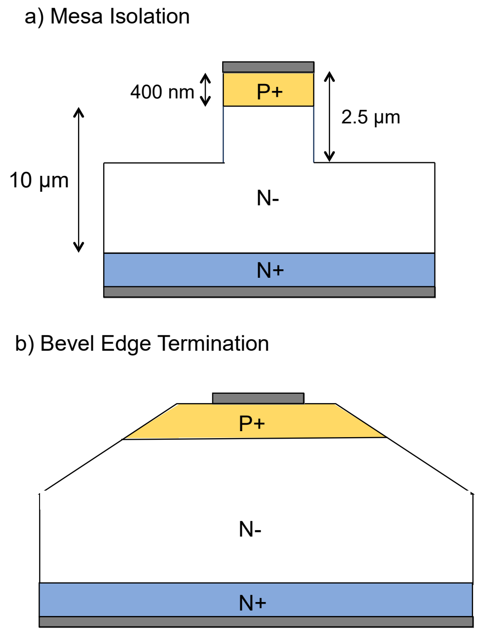

Fig. 2. Vertical GaN PN diodes with a) mesa isolation and b) bevel edge termination schemes.

Vertical GaN PN diodes are fabricated by first evaporating Ti/Al/Ni/Au on the backside of the N+ GaN substrate and annealing at 800C in N2 to form the cathode contact. Lifting off circular Pd/Pt/Au contacts to the P-type region forms the anode. Then, IP-Dip photoresist is 3D nanoprinted to serve as the etch mask for Cl_2 inductively coupled plasma (ICP) reactive ion etch (RIE). As shown in Figure 2, mesa isolated and bevel-edge terminated devices are investigated.

RESULTS & DISCUSSION

Designing appropriate height bevel structures in IP-Dip, required the etch selectivity between the GaN and IP-Dip to be determined. The Cl_2 etch consisted of 10 sccm of Cl_2 and 5 sccm of Ar at 5 mT. The RF power was 40 W and ICP power was 150 W and the etch took place at 25 C. The etch rate of test GaN was determined to be 86 nm/min. The etch rate of the IP-Dip photoresist was calibrated using optical profilometry of 3D nanoprinted pillars of various heights before and after Cl_2 ICP RIE. An example of the pillars before etching is shown in Figure 3. The IP-Dip etch rate was determined to be 102 nm/min IP-Dip. A bevel-edge angle of 1.80 deg was determined to reduce the surface field by 50%.

On the PN diode wafer, the actual bevel angle was found to be 1.06 deg, as shown in Figure 4. Atomic force microscopy (AFM) was used to measure the bevel angle of the bevel JTE after ICP RIE etching the printed IP-Dip. The actual etch rate of the GaN was 61 nm/min explaining the smaller angle than designed.

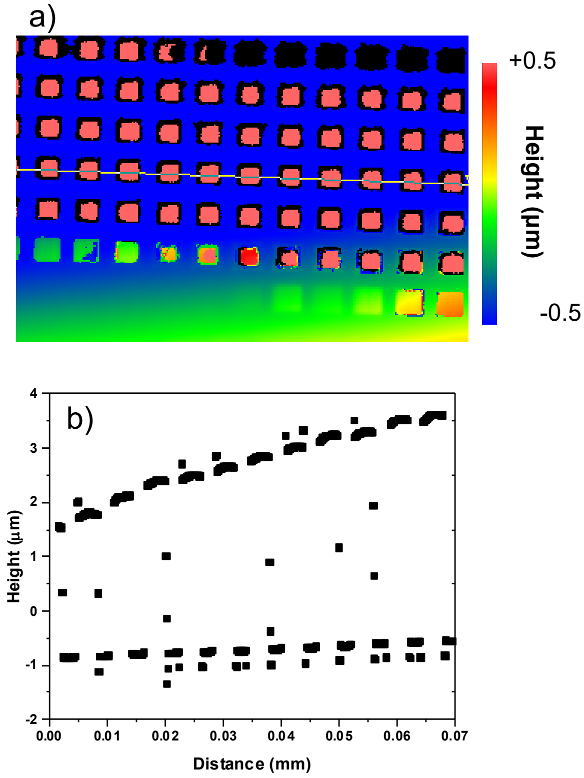

Fig. 3. a) 3D optical profilometer image of pillars used for etch rate characterization and b) line scan of pillar heights before Cl_2 etching.

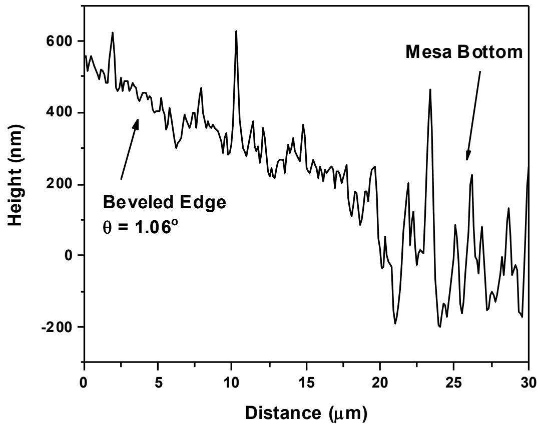

Fig. 4. Atomic force microscopy (AFM) image of bevel edge, showing angle of 1.06 deg.

The PN diodes were characterized in both the on-state and off-state. The low voltage characteristics are shown in Figure 5. The Mesa isolation device exhibits higher leakage current in the off-state, and some noise in the forward conduction characteristics indicative of charge trapping. The bevel-edge terminated PN diode has lower off-state leakage and a smooth turn-on.

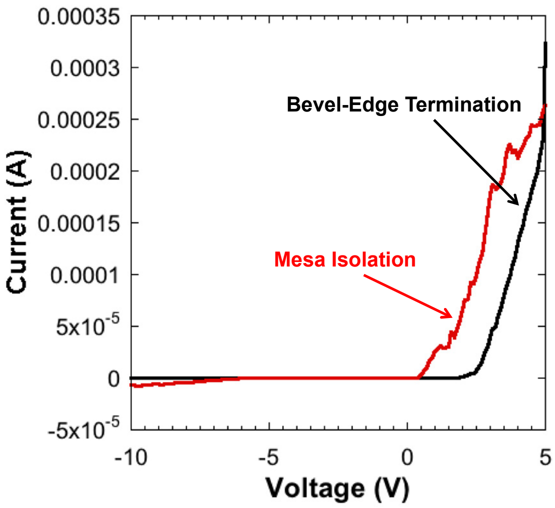

Fig. 5. Current-voltage characteristics of PN diodes with bevel-edge termination and no termination.

The breakdown voltages of the PN diodes were characterized in a vacuum probe station to prevent surface flashover. The breakdown voltage of the mesa-isolated PN diode ranged from 90 V to 140 V. Whereas, the bevel-edge terminated PN diode device exhibited breakdown ranging from 390 V to 420 V. This is a significant improvement in breakdown voltage observed in the bevel-edge termination scheme due to reduced surface electric field. Since the breakdown voltage is still relatively low, for the designed epitaxial layer thickness and doping density. The breakdown is likely still limited by defects. Although there are defects that lead to premature catastrophic failure, the improved termination and field management in the bevel-edge device can extend the breakdown voltage compared to a mesa-isolated device.

Plasma damage cleanup process will be developed and applied to the GaN PN diodes to remove damage caused from ICP RIE. This will aid in mitigating surface leakage currents along the bevel-edge termination. Experiments were performed on test samples to show the benefits of . After etching, the roughness over both short and long ranges was determined by atomic force microscopy. From the results, we determined that degradation in surface quality can be recovered by 500 °C rapid thermal anneal, a TMAH etch. In addition, Raman spectroscopy is used to interpret the etch damage by analysing the E_2 peak, which is related to crystal stress [6,7]. As shown in Figure 6, the TMAH recoverey can lessen the damage caused by the Cl_2 ICP RIE, and this technique will be applied to the PN diode devices.

SUMMARY

3D nanoprinting is demonstrated to form grayscale bevel edge termination on vertical GaN PN diodes to mitigate electric field crowding. The breakdown voltage of the PN diode was improved using the bevel-edge JTE compared to a mesa isolated PN diode. Breakdown was limited by defects in the epitaxial films. However, the bevel termination improved the breakdown voltage. Further improvement can be expected upon plasma damage cleanup to the edge surface.

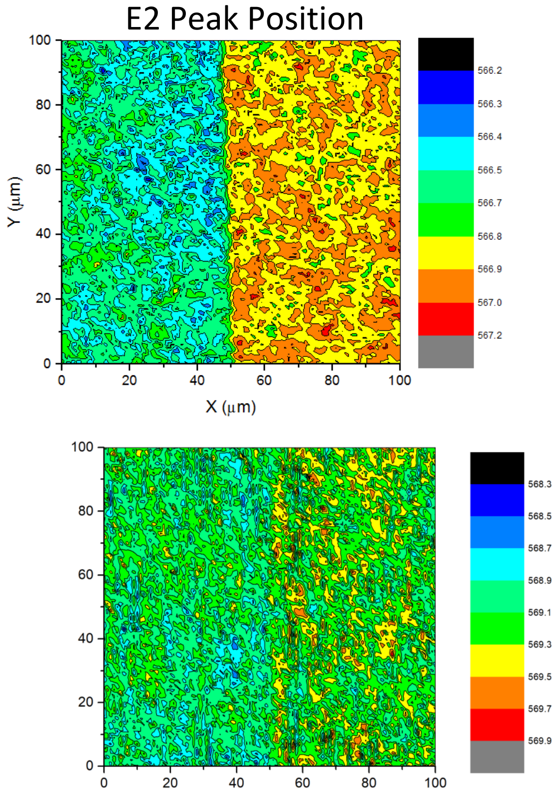

Fig. 6. Color maps of peak position for the E_2 peak of GaN surface with unetched reference on left side and plasma etched on right (top) and after a treatment of TMAH (bottom), showing recovery of the E_2 Raman peak position.

REFERENCES

1. I. Kizilyalli, A. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney. “3.7 kV Vertical GaN PN Diodes”, IEEE Elec. Dev. Lett. Vol. 35, No. 2, 2014.
2. E. Imhoff, F. Kub, K. Hobart, M. Ancona, B. VanMil, D. Gaskill, K. Lew, R. Myers-Ward, and C. Eddy, Jr., “High-Performance Smoothly Tapered Junction Termination Extensions for High-Voltage 4H-SiC Devices” IEEE Trans. on Elec. Dev. Vol. 58, No. 10, 2011.
3. N. Anscombe, “Direct laser writing” *Nature Photonics* vol. 4, pages22–23 (2010)

4. J. Balagia, “Power Semiconductor Devices” ISBN-13: 978-0534940980, 1995.
5. W. Sung, B. Baliga, and A. Huang, F “Area-Efficient Bevel-Edge Termination Techniques for SiC High-Voltage Devices” IEEE Trans. on Elec. Dev. Vol 63, No. 4, 2016.
6. M. Kuball, M. Benyoucef, B. Beaumont, P. Gibart, Stress at the Coalescence Boundary of Epitaxial Lateral Overgrown GaN, Phys. Status Solidi Appl. Res. 188 (2001) 747–750.
7. M. Kuball, Raman spectroscopy of GaN, AlGaN and AlN for process and growth monitoring/control, Surf. Interface Anal. 31 (2001) 987–999.