200 V – 20 A AlGaN/GaN MIS-HEMTs on Silicon Substrate with 60 mm Gate Width

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Abstract

In this paper, we utilized AlGaN/GaN heterostructure grown on the silicon substrate to fabricate high current high-electron-mobility transistors (HEMTs). The D-mode MIS-HEMT has gate width (W_G) of 60 mm and an Al_2O_3/SiO_2 bilayer as both gate dielectric and surface passivation. The fabricated HEMT shows a saturation current (I_{DS}) of 21.1 A, an on-resistance (R_{on}) of 0.22 Ω, threshold voltage (V_{TH}) of -9 V, and breakdown voltage (V_{BR}) of 212 V. The high I_{DS}, low on resistance, and moderate breakdown voltage characteristics show the potential and advantages of GaN MIS-HEMT for power applications.

INTRODUCTION

With the development of power electronics technology, high temperature, high efficiency, and high power density are becoming the key metrics for power applications. Wide bandgap (WBG) semiconductor devices such as the Gallium Nitride (GaN) transistors have been recognized as a promising alternative for state-of-the-art power switches. Recently, the lateral GaN High-Electron-Mobility Transistor (HEMT) has shown superior performance [1] as compared to Si devices. For power applications, it is important to reduce the gate leakage current to minimize the power consumption in the OFF-state. For this reason, the structure of metal–insulator–semiconductor HEMT (MIS-HEMT) is beneficial for low leakage current design [2,3]. Normally, Al_2O_3, SiN_x, and SiO_2 are common dielectrics which are often used as gate oxide and passivation layer. Furthermore, the GaN HEMT manufactures are reducing the cost of GaN HEMT by switching to the GaN-on-Si technology and starting mass production of GaN HEMT. At the same time, the reliability of the GaN HEMT is emphasized by both the industrial and academic researchers from all aspects, including the device fabrication technology, test method, and new standards [4,5].

In this article, we demonstrate a concept for robust GaN-on-Si MIS-HEMTs using Al_2O_3 as gate dielectric and SiO_2 as passivation layer. This device structure with the chosen gate dielectric and passivation layers, results in improved device characteristics, stable breakdown voltages, and low forward-bias gate and drain leakage currents. In order to make the AlGaN/GaN HEMT into a large-current device, the gate widths (W_G) of 200, 500, 1000, 1500, and 2000 μm were designed to analyze the forward- and reverse-bias characteristics for a single HEMT. Afterwards, multi-finger design, which has the total width 60 mm, was used to achieve 20 A high current characteristics

DEVICE STRUCTURES AND FABRICATION

Figs. 1(a) and (b) shows the schematic cross section and top view of the fabricated GaN power HEMT grown on a low-resistivity silicon substrate by metal-organic chemical vapor deposition (MOCVD). The device structure consists of a 5.0 μm GaN buffer layer, a 500 nm channel GaN layer, a 1 nm AlN spacer layer, a 25 nm $Al_{0.22}Ga_{0.78}N$ barrier layer, and a 2 nm GaN cap layer. By Hall measurement, using a standard van der Pauw geometry with 1 × 1 cm^2 of as-grown epitaxial materials, an electron mobility of 1887 cm^2/V-s and a sheet charge density of 1.25 × 10^{13} cm^{-2} were obtained at room temperature. To fabricate AlGaN/GaN MIS-HEMTs, the process started with mesa isolation by using inductively coupled plasma reactive ion etching (ICP-RIE) to an etching depth of ~ 200 nm with chlorine gas. The source and drain ohmic contacts consisting of multilayer metals Ti/Al/Ti/Au (30/120/40/60 nm) were deposited next by E-beam evaporation and subsequently annealed in nitrogen ambient for 30 s at 850 °C by rapid thermal annealing (RTA). The contact resistance (R_C) and sheet resistance (R_{sh}) were 1.64 × 10^{-4} Ω-cm^2 and 331 Ω/□, respectively, obtained by transmission line measurement (TLM). After the formation of ohmic contact, Al_2O_3 used as gate dielectric was deposited by plasma enhanced atom layer deposition (PEALD) at 250 °C. The source and drain areas were then fabricated by CF_4 dry RIE etching to open the first contact window. The gate metal, Ni/Au (30/300 nm) was deposited by thermal evaporator. The source, drain, and gate areas were then formed by CF_4 dry etching in RIE mode to etch the second contact window. Eventually, the pad metal, Ti/Au (10/800 nm) was deposited with by thermal evaporator. MIS-HEMT fabricated in this study has a gate length (L_G) of 4 μm, an electrode spacing of gate-source (L_{GS}) of 2 μm, and an electrode spacing of gate-drain (L_{GD}) of 10 μm. The DC measurements were performed by Keysight B1505A semiconductor device parameter analyzer with high-voltage and dual high-current source measure units (HVSMU and DHCSMU). The characteristics, including the forward current-voltage (I-V) as well as reverse

gate leakage current and off-state breakdown voltage were measured on the Cascade Microtech Tesla probe station. This probe station provided a well-shielded black cabinet to eliminate the static signal and disturbance from environmental light. For breakdown voltage measurement, the sample was covered with fluorinert electronic liquid (FC-40) to prevent the electric arc under high electric field.

Results and Discussion

A. Different layout design of MIS-HEMT

In this section, we discuss the device characteristics of the single MIS-HEMTs with different gate widths (W_G) of 200, 500, 1000, 1500, and 2000 μm. From Fig. 2, it is observed that as W_G increases, there do not much change in the off-state drain leakage current ($I_{DS,OFF}$), gate leakage current (I_{GS}), and threshold voltage (V_{TH}). For example, when V_{GS} = 1 V, J_{GS} is in the order of magnitude below 10^{-7} A, ON/OFF ratio is also more than the order of magnitude of 10^6. Nevertheless, when gate width goes up, the drain current (I_{DS}) increases, but not linearly, and reaches 800 mA at W_G = 2000 μm at V_{GS} = 1 V, as shown in Fig. 3(a). The saturation current density (J_{DS}) decreases with increasing W_G, as shown in Fig. 3(b). The reason is attributed to thermal heating. As the device size becomes larger, although the drain current increases, the channel temperature raises up as well, which would lead to degrade the drain current density [6]-[8]. Figure 4 shows the breakdown characteristics evaluated for an MIS-HEMT with different gate widths. The criterion of breakdown voltage is defined as the voltage at which the drain current goes over 0.1 mA/mm. Therefore, the optimum design of gate width is W_G = 2000 μm, and the single HEMT exhibits the drain current of 800 mA, on-resistance (R_{on}) of 13 Ω-mm, threshold voltage of -9.5 V, transconductance (G_m) of 45.5 mS/mm, gate leakage current of 3.6 x 10^{-8} A, and breakdown voltage (V_{BR}) of 555 V. Although the saturation current density (J_{DS}) decreases, J_{DS} still maintains above 400 mA/mm. So the design of high current HEMT will use W_G = 2000 μm as the basic device layout.

B. High current MIS-HEMT with multi-finger design

The MIS-HEMT with the total gate width of 60 mm is used as the standard device for the high-current measurement. Transfer characteristics (I_{DS}-V_{GS}) are shown in Fig. 5. The threshold voltage, which is defined at drain current density of 1 mA/mm, is -9.2 V and the peak transconductance is 2.33 S. Fig. 6 illustrates the output characteristics (I_{DS}-V_{DS}) with V_{GS} swept from −11 to 1 V in steps of +2 V. The maximum drain current is 21.1 A that corresponds to the current density of 351 mA/mm and the on-resistance is 240 mΩ in the condion of V_{GS} = 1 V and V_{DS} = 10 V. The hysteresis measurement plotted in Fig. 7 reveals that the low surface states can be well controlled by the Al_2O_3 and SiO_2 passivation process.

Fig. 8 shows the breakdown characteristics which is defined as the drain current density at 0.1 mA/mm. The breakdown voltage of MIS-HEMT is 234 V at V_{GS} = -12 V. Furthermore, the layout design of MIS-HEMT is in parallel and thus the thermal effect must be considered. Fig. 9 shows the output characteristics measured at 25℃ and 150℃ environments. When V_{GS} = 1 V, the saturation current I_{DS} is 21.1 A and R_{on} is 0.24 Ω at 25℃, while the saturation current is 15.8 A and R_{on} is 0.43 Ω at 150℃. The degradation of drain current is 25% which is better than or comparable to other reported values [6-8].

C. Dynamic characteristics for MIS-HEMT

The heterostructure AlGaN/GaN HEMT has excellent performance in on-resistance and forward current due to inherrent polarization, however, when it is used as a switching device, some disadvantages occurs such as the increasing dynamic on-resistance. When the device is under a large bias that means high stress, electrons can easily jump and be captured by some defects. These defects form a negatively charged virtual gate between the gate and the drain, which suppresses the two-dimensional electron gas (2DEG) of the channel and increases the on resistance during the device operation. The current hasa significant drop after stress which is also called current collapse.

Hence, we monitor the phenomenon by two carrier mechanisms, one is gate lag and the other is drain lag. A pulsed I-V measurement system was used for the dynamic measurements. For the gate lag, the issue is mainly related to the surface defects which are caused by interface traps or process damages. Fig. 10(a) shows the mechanism of the gate lag measurement, which turns off the gate (V_{GS} < 0) and then supplies the gate voltage to observe the drain current variation. It means that we applied gate stress and found the current degradation [9]. Moreover, the drain lag contains the surface states and buffer layer traps. Likewise, the drain lag is close the gate terminal and applied stress on drain electrode (V_{DS} > 0) simultaneously after that, turn on the HEMT to watch the current degradation, as shown in Fig. 10(b) [10]. In the measurement environment, we used a pulse width of 50 μs, a period of 5000 μs, and a duty cycle of 1%. The gate lag degradation is 11% and the drain lag degradation is 43%, as shown in Fig. 11.

Conclusions

We have fabricated a high current MIS-HEMT with excellent performance. First, we designed the single HEMT with different gate widths and optimized the layout of W_G = 2000 μm. The MIS-HEMT exhibits the characteristics of I_{DS} = 0.8 A, R_{on} = 13 Ω-mm, V_{TH} = -9.5V, G_m = 45.5mS/mm, J_{GS}=3.6 x 10^{-8} A/cm^2, and V_{BR} = 555 V. After that, we fabricated the MIS-HEMTs with a total gate width of 60 mm, the devices have a high output current of 21.1A (J_{DS} = 351

mA/mm), a low on-resistance of 240 mΩ, perfect hysteresis, a high breakdown voltage of 234 V, and good thermal stability. Finally, the dynamic characteristics are investigated and the calculated gate lag and drain lag are 11% and 43%, respectively. The high current MIS-HEMT would be an excellent candidate for implementation in high power applications.

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REFERENCES

[1] M. J. Scott, L. Fu, X. Zhang, J. Li, C. Yao, M. Sievers, and J. Wang. "Merits of gallium nitride based power conversion," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074013, 2013.

[2] L. Li, J. Zhang, Y. Liu, and J. P. Ao, "Evaluation of a gate-first process for AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors with low ohmic annealing temperature," *Chinese Phys. B,* vol. 25, no. 3, pp. 038503-1-038503-3, 2016.

[3] T. E. Hsieh, Y. C. Lin, J. T. Liao, W. C. Lan, P. C. Chin, and E. Y. Chang, "Effect of high voltage stress on the DC performance of the Al2O3/AlN GaN metal–insulator semiconductor high-electron mobility transistor for power applications," *Appl. Phys. Express,* vol. 8, no. 10, pp. 104102-1-104102-4, 2015.

[4] S. R. Bahl, "A comprehensive methodology to qualify the reliability of GaN products," *White Paper, Texas Instruments,* 2015.

[5] C. Y. He Li, L. Fu, X. Zhang, and J. Wang, "Evaluations and applications of GaN HEMTs," *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia),* 2016.

[6] A. P´erez-Tom´as, A. Fontser`e, M. Placidi, N. Baron, S. Chenot, J. C. Moreno, and Y. Cordier., "Temperature impact and analytical modeling of the AlGaN/GaN-on-Si saturation drain current and transconductance," *Semicond. Sci. Technol.*, vol. 27, no. 12, pp. 125010-0-125010-5, 2012.

[7] W. S. Tan, M. J. Uren, P. W. Fry, P. A. Houston, R. S. Balmer, and T. Martin, "High temperature performance of AlGaN/GaN HEMTs on Si substrates," *Solid-State Electron.,* vol. 50, no. 3, pp. 511-513, 2006.

[8] W. S. Tan, M. J. Uren, P. W. Fry, P. A. Houston, R. S. Balmer, and T. Martin, "High temperature performance of AlGaN/GaN HEMTs on Si substrates," *Solid-State Electron.,* vol. 50, no. 3, pp. 511-513, 2006.

[9] N. Ramanan, "Investigation of ALD dielectrics for improved threshold voltage stability and current collapse suppression in AlGaN-GaN MOS-HFETs," *Ph. D. dissertation*, *North Carolina State University,* 2014.

[10] S. Agnihotri, S. Ghosh, A. Dasgupta, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Modeling of trapping effects in GaN HEMTs," *2015 Annual IEEE India Conference (INDICON)*, pp. 1-4, 2015.

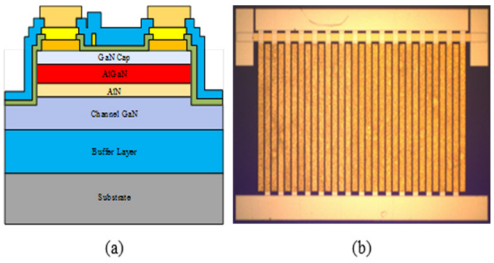

Fig.1 (a) Schematic cross section and (b) top view of the AlGaN/GaN MIS-HEMT.

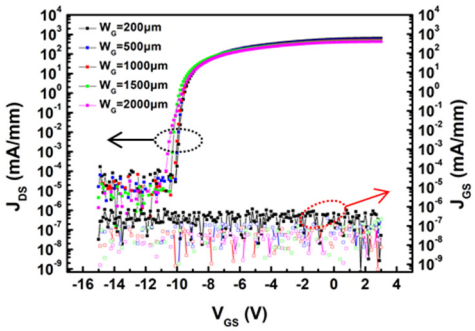

Fig. 2 Transfer characteristics of the single MIS-HEMTs with different gate widths (W_G).

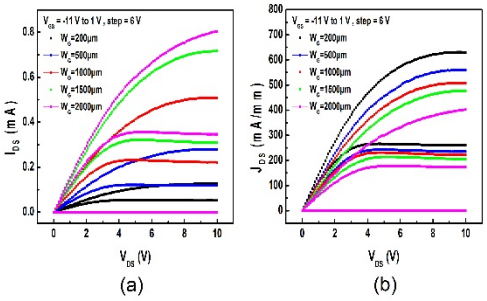

Fig. 3 (a) Output drain current (I_{DS}) and (b) drain current density (J_{DS}) as a function of drain voltage for the single MIS-HEMTs with different gate widths (W_G).

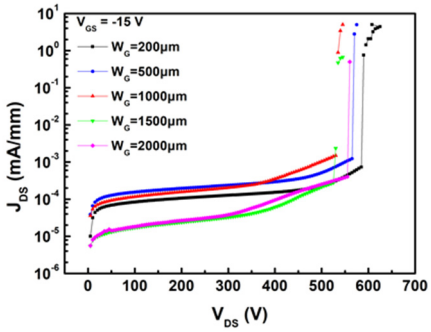

Fig. 4 Breakdown characteristics of the single MIS-HEMTs with different gate width (W_G).

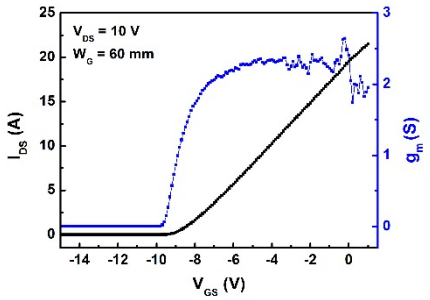

Fig. 5 Transfer characteristics (I_{DS}-V_{GS}) of the MIS-HEMT measured at V_{DS} = 10 V (the black line is transfer curve, the blue line is transconductance curve.)

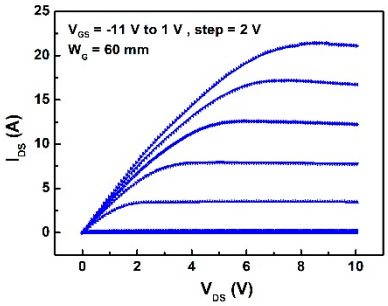

Fig. 6 Output characteristics of the MIS-HEMT with V_{GS} sweeping from -11 to 1 V.

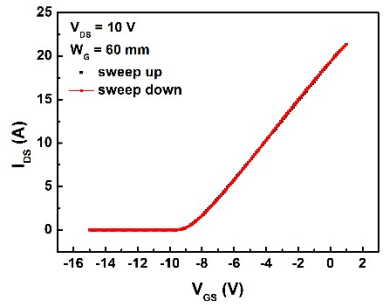

Fig. 7 Hysteresis measurement by sweeping up and down.

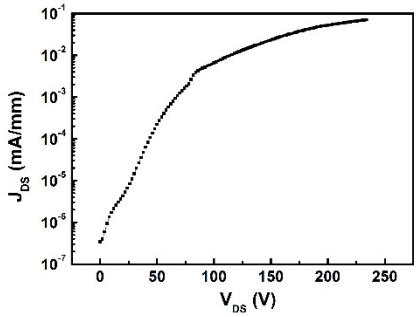

Fig. 8 The breakdown characteristics of the MIS-HEMT.

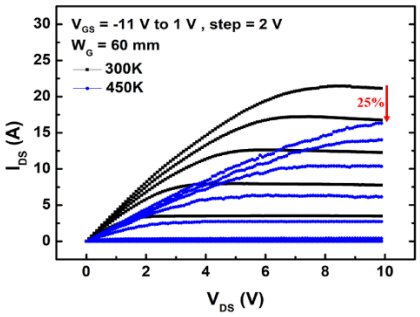

Fig. 9 The high current MIS-HEMT with W_G = 60 mm at 300K and 450K. The source to drain current at V_{GS} = 1 V only has the degradation of 25% from 300K to 450K.

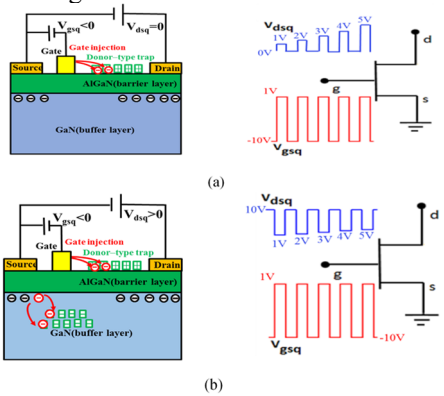

Fig. 10 Schematic diagrams of (a) Gate lag and (b) drain lag measurements.

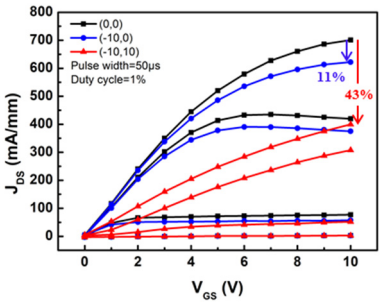

Fig. 11 The output characteristics of MIS-HEMT after different stress conditions under off-state gate lag (blue line) and drain lag (red line) to show the current degradation.

ACRONYMS

2DEG: two-dimensional electron gas
HEMT: high-electron-mobility transistor
ICP-RIE: inductively coupled plasma reactive ion etching
MIS-HEMT: metal–insulator–semiconductor HEMT
MOCVD: metal-organic chemical vapor deposition
PEALD: plasma enhanced atom layer deposition
RTA: rapid thermal annealing
TLM: transmission line measurement
WBG: widebandgap