Yield Improvement of Voltage Regulator in Next-Generation Front-End Module

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INTRODUCTION

Through detailed data analysis at the process, device, circuit, and package level, a number of factors were uncovered and steps were taken to improve yield. This paper seeks to document the productive events that took place as well as what we have learned, technical and institutional. We believe this learning can have an impact on the overall GaAs semiconductor community.

The framework of this paper is based upon the data analysis presented in [1]; it is through automatic assembly of "Big data" taken from various stages of wafer fabrication, packaging and assembly, and leveraging the data exploration capability of the Universal Data Query software to find the starting point for detailed analysis. Going further to find the root causes, we reviewed datasheets, delved into IEEE journals, re-simulated circuits in ADS, updated device-level models, and then conducted numerous meetings with different teams within and outside of the company. As many have articulated the yield improvement process in general terms [2][3][1], we will use this particular experience as a case study, to highlight the challenges we have encountered at various stages.

From the technical side, we discovered that products are failing for idle Icc, TX Pout, and Error Vector Magnitude (EVM. Using the UDQ [1] to examine packaged, KGD, PCM, and epi data, we accurately pinpointed the failure to be a voltage regulator circuit. By examining the formal interactions between wafer fab, product line, epi vendors, PDK modelers, and circuit designers, we have identified several key points which enabled yield improvement in every stage, and we further recommend ways to improve/encourage dialogue between different groups to prevent problems like this from happening in the future.

SECTION I: TIMELINE OF EVENTS THAT TOOK PLACE

In order to simplify the timeline, day 1 is defined as the approximate time the FEMs started production. This is defined as the "relative fab start day" in Figure 2 and 3.

Day 151: Product line reported to the fab that yield improvement was needed on several FEMs, mainly due to EVM problems. Product line wanted to find out if the yield loss was due to any changes from the wafer fab. Regular meetings were set up to encourage dialog between various product groups and the fab.

Day 154: The yield engineer responsible for the pHEMT technology used the UDQ to quickly find commonality between package, KGD, PCM, epi, and tool data. Details of this data analysis methodology is presented in [1], the steps taken can be summarized as follows. During wafer fabrication large amount of data were collected to monitor the many processing operations. Very valuable information is hidden in these dozens of databases, located at different servers and different formats. The UDQ allows the yield engineer to quickly download all relevant data to help answer questions such as: what PCM parameters have shifted in the recent months that can explain these FEM fails? What was the pareto of failure signatures, and do each of these parameters correlate to any KGD or PCM parameters? Once all relevant data is combined into one JMP table, outliers are filtered, followed by automated correlation procedure to find which PCM value or specific tool has a strong influence. In this particular case, one of the important package parameters was EVM and it was found best correlated with the regulator voltage (Vreg) measured at KGD. Then this process is repeated again and device Gm was found to be well correlated with Vreg (Figure 1). Since the regulator voltage is critical to the PA function, a tighter Vreg spec limit was set to improve package test yield.

Day 162: The anomalous variation of Gm was traced to a specific reactor material. The impact of Gm variation by the rogue reactor was communicated to epi vendor, and the vendor representatives became an active part of the team to improve our understanding of the issue. For the time being, epi material from that reactor was blocked from being kitted into lots. Once this short-term fix was in place, we shifted our focus to a long-term solution.
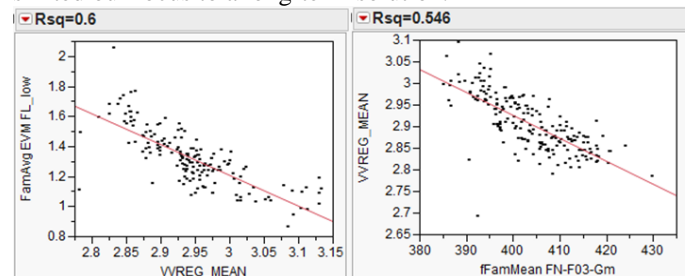

Figure 1. Correlation of package, KGD, PCM using UDQ

Day 202: By this time the yield engineer observed that while 4 FEMs have yield sensitivity with Gm, 3 other FEMs are less sensitive to Gm. Through meetings with designers and examining the circuit layouts, the main difference between the two types of FEMs was found to be the type of resistors used in the regulator. For these three FEMs, the resistor and epi contributed to Vreg variation. This additional sensitivity to resistor (Res1) was reported to both product line and process engineering.

Day 450: At this time all of these FEMs have improved yield at KGD and package levels. While we still had work to do, some of the fruits of our labor could be seen. Figure 2 and 3 summarizes the trend of the regulator voltage, Res1 and Gm. Regulator voltages from a FEM which showed sensitivity to FET Gm is labeled "FEM #1 Vreg", and "FEM #2 Vreg" is for the regulator which was sensitive to Res1. As epi and resistor process controls were tightened, FEM #1 Vreg steadily came back to target. However FEM #2 Vreg was off-target for much longer period; this was due to tightening the Res1 variation as well as re-centering, which will be explain in more detail in Section IV on process improvement.

SECTION II: YIELD IMPROVEMENT FROM EPI CONTROL

By monitoring look-ahead wafers in a growth campaign, the epi vendor makes adjustment to the growth process to make sure wafers are meeting PCM targets. Since pHEMT technologies were originally used as RF switches, epi growers and yield engineers were mostly focused on parameters relevant for that application; namely leakage current, Vpo, and Idmax. More analog-oriented parameters such as Gm were considered less important. In some situations, an adjustment to make leakage on-target resulted in making Gm off-target.
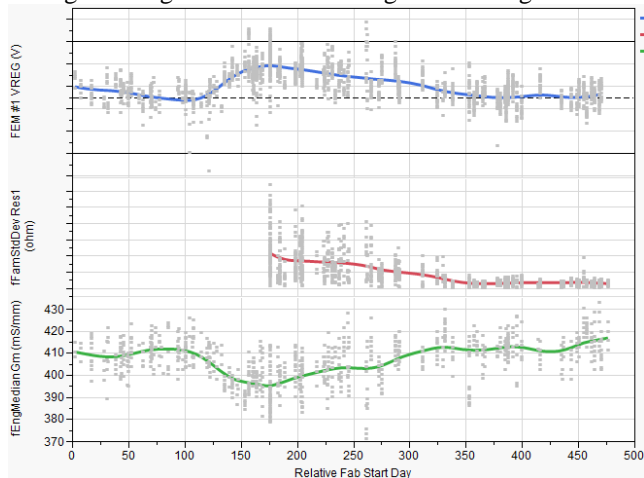

Figure 2. Trend chart of Vreg, standard deviation of Res1, and Gm, plotted against fab start day. Vreg shown in this figure was sensitive to Gm.

The link between Gm and epi growth became very clear after a series of meetings internally as well as with epi growth engineers. Various past DOE lots and previous

excursions were reviewed, as well as recent epi data. The DOEs provided epi vendor critical info for them to control their growth process (Figure 4). Epi growth engineers also spent considerable effort on their end to scrutinize every step of the growth process and identify possible inconsistencies. One of the changes made was that the flow of gases was more rigorously monitored.
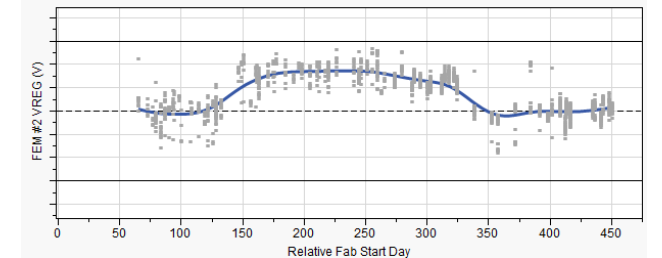

Figure 3. Trend chart of Vreg plotted against fab start day. This Vreg is different from Figure 2 since the circuit design was different.
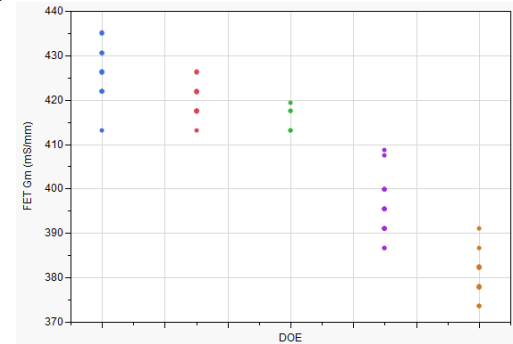

Figure 4. pHEMT Gm sensitivity observed in a DOE.

SECTION III: DEVICE MODELING AND CIRCUIT DESIGN

Ideally the process variation of a technology should be accurately reflected in the model, such that designers can simulate how the process variation will impact production circuits. In effect an inaccurate model increases the liability of the fab to final yield loss. Usually Monte Carlo process models are in place by the beta stage of the technology development.

An effective way of measuring model accuracy would be to simulate the entire PCM test, and benchmark against actual PCM data. If the fab is concerned about variation of certain parameters (ie Vpo or BVgdo) to measure them and place spec limits on them, they need to be reflected in the model. About some 20 PCM parameters were simulated simultaneously and compared against actual data.

To compare simulation and actual PCM data, individual pHEMT site data were collected through the UDQ. A JMP script was writen to convert PCM JMP tables into an ADS Citi format, so that simulation and PCM data could be compared together.

During this exercise, the D-mode FET model was found to be off-target. This discrepancy in the D-mode FET model was reported and corrected by the modeling team. Afterwards Monte Carlo's statistical capabilities

were added to the design kit, and care was taken to model the Gm variation seen in the process. The epi DOE results indicated that the Gm variation was due to the source degeneration effect, whereby the intrinsic Gm was masked by the effect of the source resistance. Therefore, to capture this source resistance variation in process an additional statistical parameter was introduced. The improved FET model was demonstrated to be quite close to the hardware. Figure 5 shows the final result of the FET Monte Carlo models. The model is not only on-target with PCM data but is also in agreement with the production circuit data, giving deeper insight into the circuit itself. Figure 6 shows the regulator voltage Vreg and Gm correlation from both Monte Carlo simulation and measured KGD data. While there is still discrepancy between the measured and simulated data, this gives designers some idea of the true variation, whereas the previous model assumes a constant Gm over the entire process. A new design kit was released with these models so designers could use it for future work.

SECTION IV: PROCESS IMPROVEMENT IN RES1

As mentioned previously the variation of some voltage regulators could be traced back to Res1 variation. PCM site data was carefully studied to identify whether the variation was greatest in lot-to-lot, wafer-to-wafer or across wafer. A photo DOE was performed to evaluate the effect of exposure dose and depth of focus on resistance. Then wafers were cross-sectioned after coat and bake to examine the resist profiles. Adjustments to the photo process were carefully made, and many lots were allowed to be processed in between adjustments. Over a period of several months the variation of Res1 steadily dropped down to record low values. However even as variation reduced below previous levels the Vreg in 3 FEM were still elevated as mentioned in Section I and Figure 3. Delving deeper into this problem we found that a particular layout of Res1 was off target; when this was fixed Vreg immediately shifted back on target, shown at around day 350 in Figure 3.
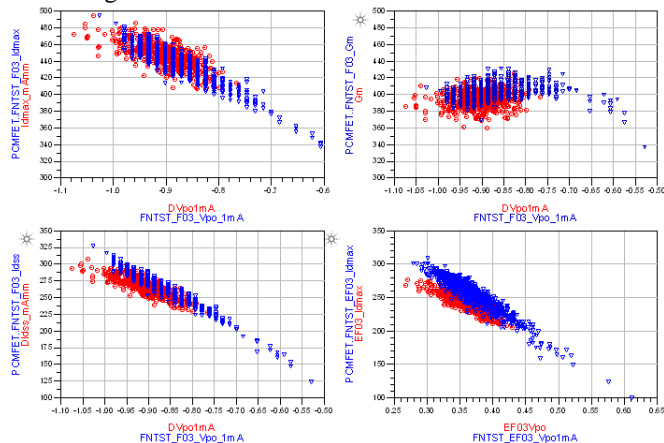

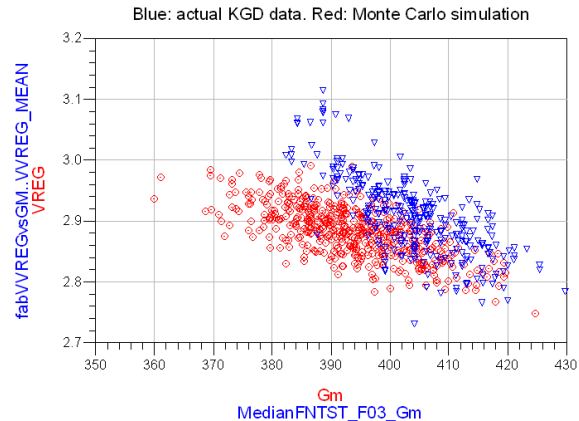Figure 5. Updated pHEMT model; blue triangle is data, and red dot is model

Figure 6. The effect of FET Gm on Vreg. Blue triangle is actual KGD data, red circle is Monte Carlo simulation.

SECTION V: DISCUSSION AND RECOMMENDATIONS

Assuming that this paper was well-written, the audience should find many issues brought up so far to be obvious. Tight specs, accurate models, careful epi growth and resistor process control all seemed like reasonable steps taken to improve yield in this situation. However, during the actual process taking place the yield team at first felt very lost, being submerged with endless amount of data with no clear direction, having received gigabytes of reports and PowerPoint slides and finding nothing relevant, and having received dozens of contradicting hints and advice from others. So what did we learn from this experience that could be of help for solving future yield improvements?

Perhaps the first thing would be to realize that we are no longer in a component-driven mobile market, but a much more integrated one. Increasing yield for a front-end module is more difficult than for individual RF switch, PA or regulator. FEM production increases the complexity in setting spec limits and yield analysis due to additional interactions between various components. In this particular case, the regulator voltage specs weren't initially set tightly because it wasn't clear what Vreg range the PA could tolerate in order to maintain good idle current, gain and EVM. In order to observe this relationship clearly package data was needed in order to correlate back to the regulator voltage, but the drawback was that in the first 1-3 months there wouldn't be enough data. One way to improve yield for future FEM production could be to build corner lots initially to establish this correlation faster, or if possible use data from existing production data as a guideline provided the FEMs are similar to each other.

The second observation is that complex analysis requires thorough knowledge of data query and exploration. When combined with device and circuit knowledge even further progress can be made to understand the root cause. In [1], data was retrieved from boule, epi, PCM, KGD and package test databases using JMP. Here we have taken one step further to incorporate

ADS statistical capabilities to compare PCM and KGD data to ADS Monte Carlo simulation. A major hurdle has been to combine data from different formats into one, which requires complex coding skills and time (something that yield engineers do not have in abundance!); oftentimes this required collective knowledge and many iterations and revisions to accomplish.

Thirdly, this paper has so far mentioned seven different groups involved in this event: product line yield team, product design group, modeling team, research development, process engineering, epi growth engineering and fab yield team. While others had specific responsibilities, the role of the fab yield team was to chart a clear path toward yield improvement--- even though initial process maybe rocky. First of all, when package yield was affected, KGD yield for these FEMs were actually much better than other products. So from this traditional role of maintaining good PCM and KGD yield the fab yield team technically didn't need to act. However when the effects of Vreg, epi, and Res1 became obvious it was hard to ignore its impact on package yield. But fab yield teams traditionally don't set KGD specs, this was the responsibility of product line yield team. In this particular case the fab yield team had to make the case that tighter KGD specs were needed; it is better to suffer loss at wafer-level than at package-level. At epi growth and process engineering levels, since Cpk was good it took some time to convince them that improvement was needed. Thus the fab yield team can feel helpless at times since it doesn't have any firm control over anything and yet somehow expected to improve the final product yield. This FEM yield event has made clear that the yield team was the "oil" that enabled all the gears of production, and in some ways leading other teams to improve yield.

In the light of these group dynamics, perhaps the most important lesson learned from this event was the importance of building relationships across departments. Without the help from research development none of this would have been possible, while the yield team conducted most of the worked described in this paper it was research development that gave a patient and guiding hand. We took extra care to building trust with the product line yield team. The obvious thing was to routinely meet with them to understand their needs and their products. Their actions directly impact the bottom line and therefore it was important to support them in any way possible. On the issue of epi, the epi growth engineers were very collaborative in understanding why certain reactors had high or low Gm. Understanding the root cause was relatively straightforward, however preventing it from happening for all reactors and growth campaigns had been a challenge. Setting clear goals and clear monitor procedures had been beneficial to this process. Admittedly epi process changes take time and for a short period of time fab yield team accommodated them by selectively kitting from existing inventory.

Process engineering were also very open with us and going beyond to improve Res1 process; making process adjustments takes time and therefore it is better to notify them before a yield problem occurs. This would require constant PCM and KGD monitoring to observe anything that has recently shifted, which automated JMP scripts can be very efficient for this task. Subsequently, as a result of the process tightening, much narrower spec and control limits were established to provide immediate feedback if the process starts to drift.

In working with designers and modelers the yield teams helped them identify some key points that needed to be addressed and provided statistical PCM data to improve the models. The designers were also very willing to explain the regulator circuit which was critical to helping the yield team isolate Res1 to be the root cause of the Vreg variation.

Section VI: Summary

This paper documents the productive events that took place as well as what we have learned, technical and institutional during FEM production. It illustrates the need for overall cross functional leadership to make the improvements to establish successful, high cost margin products that contributes to the success of a company. It is through automatic assembly of "Big data" taken from various stages of wafer fabrication, packaging and assembly, and leveraging the data exploration capability of the Universal Data Query software to find the starting point for detailed analysis. Going further to find the root cause, we simulated circuits in ADS, updated device-level models, and tighten epi growth and resistor process control. We have made several observations that are relevant solving future yield problems.

Section VII: Acknowledgement
We would like to thank Bob Baeten and Billy Elliott for their support on this work with respect to product-line yield improvement.

Section VII: Reference
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[2] Eastham *et al*., 2012 CSMANTECH Tech. Dig., May 2012
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ACRONYMS
EVM: Error Vector Magnitude
KGD: Known-Good Die
PCM: Process Control Monitoring
FEM: Front-End Module