Recent Progress in GaN-on-Diamond Device Technology

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Abstract

The intrinsic properties of gallium nitride (GaN) make it an ideal semiconductor material for microwave/millimeter wave power amplifiers. Numerous groups have demonstrated AlGaN/GaN high electron mobility transistors (HEMTs) with power densities exceeding 40 W/mm [1]. Operation at their maximum potential is impractical due to the lack of a viable cooling solution. The majority of high power GaN RF devices are fabricated on semi-insulating silicon carbide (SiC) substrates. This has been shown to be a viable solution albeit even SiC with its superior thermal conductivity (~350 W/m-°K), cannot overcome the heat loads being generated by the GaN HEMTs. It has become readily apparent as GaN device technology matures that thermal impediments are limiting it from realization of its true capability. One strategy under consideration is to substitute the SiC substrate with a much higher thermal conductivity diamond substrate (~2000 W/m-°K) to enhance localized thermal management. In 2006 AFRL demonstrated the first working AlGaN/GaN HEMT on a GaN/DIA wafer fabricated by Group4 and Emcore [2]. This early technology demonstration provided a pathway for future exploration of producing GaN based devices on polycrystalline CVD diamond substrates. For the past two years, the DARPA Near Junction Thermal Transport (NJTT) Program has explored the development of passive cooling approaches through integration of high thermal conductivity diamond in close proximity to the active transistor junction. In this work, AFRL provides an assessment of the electrical and thermal performance of diamond integrated GaN devices fabricated under the NJTT Program.

INTRODUCTION

GaN HEMTs are rapidly becoming the technology of choice for high power RF applications. However, exploiting the true operational capability of GaN remains problematic due to the inability effectively manage device self-heating. In order to obtain peak performance and reliable operation, improved thermal transport solutions are required. An approach under consideration is the integration of high thermal conductivity diamond in close proximately (~1um) to the active channel. The electrically insulating and thermal dissipation properties of CVD diamond provide an attractive option. The high thermal conductivity of polycrystalline CVD diamond (2000W/m-K) provides a superior means of thermal dissipation compared to silicon or SiC substrates. Modeling simulations have projected GaN/DIA HEMTs to run cooler and therefore more reliably and efficient. Since 2006, AFRL has been actively engaged in device fabrication and assessment of GaN/DIA technology [2][3][4][5][6]. In partnership with DARPA and industry performers BAE, Northrop-Grumman, Raytheon, RFMD and Triquint, AFRL has assessed the electrical and thermal characteristics of NJTT Program deliverables.

DIAMOND INTEGRATION

Integration of CVD diamond heat spreaders into conventional semiconductor processing techniques have evolved over the past several years. Substrate bonding approaches have been reported that successfully integrate diamond with GaN HEMT devices [7][8][9]. Diamond integration introduces many challenges due to interface issues associated with materials mismatch, thermal expansion and thermal resistances. Under the DARPA NJTT Program, performers employed three different fabrication approaches to integrate diamond in close proximity to the active heat source. The first approach involved the growth of AlGaN/GaN device layers on silicon (111) substrates by metal organic chemical vapor deposition (MOCVD). A sacrificial silicon handle wafer was attached to the front-side of the GaN epi wafer to facilitate removal of the host silicon substrate. Following removal of the host silicon substrate and epitaxial transition layers, a proprietary dielectric layer was deposited onto the epi-inverted GaN buffer to facilitate growth of approximately 100 µm of polycrystalline diamond. The handle wafer was removed and the GaN/DIA wafer was ready for device processing.

The second approach involved the growth of AlGaN/GaN device structures on SiC substrates by MOCVD. The wafer underwent front side processing first followed by bonding a silicon carrier to facilitate

SiC substrate removal [10]. The GaN and diamond surfaces were prepared for dielectric layer deposition and subsequent low temperature bonding.

The final approach involved the direct growth of high quality CVD diamond into via's located within microns from the device junction. AlGaN/GaN layers were grown on 4H SiC substrates by molecular beam epitaxy (MBE). Via's were subsequently etched into the SiC backside. A microwave plasma deposition system using purified methane and hydrogen as reactants was used for diamond via growth [11]. Front side device processing was performed following diamond deposition.

RESULTS AND DISCUSSION

Pulsed IV characteristics were evaluated with an Accent DiVA 265. Dynamic IV (200 ns pulse separated by 1 ms, Vd = 0V and Vg = 0V) performance was compared with static IV performance as shown in Figure 1. Here, the black traces show the dynamic and static characteristics for GaN/SiC with the red curves showing the GaN/DIA characteristics. The percentage of current droop was calculated:

$$(Id_{dynamic} - Id_{static})/\ Id_{dynamic}\ at\ Vd_{max}$$

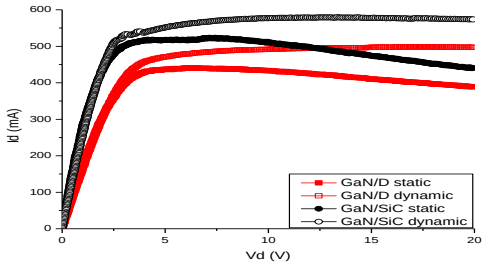

Figure 1: Representative pulsed IV characterization

Table 1 summarizes current droop measured on different device materials from multiple sources. No pulsed IV analysis was performed on devices from source A. In general, the percentage of current droop for GaN/DIA and GaN/SiC was similar at roughly half that of GaN/Si.

Table 1: Pulsed IV current droop

Source	GaN/Si	GaN/SiC	GaN/DIA
A	-	-	-
B	28.1	13.3	15.6
C	-	23.1	21.7
D	39.2	-	19.6

The effects of pulse length on current droop were also investigated as seen in Figure 2. Samples were conditioned through multiple IV sweeps to stabilize trapping related effects. Pulse length was varied from 0.5 µs to 20 µs and current droop calculated. The GaN/DIA device technology exhibited less current droop as a function of pulse length relative to the GaN/Si device technology as summarized in Table 2.

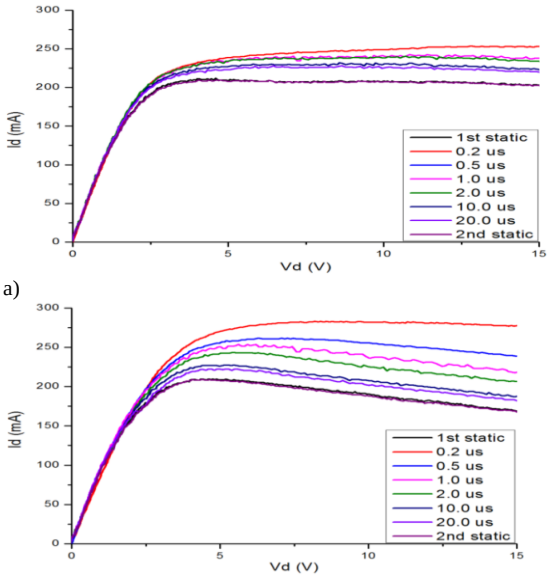

Figure 2: Current droop as a function of pulse length for a) GaN/DIA and b) GaN/Si

Table 2: Pulsed IV as a function of pulse length

Pulse Width (µs)	GaN/Si	GaN/DIA
0.5	14.1	5.9
1.0	21.3	5.9
2.0	25.7	7.4
10.0	32.4	11.9
20.0	34.6	13.0
static	39.2	19.6

Performer D compared as-grown GaN/Si material properties (mobility, sheet charge, and sheet resistance) with those of the material integrated with diamond to evaluate any impact on performance due to diamond growth process. Room temperature, on-wafer Hall measurements on fabricated van der Pauw test structures were used to evaluate material properties. Average sheet resistance (Rsh), mobility (µ), and sheet charge (Ns) values for the GaN/DIA wafer were 423.1 Ω/sq, 1197 $cm^2/V*s$, and 1.2 $10^{13}/cm^2$, respectively. Values for the GaN/Si wafer were 427.91 Ω/sq, 1304 $cm^2/V*s$, and 1.1 $10^{13}/cm^2$, respectively. The material properties for the two wafers were in reasonable agreement. The slightly lower mobility seen in the GaN/DIA could be due to interface roughening as a result of the wafer preparation process. Table 3 shows a summary of the average and (standard deviation) for measured material properties.

Table 3: Material properties – average and (standard deviation)

Parameter	GaN/Diamond	GaN/Si
Rsh (Ω/sq)	423.1 (12.0)	427.9 (15.3)
μ (cm^2/V*s)	1197 (69)	1304 (32)
Ns (10^{13}/cm^2)	1.2 (0.1)	1.1 (0.1)

A Quantum Focus Instruments Infrascope II infrared (IR) microscope was used to evaluate the thermal characteristics of the various device material systems. IR signatures (Figure 3) were used to obtain an estimate of the temperature rise in the devices under dc bias. Figure 4 shows the relative temperature rise for GaN/Si, GaN/SiC, and GaN/DIA for performers B and D. For these performers devices were vacuum mounted to IR thermal chuck and devices biased at power levels from 1 – 10 W/mm. As expected the temperature rise for the GaN/Si devices is the highest and the GaN/DIA the lowest with the GaN/SiC falling somewhere in the middle. There was reasonable agreement in the temperature rise data between the two performers. Performer A provided packaged parts for characterization. These packages were screwed down to thermal chuck and the temperature rise for GaN/SiC and GaN/DIA devices of the same periphery were measured (Figure 5). This data was used to calculate the relative thermal resistance (Rth):

*Rth ~ (Tpeak – Tbase) / (Vd * Id)*

This data is shown in Figure 6. For these parts the Rth for GaN/DIA devices is roughly 20% lower than for GaN/SiC devices. Looking at a fixed temperature rise of 88 K, the GaN/DIA devices achieved 16.2 W versus 10.03 W for the GaN/SiC devices or a 1.62X improvement (Figure 7). Conversely, at a fixed power level of 8 W, the GaN/DIA devices had only a 45 K rise in temperature relative to the 70 K temperature rise for the GaN/SiC, a difference of roughly 36% (Figure 8).

Performer C delivered fixtured devices that were characterized with Raman spectroscopy (Renishaw). GaN/DIA and GaN/SiC devices were biased and two-peak Raman analysis used to determine the temperature rise at several locations in a multi-finger device. The GaN/DIA sample had a gate pitch 1/3 that of the GaN/SiC sample. Given this difference in device area (mm^2) one would expect roughly a 3X increase in temperature rise. As seen in Figure 9, the GaN/DIA device showed only an average 18K temperature rise relative to the GaN/SiC device. This equates to only a 0.35X increase in temperature rise whereas one would expect a 3.0X increase based on device area (mm^2).

Large signal performance of the different material systems was evaluated via load pull. Power sweep data from performer D are shown in Figure 10. Here, GaN/DIA and GaN/Si devices with identical device topology are compared. Under the same bias conditions, the GaN/DIA device yielded ~ 0.22 W higher power (22% increase) and 8% higher power added efficiency. Power sweep data for GaN/DIA and GaN/SiC devices from performer C are shown in Figure 11. While the GaN/DIA device does not perform as well as the GaN/SiC, the performance per area (mm^2) is what matters. As with the devices characterized with Raman spectroscopy, the GaN/DIA device here has 1/3 the gate pitch, which equates to roughly 1/3 the active area. Looking at the relative power per area (W/mm^2), the GaN/DIA device yields 3.6X W/mm^2 compared with the GaN/SiC.

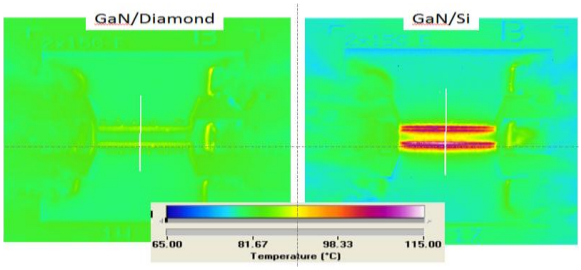

Figure 3: Representative IR thermal signatures

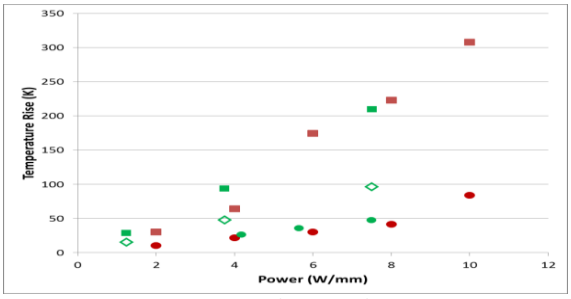

Figure 4: Temperature rise as a function of material measured with IR Microscopy

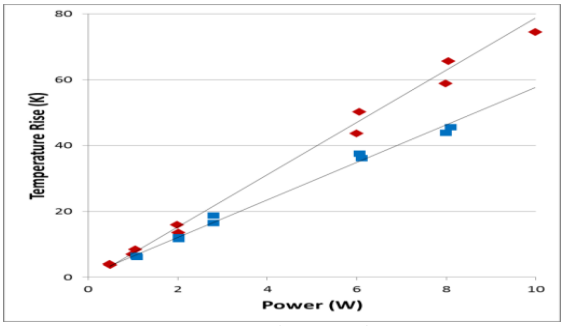

Figure 5: Temperature rise as a function of material measured with IR Microscopy

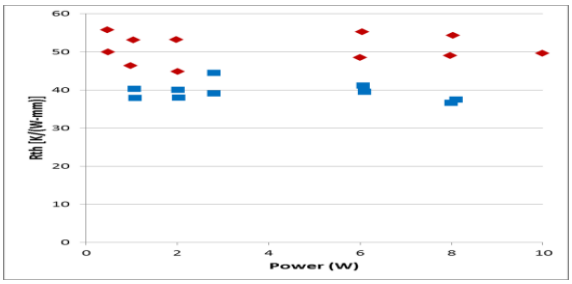

Figure 6: Thermal resistance (Rth) as a function of material

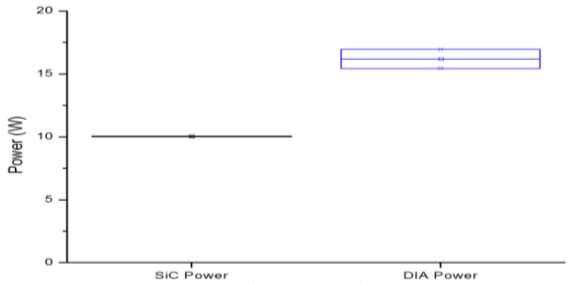

Figure 7: Relative power performance at fixed temperature rise

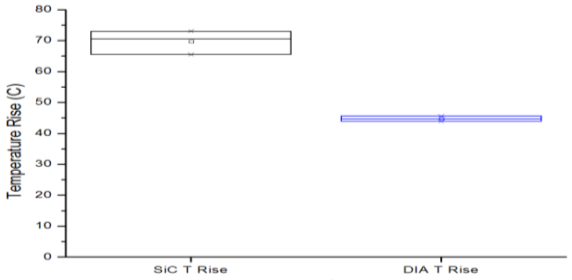

Figure 8: Relative temperature rise at fixed power level

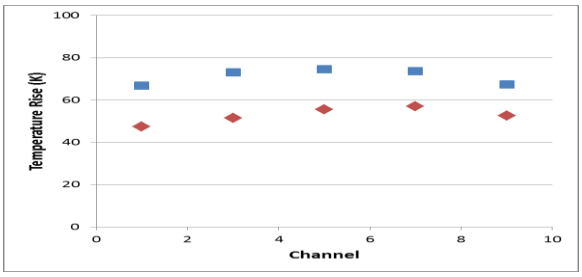

Figure 9: Temperature rise as a function of material

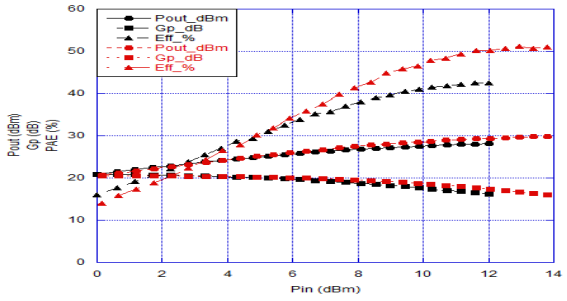

Figure 10: Power sweeps for GaN/DIA and GaN/Si devices

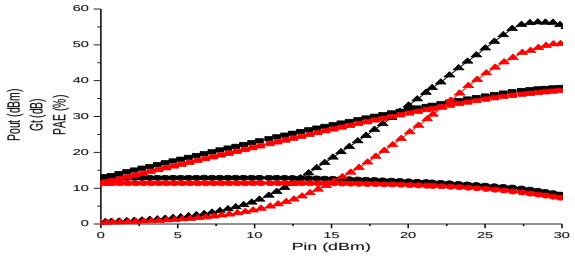

Figure 11: Power sweeps for GaN/DIA and GaN/SiC devices

CONCLUSIONS

The Air Force Research Lab's Sensors Directorate, in cooperation with DARPA NJTT Program performers have characterized the electrical and thermal performance of devices fabricated on GaN/SiC, GaN/Diamond and GaN/Si. Analysis showed that the diamond integration process did not significantly degrade the electrical performance and clear trends show improved thermal performance. This novel materials technology continues to show promise but significant improvements with material quality are necessary.

ACKNOWLEDGEMENTS

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