Yield Improvement of Metal-insulator-metal Capacitors in MMIC Fabrication Process Based on AlGaN/GaN HFETs

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Abstract

This contribution deals with the metal-insulator-metal (MIM) capacitor yield improvement in a GaN-based MMICs fabrication process. High MIM capacitor yield is one of the prerequisites for the fabrication of reliable and cost efficient GaN MMICs. In this work, technological factors influencing capacitor yield were identified and analyzed. The analysis was focused on the quality of the bottom capacitor electrode. Based on the analysis, a modification to the fabrication process has been proposed and tested. As a result of the process optimization, 94 % yield of 160×250 µm^2 MIM capacitors was achieved with a breakdown field strength of 5×10^8 V/m. The proposed modification to the process does not require additional technological steps, which is a great advantage of our approach.

INTRODUCTION

Reproducible GaN HFET technology enables the realization of broadband high power amplifiers and highly efficient amplifier concepts such as Class-D, E, F, Doherty, envelope-tracking and other techniques [1]. The fabrication of reliable and low-cost monolithic microwave integrated circuits (MMICs) in general requires high yield of both transistors and passive elements, i.e. resistors, metal-insulator-metal (MIM) capacitors, and inductors. Fabrication of MIM capacitors with high breakdown field strength has been discussed extensively in literature as a stand-alone task, or in conjunction with other technologies, such as GaAs, InP, and CMOS [2-4]. In this contribution, we will focus on the integration of MIM capacitors in the existing AlGaN/GaN HFET fabrication process flow and discuss technological factors influencing yield and breakdown voltage (V_{br}) of capacitors.

EXPERIMENTAL DETAILS

The most commonly used dielectric for the fabrication of AlGaN/GaN HFETs is silicon nitride. In the standard FBH GaN process flow two layers of SiN_x are deposited. The first is for the realization of "embedded" gates, and the second for the encapsulation of the gates [5]. The second layer also serves as a dielectric insulator for the MIM capacitors. Both layers are deposited by plasma enhanced chemical vapor deposition at 325 °C. The recipes of these two layers differ from each other in order to compensate mechanical strain caused by SiN_x. The targeted thickness of the 2nd SiN_x passivation layer is 200 nm. After in-situ NH_3-plasma pre-treatment, the layer is deposited using a SiH_4/NH_3 gas ratio of 2/1. The resulting amorphous SiN_x has a refractive index in the range 1.86-1.87 as measured by ellipsometry. A typical epitaxial structure consisting of a GaN:Si/$Al_{0.25}Ga_{0.75}N$/GaN epitaxial layer stack on s.i.SiC substrate was used for the fabrication of MMICs with transistors having Ir-based gate metallization. On wafer isolation was realized by N^+ ion implantation yielding typical isolation resistance of ~ 10^{11} – 10^{12} Ω/□ at 100 V.

As a starting point of our optimization, we analyzed MIM capacitor test structures with 160×250 µm^2 top electrode area as shown in Fig. 1. The capacitor was formed between interconnect metallization Ti/Au (20/600 nm) and 3.5 µm of plated Au used for the formation of air-bridges. Our MIM breakdown measurements were limited to 200 V or 400 V and breakdown was defined by a leakage current limit of 1×10^{-5} A or damage of the capacitor.

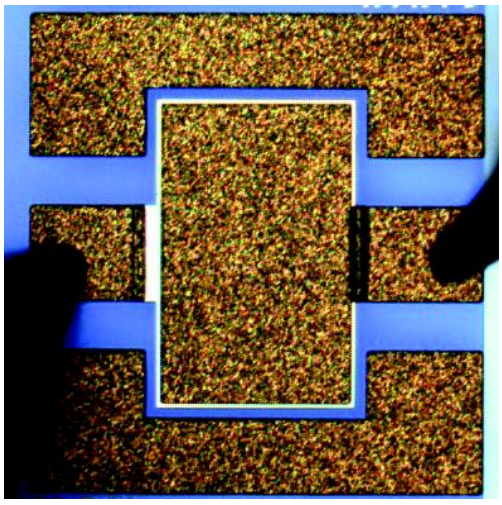

Figure 1. Test MIM capacitor having structure Ti/Au (20/600 nm) - SiN_x (200 nm) - Au (3.5 µm) and 160×250 µm^2 area of the top electrode.

RESULTS AND DISCUSSION

The results of measurements taken from 11 wafers processed in three consecutive runs show the distribution of the breakdown voltage means in the range from 9 V (σ = 23 V) to 171 V (σ = 16 V) between wafers. In the process of identifying the existing problem, it was found that the bottom metal roughness was the dominant factor explaining the observed scattering of V_{br} and the reduced yield. Another important weakness was related to the edges of the MIM structures. The identified sources of metal roughness are listed below in descending order of importance:

- particles from metal evaporation
- scratches of the metal surface, as a result of conventional lift-off
- defects on the semiconductor (GaN in our case) surface.

Fig. 2 (top row) shows examples of dark field light microscopy images of the bottom MIM plate after the subsequent deposition of SiN_x capacitor dielectric. In addition, Fig. 2 (bottom row) shows an example where a particle on the bottom electrode observed during processing was found to cause a short during breakdown measurements. The quality of the bottom electrode associated with the metal evaporation procedure has been discussed for example by Wang *et al.* [2]. The suggested improvements include cleaning and pre-melting of a metal source prior to each run in conjunction with evaporation rate adjustment and post-evaporation treatments. The obvious problem with this approach is integration of the proposed treatments in the existing process flow and mass-production. Furthermore, in order to improve process stability, one should prevent scratches due to lift-off where the thickness of the bottom metallization becomes an important parameter.

Following the above considerations we have modified the processing sequence of the MIM capacitors by moving the formation of MIM bottom electrodes into a different process step, namely the gate metallization. By doing this we have achieved a few goals simultaneously. First, the total thickness of the bottom electrode metallization has been reduced to ~300 nm. This already improved the roughness of the metal surface due to fewer particles. Second, the gentler manual or soak lift-off procedure applied for the gate metallization (and consequently also for the

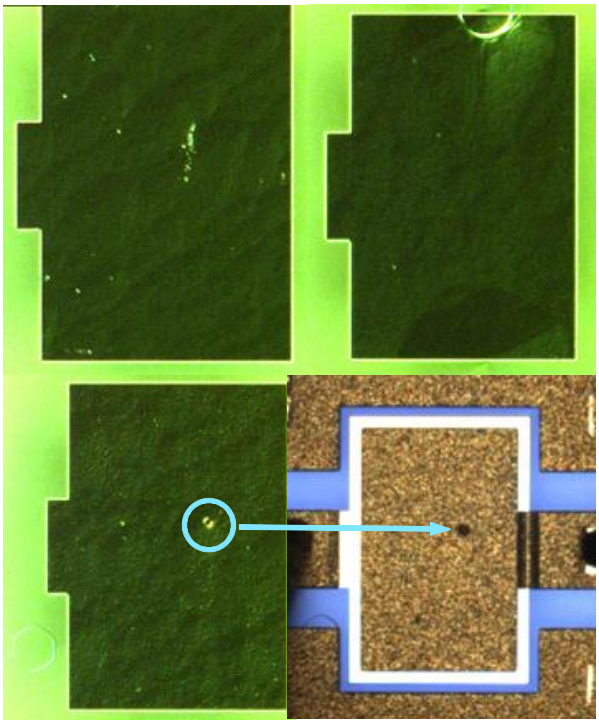

Figure 2. Dark field light microscopy images of the MIM bottom plates showing particles, scratches and epitaxial defects as spots with increased intensity (top row). As an example (bottom row), marked particle on bottom electrode observed during processing was found to cause a short during breakdown measurement.

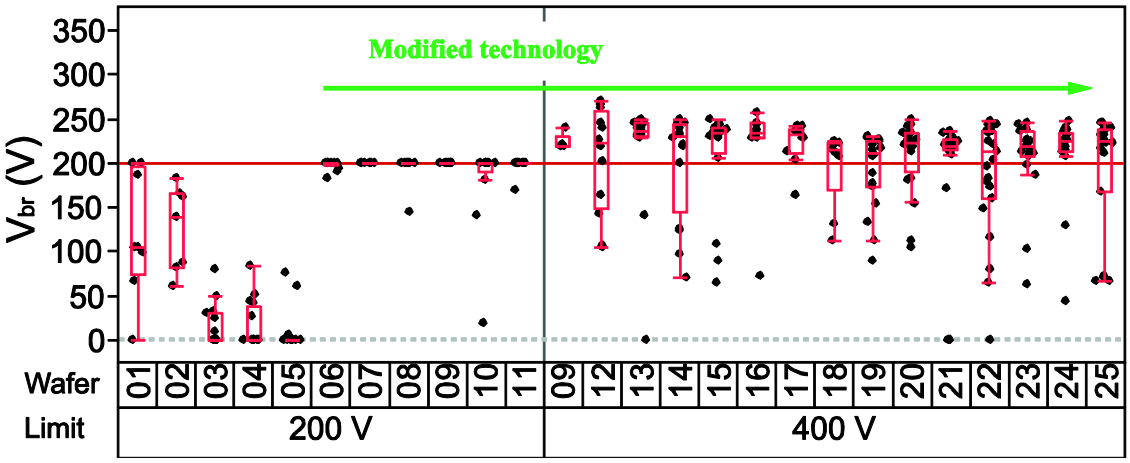

Figure 3. Box-and-whisker plots of MIM capacitor breakdown measurements performed on wafers 01-05 processed before modification and 20 wafers (06-25) processed in 5 consecutive process runs after modification of technology. The measurements were limited to 200 V and 400 V as represented by two groups of plots. The current limit is always 1×10^{-5} A. The red line shows targeted breakdown voltage of 200 V.

metallization of the bottom capacitor plate) avoids numerous scratches from the patterned metal. Third, the top electrode can now be formed by the evaporated 1st interconnection metallization, which was found to be better in terms of edge roughness as compared to the 2nd interconnection metal used in the previous process. In addition, a soft gate metal annealing (tempering) at 350 °C after lift-off smooths the surface of bottom electrode due to built-in stress reduction by recrystallization.

Fig. 3 shows the results of the optimization: box-and-whisker plots of the MIM breakdown measurements given for 20 wafers processed in 5 consecutive process runs in comparison to the wafers (wafer 01-05) processed before modification of the technology. On the wafers processed with modified technology, the breakdown voltage was equal to or above 200 V, which indicates a breakdown field strength of 1×10^9 V/m, and has been measured for 81 % of the MIM capacitors. Lowering the limit for V_{br} to 100 V (requirement for our quarter micron GaN MMIC process), which indicates a breakdown field strength of 5×10^8 V/m, results in 94 % MIM capacitor yield. The results of the measurements show the distribution of the V_{br} means and standard deviations in the range from 180 V (σ = 51 V) for wafer 10, where the measurements were limited by 200 V, to 220 V (σ = 56 V) for wafer 16.

Current-voltage (*I-V*) characteristics of non-shorted MIM capacitors from wafers 01-05 are shown on Fig. 4(a). For comparison, *I-V* measurement curves obtained on wafers 16 and 21 are shown in Fig. 4(b). The degree of current increase before technology modification shows that a vast majority of MIM structures were physically damaged. On the other hand, current gradually increases on wafers processed using the modified technology. This is a property of the SiN_x dielectric layer and it is caused by hopping conductivity mainly visible at bias levels close to the dielectric breakdown.

We conclude that the improvement obtained as a result of MIM technology modification is due to an effective reduction of the number of particles and scratches on the bottom MIM electrodes. Furthermore, the breakdown of MIM capacitors on wafers 06-25 is now limited by the quality and properties of the SiN_x layer and defined by the selected current limit of 1×10^{-5} A.

In additional investigations we designed and processed capacitors with increased areas of 200×500 µm^2 and 400×500 µm^2. Breakdown measurements revealed distributions of the V_{br} means and standard deviations in the range from 137 V (σ = 71 V) to 205 V (σ = 33 V) for 200×500 µm^2 area capacitors and from 81 V (σ = 28 V) to 185 V (σ = 51 V) for 400×500 µm^2 area capacitors. The statistics are based on 7 wafers and at least 14 capacitors of each type measured on each wafer. The results are in line with our understanding of the problem. They also indicate that larger capacitor areas have higher probability to be affected by particles/defects/scratches on the bottom capacitor electrodes and therefore show larger statistical variability and lower breakdown voltage means. These results show also stability, robustness and limitations of our technology.

In order to clarify possible contribution of the SiN_x thickness variation on the reported breakdown results as well as to control reproducibility of our technology, the

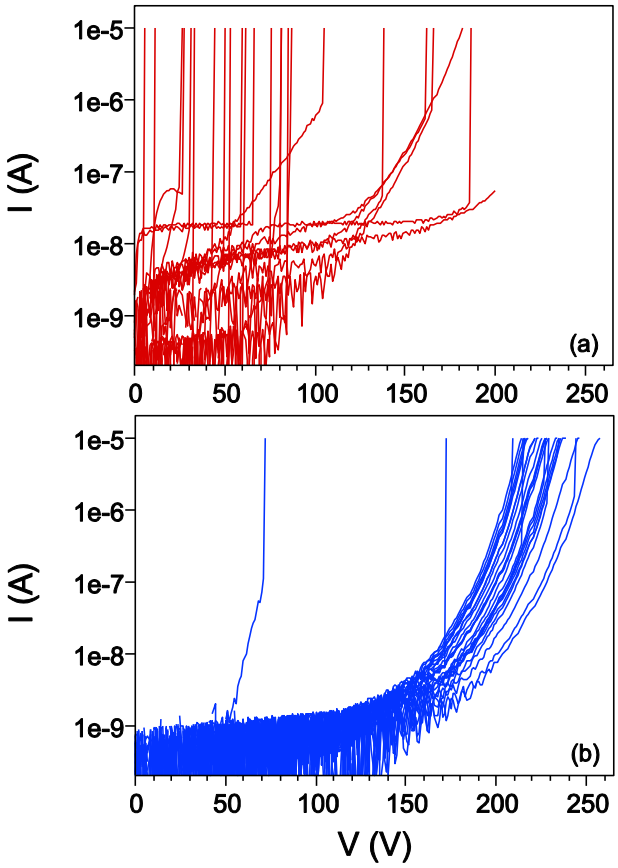

Figure 4. Current-voltage (*I-V*) breakdown characteristics with current limit of 1×10^{-5} A measured on (a) wafers 01-05 processed before modification of technology and (b) wafers 16 and 21 processed using modified technology.

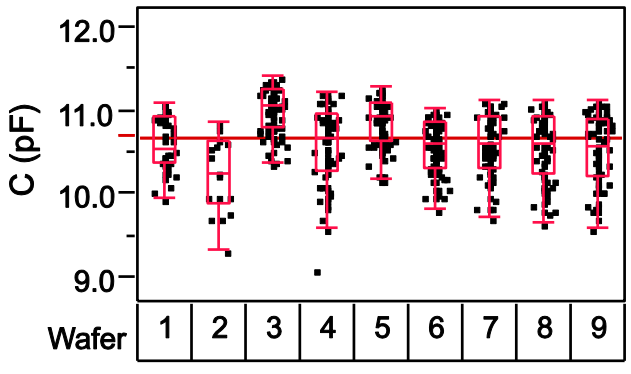

Figure 5. Box-and-whisker plots of capacitance values for the MIM structures with 160×250 µm^2 area fabricated on 9 wafers from 3 consecutive runs. The line shows 10.7 pF average value of a complete data set.

capacitance measurements were performed on 9 wafers from 3 consecutive runs using the modified technology. The capacitor values were defined from on-wafer *C-V* measurements performed at 500 kHz frequency and bias of 23 V with an AC amplitude of 50 mV. The results of these measurements for MIM capacitor test structures with 160×250 μm^2 top electrode are presented in Fig. 5. The mean value of the capacitors is 10.7 pF and standard deviation is 0.4 pF. This indicates very good reproducibility of the capacitance within wafer and from wafer to wafer. Thus, the thickness of the SiN_x layer does not have a significant contribution to the breakdown statistics provided in Fig. 3. The reproducible capacitance value of the MIM structures indicates a stable quality of the SiN_x itself, which potentially could have a significant impact on all results presented in our work.

CONCLUSIONS

In conclusion, we have analyzed the reasons for reduced yield of MIM capacitors in the fabrication process of GaN-based MMICs. In the process of problem identification, it was found that mainly the bottom metal roughness causes reduction in capacitor breakdown and therefore reduced yield. Based on our findings we optimized the MMIC fabrication process sequence and improved MIM capacitor yield by moving the formation of the bottom MIM electrode into a different process step. The introduced changes to the process sequence resulted in yield of 94 % for 160×250 μm^2 MIM capacitors with a breakdown field strength of 5×10^8 V/m. A great advantage of our approach is that it does not require any additional process steps. In addition, the stability and reproducibility of the modified technology has been demonstrated by providing statistics for the breakdown voltages and capacitance values within wafers and across process runs.

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ACRONYMS

HFET: Heterojunction Field Effect Transistor
MIM: Metal-Insulator-Metal
MMIC: Monolithic Microwave Integrated Circuit