Homojunction GaN *p-i-n* Rectifiers with Ultra-low On-state Resistance

T.-T. Kao*, J. Kim, Y.-C. Lee, M.-H. Ji, T. Detchprohm, R. D. Dupuis, and S.-C. Shen

School of Electrical and Computer Engineering, Georgia Institute of Technology,

777 Atlantic Drive NW, Atlanta, GA, 30332-0250

* Email: tkao6@gatech.edu ; Phone: 404-385-8327

Keywords: GaN, *PIN*, rectifiers, III-nitride.

Abstract

We present a comparative study of homojunction GaN *p-i-n* (*PIN*) rectifiers grown on either free-standing GaN (FS-GaN) or sapphire substrate. The *PIN* rectifier grown on sapphire shows the breakdown voltage (V_B) of 600 V and a specific on-resistance ($R_{ON}A$) of 0.66 mΩ-cm^2. On the other hand, a *PIN* rectifier grown on a FS-GaN substrate shows substantial improvement with V_B> 800 V and $R_{ON}A$ = 0.28 mΩ-cm^2. The corresponding Baliga's Figure of Merit (V_B^2/ $R_{ON}A$) of >2.5 GW/cm^2 is achieved. The device performance follows the same trend for GaN switches and demonstrated the lowest on-resistance for 800-V diode switches reported to date.

INTRODUCTION

GaN-based power rectifiers including *p-i-n* (*PIN*) diodes [1]-[7] and Schottky Barrier Diodes (SBDs) [8]-[12] have attracted much research interest in recent years because of their ultra-low conduction loss, high-voltage and high-temperature operations for next-generation power electronic circuits. GaN *PIN* rectifiers in particular possess several performance advantages over SBDs such as ultra-low leakage current and avalanche capabilities that are preferred for high-power applications. Previously, these devices were fabricated on foreign substrates such as sapphire [5] and silicon carbide (SiC) [7]. However, high density of threading dislocations (in the order of $10^8 \sim 10^9$ cm^{-2}) originated from the strained heteroepitaxial growth on foreign substrates may become problematic for high-voltage *PIN* rectifiers as the *i*-GaN drift layer becomes thicker. While this rather high dislocation density does not prevent these III-nitride devices from working, it limits their full potential as these defects serve as leakage paths, carrier traps, and premature breakdown sites which significantly reduce the current handling capabilities of power electronic devices.

Most recently, the availability of sufficiently large GaN substrates enabled the homoepitaxial growth of GaN-based devices. Among these high-quality native substrates prepared by different techniques, free-standing GaN (FS-GaN) substrates [13] currently offer a threading dislocation density below the order of 10^6 cm^{-2} with a large size of > 2 in. diameter.

Using conducting FS-GaN substrates, one may realize a vertical power switch in III-N power electronic devices that allow for high-current operations and lowest possible conduction loss at a given blocking voltage rating.

In this paper, we conducted a comparative study for GaN *PIN* rectifiers grown on sapphire and FS-GaN substrate, respectively, and studied the *C-V* and *I-V* characteristics in these devices. The *PIN* rectifiers grown on FS-GaN show breakdown voltage (V_B) of >800 V and $R_{ON}A$ of 0.28 mΩ-cm^2, in comparison to V_B = 600 V and $R_{ON}A$ = 0.66 mΩ-cm^2 for similar device sizes grown on a sapphire substrate. The corresponding Baliga's Figure of Merit (BFOM) is greater than 2.5 GW/cm^2 for the device grown on FS-GaN. These results show a substantial improvement through the use of native substrates in III-N bipolar switches. The on-resistance is also among the lowest value reported for 800-V switches to date.

DEVICE STRUCTURES AND FABRICATION PROCESSING

In this study, GaN *PIN* rectifiers were grown on either *c*-plane sapphire substrates or *c*-plane FS-GaN substrate using a Thomas–Swam metal–organic chemical vapor deposition (MOCVD) system. The GaN *PIN* rectifier structure consists of a 1.1-µm n^+-GaN ($n\sim 1.5\times10^{18}$/cm^3), a 6-µm unintentionally-doped GaN drift layer, a 260-nm thick *p*-GaN ($p\sim 1\times10^{18}$/cm^3), and a 20-nm thick heavily doped p^+-GaN cap layer ($p> 2\times10^{20}$/cm^3). For the devices grown on sapphire, a 4 µm-thick GaN buffer layer was grown on top of the non-conductive substrate. On the other hand, for the devices grown on FS-GaN substrate ($n> 1\times10^{18}$/cm^3), the thickness of GaN buffer layer is ~ 1 µm. The carrier concentrations for *p*-type and *n*-type regions were estimated by the Hall-effect measurement on thicker epitaxial layers grown in separate calibration runs under similar conditions. *PIN* rectifiers were processed under similar processing recipes to minimize the processing variation in the performance evaluation. Nevertheless, the device grown on sapphire uses a side-contact scheme while the devices grown on a conducting FS-GaN

substrate enable a vertical current-injection scheme. The device fabrication started with a mesa etching using an inductively coupled plasma (ICP) etching tool. Ni/Ag-based metal stacks were deposited to form the *p*-type contact. Ti/Al-based metal stacks were deposited on the exposed *n*-type GaN region for devices grown on sapphire substrates to form *n*-type contact on the top side of the wafer. For devices grown on the *n*-type conducting FS-GaN substrate, the *n*-type ohmic contact was formed on the backside of the wafer. An additional Ti/Au metal layer was deposited to serve as a field termination plate. The spin-on-glass was used for the device passivation and the accessing via-holes were opened. Finally, a 1-um-thick Ti/Au metal layer was deposited to form the anode electrode. The fabricated *PIN* rectifier grown on FS-GaN was mounted on a copper plate for the device testing.

RESULTS AND DISCUSSIONS

Fig. 1 shows the measured capacitance-voltage (*C*-*V*) characteristics for two *PIN* rectifiers grown on sapphire and FS-GaN substrates, respectively. Since the free-hole concentration in *p*-type GaN is presumably much higher than the free-electron concentration in the unintentionally-doped "i" layer, the depletion width under the reverse bias falls mostly in the drift layer. The free-carrier concentration of the unintentionally-doped layer (N_i) is

$$\frac{1}{C^2} = \frac{1}{A} \cdot \frac{2}{q\varepsilon_s \varepsilon_0 N_i} (V_{bi} - V) \qquad (1)$$

where ε_0 is the free-space permittivity, A is defined by the anode contact area, V_{bi} is the built-in potential, and ε_s is the relative permittivity of the un-doped GaN layer. Therefore, N_i can be determined by the slope of $1/C^2$ plots under the reverse bias. As shown in Fig. 1, the calculated N_i is ~1.3×10^{16} (cm^{-3}) for the device grown on sapphire or FS-GaN substrate. These results suggest the heteroepitaxial growth yields similar unintentionally doped drift layer as in the case of homoepitaxy on FS-GaN substrates in the MOCVD system.

The current-voltage (*I*-*V*) characteristics were measured using a Keithley 4200-SCS semiconductor parameter analyzer at room-temperature. Fig. 2 (a) shows a comparison of the forward *I*-*V* characteristics of a GaN *PIN* rectifier grown on sapphire and FS-GaN substrate, respectively. The *PIN* rectifier under test has anode contact diameter of 30 microns. The left and right axes represent the current density (*J*) and specific on-resistance ($R_{ON}A$), respectively. R_{ON} is defined as the differential resistance (*dV/dI*) at a given *J*. For the device grown on sapphire, the ideality factor (η) is ~ 3.1 and $R_{ON}A$ is ~ 0.66 mΩ-cm^2 at *J*= 2.5 kA/cm^2. This unrealistic η value may simply result from the resistive *PIN* structure grown on sapphire substrate. On the other hand, for the device grown on FS-GaN, η is ~ 2.1 and

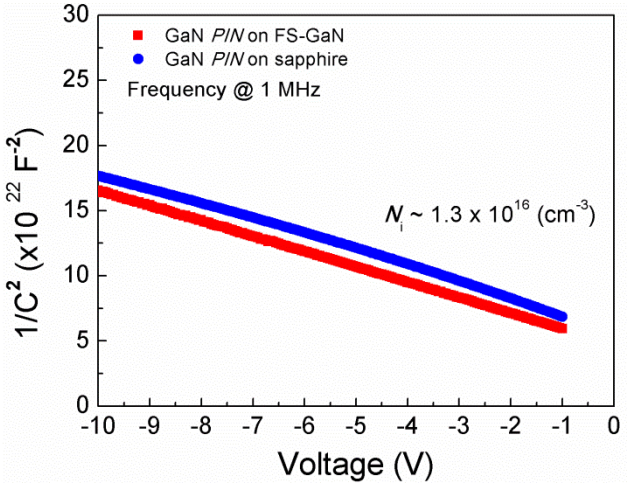

Fig. 1. Measured $1/C^2$ plots versus reverse voltage for the *PIN* rectifiers grown on FS-GaN or sapphire substrate. The net carrier concentration in the unintentionally-doped "i" layer can be determined from Eq. (1).

$R_{ON}A$ value is significantly reduced to 0.28 mΩ-cm^2 at the same *J*. These results indicate a high-quality *p*-*i*-*n* structure was realized on the native substrate with improved $R_{ON}A$ due to less scattering centers arising from the extensive defects in the epitaxial layers.

Fig. 2 (b) shows the reverse *I*-*V* characteristics of the same *PIN* rectifiers up to –200 V. For the devices grown on sapphire, the leakage current increases with the reverse bias voltage and reaches ~ 30 nA (or *J*~ 1 mA/cm^2) at –200 V. The off-state breakdown voltage (V_B) was also evaluated using a Tektronix 576 curve tracer, where V_B is the voltage as *J* reaches 1 A/cm^2 under reverse bias. The devices under test were measured in a fluorinert environment to prevent outer electric discharge at a high voltage. V_B of ~600 V was achieved for the device grown on sapphire (data not shown here).

On the other hand, the device fabricated on FS-GaN substrate shows low leakage current below 1 pA (or $J < 0.1$ μA/cm^2) for voltage up to –200 V. It represents at least four orders of magnitude of reduction in the leakage current at –200 V. Fig. 3 (a) shows the reverse characteristics of the same *PIN* device grown on FS-GaN substrate. The left and right axes represent the measured reverse voltage and current, respectively. As shown in the graph, the reverse current is ~1 μA (*J*~ 0.14 A/cm^2) at –800 V and the corresponding BFOM ($V_B^2/R_{ON}A$) of >2.5 GW/cm^2 was achieved. It is also noted the BFOM obtained in the homojunction GaN *PIN* rectifier shows better performance when compared to the reported vertical GaN SBDs (BFOM = 1.7 GW/cm^2 [8]). Since *PIN* rectifiers grown on either substrate have similar doping concentrations, the nature of low reverse current and high breakdown voltage can be ascribed to the adoption of low-dislocation-density epitaxial layers using native substrates.

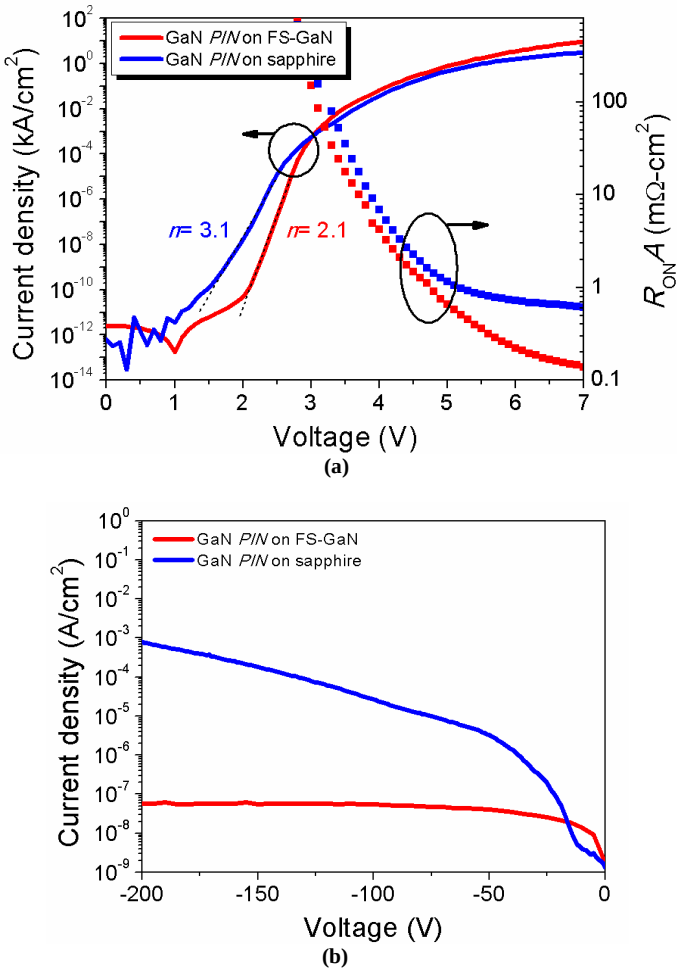

Fig. 2. (a) The forward and (b) reverse *I-V* characteristics of the GaN *PIN* rectifiers grown on FS-GaN (solid line in red) and sapphire substrate (solid line in blue), respectively.

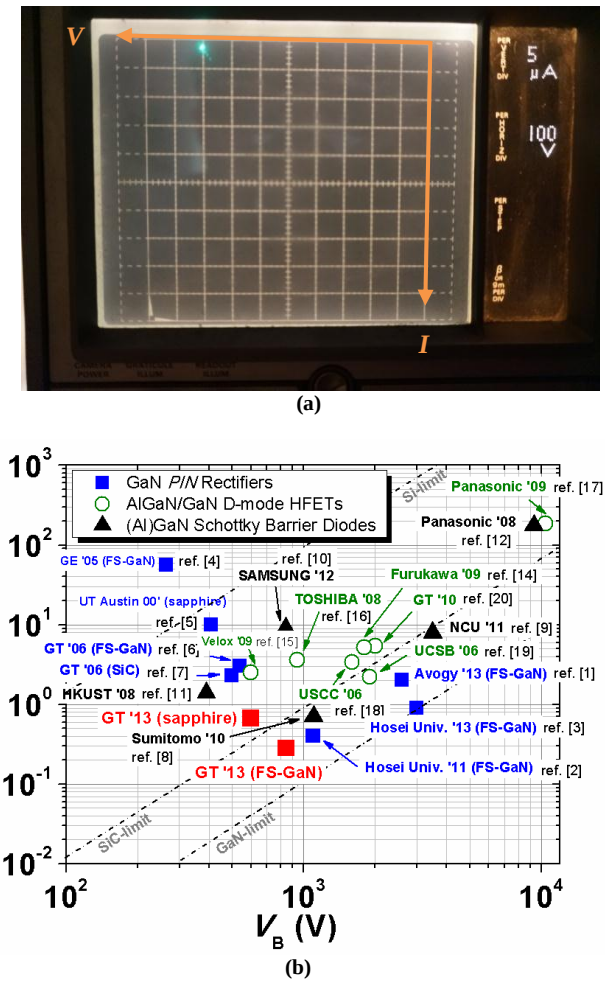

Fig. 3. (a) The off-state characteristics (as indicated by the bright dot) for a GaN *PIN* rectifier grown on FS-GaN. The device has an anode contact diameter of 30 microns. The reverse current is ~ 1 µA at –800 V. (Horizontal: 100 V/Division. Vertical: 5 µA/Divisions). (b) A comparison chart showing the breakdown voltage versus specific on-state resistanc for GaN power rectifiers grown on different substrates (sapphire, SiC and FS-GaN), GaN or AlGaN/GaN SBDs, and normally-on AlGaN/GaN HFETs.

Fig. 3 (b) shows a competitive study of state-of-the-art GaN *PIN* rectifiers grown on different substrates (sapphire [5], SiC [7] and FS-GaN [1-234]), SBDs [8-912], and normally-on AlGaN/GaN heterojunction field-effect transistors (HFETs) [14]-[20]. The dotted lines on the plot represent the theoretical limits for Si, SiC, GaN switches. For a given breakdown voltage rating, vertical *PIN* rectifiers show at least 10 times lower R_{ON}×A values when compared to III-nitride-based SBDs and AlGaN/GaN HFETs achieved so far. These *PIN* devices are consistently demonstrating the best BFOM for GaN-based switches and approaching to the theoretical limit for GaN. Our device also demonstrated the same trend for GaN *PIN* rectifiers when it scales to the 800-V range and, as our best knowledge, showed the lowest on-state resistance for 800-V devices reported to date.

CONCLUSIONS

We present a comparative study of GaN *PIN* rectifiers grown on either sapphire or FS-GaN substrate. Similar carrier concentrations of the un-doped drift layer are obtained for *PIN* devices grown on different substrate platforms. The fabricated *PIN* rectifier on FS-GaN exhibits a higher V_B> 800 V and extremely lower $R_{ON}A$ value of 0.28 mΩ-cm^2, in comparison to the device on sapphire with V_B of 600 V and $R_{ON}A$ value of 0.66 mΩ-cm^2. The corresponding BFOM of >2.5 GW/cm^2 is achieved for the device on FS-GaN and represents a 5× improvement over similar devices grown on sapphire substrate. The device performance reported in this paper also demonstrates the same trend for GaN *PIN* rectifiers when it scales to the 800-V range and shows the lowest on-state resistance for 800-V devices achieved to date.

ACKNOWLEDGEMENTS

The authors are thankful for the cleanroom facility support of the staff in the Microelectronic Research Center at the Georgia Institute of Technology in Atlanta, GA.

REFERENCES

[1] Isik C. Kizilyalli, Andrew P. Edwards, Hui Nie, Don Disney, and Dave Bour, "High voltage vertical GaN p-n diodes with avalanche capability," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3067–3070, Oct. 2013.

[2] Y. Hatakeyama, K. Nomoto, N. Kaneda, T. Kawano, T. Mishima, and T. Nakamura, "Over 3.0 GW/cm^2 figure-of-merit GaN p-n junction diodes on free-standing GaN substrates," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1674–1676, Dec. 2011.

[3] Y. Hatakeyama, K. Nomoto. A. Terano, N. Kaneda, T. Tadayoshi, T. Mishima, and T. Nakamura, "High-Breakdown-Voltage and Low-Specific-on-Resistance GaN p–n junction diodes on free-Standing GaN substrates fabricated through low-damage field-plate process," *Jpn. J. Appl. Phys.*, vol. 52, pp. 028007, Jan. 2013.

[4] X. A. Cao, H. Lu, S. F. LeBoeuf, C. Cowen, and S. D. Arthur, "Growth and characterization of GaN PIN rectifiers on free-standing GaN," *Appl. Phys. Lett.*, vol. 87, no. 5, pp. 053503, Aug. 2005.

[5] T. G. Zhu, D. J. H. Lambert, B. S. Shelton, M. M. Wong, U. Chowdhury, H. K. Kwon, and R. D. Dupuis, "High-voltage GaN pin vertical rectifiers with 2 μm thick i-layer," *Electron. Lett.*, vol. 36, no. 23, pp. 1971–1972, Nov. 2000.

[6] J. B. Limb, D. Yoo, J.-H. Ryou, W. Lee, S.-C. Shen, and R. D. Dupuis, "High performance GaN pin rectifiers grown on free-standing GaN substrates," *Electron. Lett.*, vol. 42, no. 22, pp. 1313–1314, Oct. 2006.

[7] J. B. Limb, D. Yoo, J.-H. Ryou, S.-C. Shen, and R. D. Dupuis, "Low on-resistance GaN pin rectifiers grown on 6H-SiC substrates," *Electron. Lett.*, vol. 43, no. 6, pp. 67–68, Mar. 2007.

[8] Y. Saitoh, K. Sumiyoshi, M. Okada, T. Horii, T. Miyazaki, H. Shiomi, M. Ueno, K. Katayama, M. Kiyama, and T. Nakamura, "Extremely low on-resistance and high breakdown voltage observed in vertical GaN Schottky barrier diodes with high-mobility drift layers on low dislocation-density GaN substrates," *Appl. Phys. Exp.*, vol. 3, no. 8, pp. 081001-1–081001-3, Jul. 2010.

[9] G. Y. Lee, H. H. Liu, and J. I. Chyi, "High-performance GaN pin rectifiers grown on free-standing GaN substrates," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1519–1521, Nov. 2011.

[10] J. H. Lee, J. K. Yoo, H. S. Kang, and J. H. Lee, "840 V/6 A-AlGaN/GaN Schottky barrier diode with bonding pad over active structure prepared on sapphire substrate," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1171–1173, Aug. 2012.

[11] W. Chen, K. Y. Wong, W. Huang, and K. J. Chen, "High-performance AlGaN/GaN lateral field-effect rectifiers compatible with high electron mobility transistors," *Appl. Phys. Lett.*, vol. 92, pp. 253501, June 2008.

[12] H. Ishida, D. Shibata, H. Matsuo, M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "GaN-based natural super junction diodes with multi-channel structures," in *IEDM Tech. Dig*., pp. 1–4, 2008.

[13] M. K. Kelly, R. R. Vaudo, V. M. Phanse, L. Gorgens, O. A. Ambacher, and M. Stutzmann, "Large Free-Standing GaN Substrates by Hydride Vapor Phase Epitaxy and Laser-Induced Liftoff," *J. Appl. Phys.*, vol. 38, pp. L217-219, Feb. 2009.

[14] N. Ikeda, J. Lee, S. Kaya, M. Iwami, T. Nomura, and S. Katoh, "High-power AlGaN/GaN HFETs on Si substrates for power-switching applications," in *Gallium Nitride Materials and Devices IV*, San Jose, CA, USA, pp. 721602-11, 2009.

[15] X. Xiaobin, S. Junxia, L. Linlin, J. Edwards, K. Swaminathan, M. Pabisz, M. Murphy, L. F. Eastman, and M. Pophristic, "Demonstration of Low-Leakage-Current Low-On-Resistance 600-V 5.5-A GaN/AlGaN HEMT," *IEEE Electron Device Lett.*, vol. 30, pp. 1027-1029, Oct. 2009.

[16] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "A 120-W boost converter operation using a High-Voltage GaN-HEMT," *IEEE Electron Device Lett.*, vol. 29, pp. 8-10, Jan. 2008.

[17] Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "Recent advances of high voltage AlGaN/GaN power HFETs," in *Gallium Nitride Materials and Devices IV*, San Jose, CA, USA, pp. 721606-11, 2009.

[18] N. Tipirneni, A. Koudymov, V. Adivarhan, J. Yang, G. Simin, and M. A. Khan, "The 1.6 kV AlGaN/GaN HFETs," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 716–718, Sep. 2006.

[19] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaNHEMTs With Integrated Slant Field Plates*", IEEE Electron Dev. Lett.*, vol. 27, no. 9, pp. 713, Sep. 2006.

[20] T. T. Kao, C. Y. Wang, S. C. Shen, D. A. Girdhar and F. Hebert, "2.5-Ampere AlGaN/GaN HFETs on Si Substrates with Breakdown Voltage > 1,250V," in *2011 CSMANTECH Technical Digest*, May 2011.

ACRONYMS

SBD: Schottky Barrier Diode
GaN: gallium nitride
SiC: silicon carbide
FS-GaN: free-standing GaN
$R_{ON}A$: specific on-resistance
BFOM: Baliga's Figure of Merit
V_B: breakdown voltage
ICP: inductively coupled plasma
η: ideality factor
J: current density
HFET: heterojunction field-effect transistor