# Thermal Property of WNiSi Thin Film Resistor

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**Abstract**

**Thin film resistor is a very important component in the integrated circuits for both Si and compound semiconductors. There are many different materials for different applications or processes. In this paper, the thermal property of a PVD deposited WNiSi is investigated. Correlations of a film sheet resistance with annealing temperature and time are established. The activation energy is derived from the experiment data.**

## INTRODUCTION

Thin film resistor (TFR) is a component widely used in semiconductor integrated circuitries. There are many different types of thin film resistors, such as Cr [1], NiCr [2],[3], WSi [4]-[9], and TiN [10]. Their applications depend on their sheet resistance ranges and thermal properties. One of the most important parameters to describe the thermal property is the Temperature Coefficient of Resistivity (TCR). The TCR of each type of TFR has to be well understood before it is integrated into the wafer processes and circuit designs.

There is another interesting thermal property, which is the dependence of the film sheet resistance on the anneal temperature. For some of the TFRs, it is very important because an improper thermal budget or a large temperature variation during a wafer process can cause a large variation of the final sheet resistance. WNiSi is one of these TFRs and typically deposited in room temperature.

In this paper, we will report our study of the WNiSi thin film sheet resistance with different annealing temperatures and time. Strong correlations between the sheet resistance and the heating temperature and time were established. The activation energy of WNiSi was determined. The mechanism of the sheet resistance changing with heating temperature and time will be discussed.

## EXPERIMENT

WNiSi thin film is deposited on a GaAs substrate which has a layer of $SiO_2$ for electrical isolation purpose. PVD system is used for WNiSi deposition at room temperature. The different thicknesses of WNiSi are used in the experiment. Then WNiSi deposited wafers are annealed in either an oven or a hot plate system. Figure 1 shows the simplified diagrams of these two heating systems. Figure 1(a) is a hot plate in a chamber with the pressure of 2.65τ. Figure 1(b) is an oven with a $N_2$ flow. The thermal transfer in the hot plate system is dominated by the thermal conduction, while the thermal radiation and convection are the dominated heat transfer mechanisms in an oven. The temperature disturbance in the hot plate system is negligible during the wafer loading, but the temperature drops dramatically in an oven system during the wafer loading and requires minutes to recover back and become stable. Therefore the heating is much faster in the hot plate system than that in the oven. Furthermore, the hot plate heating is more suitable for the study of WNiSi sheet resistance change with temperature range from room temperature up to 400°C. The oven is more suitable for the study of the time dependence at a certain temperature.

## RESULTS AND DISCUSSIONS

The sheet resistance was measured before and after the annealing process. For the convenience of the discussion of the sheet resistance at different temperatures and time, the percentage change relative to the film sheet resistance as deposited is used in this paper. The WNiSi sheet resistance is a function of the annealing temperature T and the time t as $R_\square(T, t)$. The percentage change of the annealed WNiSi sheet resistance relative to the original value $R_{\square 0}$ as the film deposition at room temperature is $\Delta R(T, t)/R_{\square 0}$. Actually, $\Delta R(T, t)/R_{\square 0}$ is $\Delta R[T(t), t]/R_{\square 0}$ because the temperature can be also a function of the time in the temperature ramping period.

Figure 2 shows the WNiSi sheet resistance change as a function of the time at the annealing temperature of 250°C in the oven. X axis is the time in second and Y is in a scale of percentage. The normal annealing cycle is 30 minutes. For a anneal time at 60 and 90 minutes, it will go through the annealing cycle two or three times accordingly. The TFR sheet resistance was measured prior to the first annealing

9

cycle, between each annealing cycle, and post the final cycle. The correlation is shown as diamonds in the chart with a linear fitting. The interception gives the value of $\Delta R[T(t), t]/R_{\square 0}$ at t=0 which is 17.4%. For all annealing process, there is always a temperature ramp period. In the case of the oven annealing here at 250°C, the wafer temperature ramping was slow and long because of the large temperature drop during the wafer loading and the large system thermal capacity. Actually it took about 7 minutes for the wafers reaching the set point of 250°C without an over shoot. The square points are the data by removing the first 7 minutes from each annealing cycle. The linear fit also gives the same 17.4% interception. This means that the 17.4% change of the sheet resistance is coming from the impact of the temperature of 250°C, while the ~70 minutes at 250°C only gives another 2.4% change of the sheet resistance. In fact, the slope of the fit line, which is only 6ppm/s, describes the time dependence of the sheet resistance at 250°C.

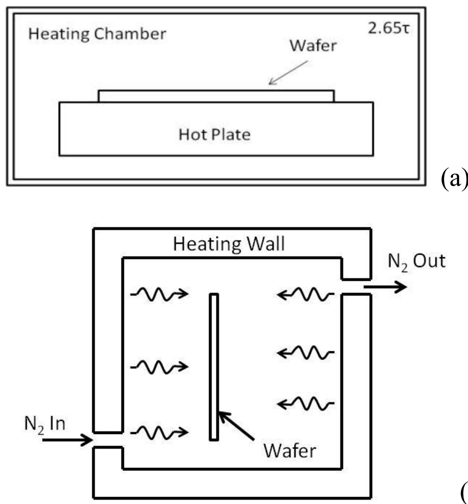


FIGURE 1. SIMPLIFIED DIAGRAMS OF TWO HEATING SYSTEMS: (A) A HOT PLATE IN A VACUUM CHAMBER WITH A PRESSURE OF 2.65T; (B) AN OVEN WITH A $N_2$ FLOW

The temperature ramping in the oven is slow and complicated, while it is much faster with a hot plate heating. Figure 3(a) shows the $\Delta R[T(t), t]/R_{\square 0}$ behavior with the hot plate anneal. The set temperature of the hot plate was 350°C. There are two regions in the chart. The zone I is a region of $\Delta R[T(t), t]/R_{\square 0}$ fast growing, which is related to the temperature ramping. Since the time impact on the sheet resistance is only at ppm level, we can ignore the time contribution to $\Delta R[T(t), t]/R_{\square 0}$ in the zone I. The zone II is a region of a slow change. Therefore, $\Delta R[T(t), t]/R_{\square 0}$ can be expressed as below:

$$\Delta R[T(t), t]/R_{\square 0} = \Delta R[T(t)]/R_{\square 0} + B*t \qquad (1)$$

where B is the slope of the linear correlation of the sheet resistance and the time in the zone II.

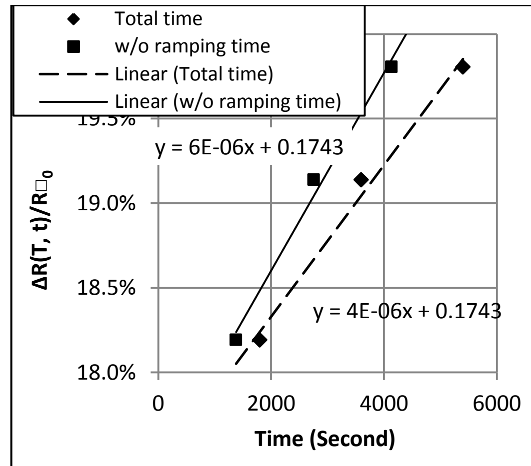


FIGURE 2. THE PERCENTAGE WNISI SHEET RESISTANCE CHANGE AT 250°C IN AN OVEN

In the hot plate system, the heat transfer is dominated by the thermal conductance. Because of the similarity of the thermal conductance equations and the electrical equations, we can use an electrical capacitor charging process to simulate the hot plate heating process. Then, the Eq. (1) can be written as

$$\Delta R[T(t), t]/R_{\square 0} = A*\{1-EXP[-(t-t_0)/RC]\}+B*t \qquad (2)$$

where A is the percentage sheet resistance change at the time the wafer reaches the hot plate temperature 350°C; $t_0$ is a time delay; R is the wafer thermal resistance and C is the wafer thermal capacity assuming that the temperature disturbance of the wafer to the hot plate is negligible.

The solid line in Figure 3(b) is a simulation with only the capacitor charging model, the first term of the Eq. (2). The sheet resistance change is saturated with the time and has almost no change after the wafer reaches the set temperature. The dotted line in Figure 3(b) is the fit with the Eq. (2). The coefficient A in the Eq. (2) fitting is 24.4%, which is the impact of 350°C to the resistance change. The time constant RC is 30 sesonds, which is an indicator of how fast the wafer can be heated. WNiSi was deposited in a PVD with a chuck at the room temperature. However, the real film deposition temperature with the plasma strike was about 50+°C. The delay time $t_0$ is the time for the wafer heated up to the PVD deposition temperature (50+°C) in order to have the sheet resistance begin to change. In our case, $t_0$=8s. $B=4x10^{-5}$/s, which is the slope of the correlation to the time once the temperature is stable similar to the discussion of Figure 2. Although the slope here is almost one order higher than 250°C in the oven, it is still only 40ppm, which again proves

that the time impact to the annealing is a secondary factor comparing to the temperature.

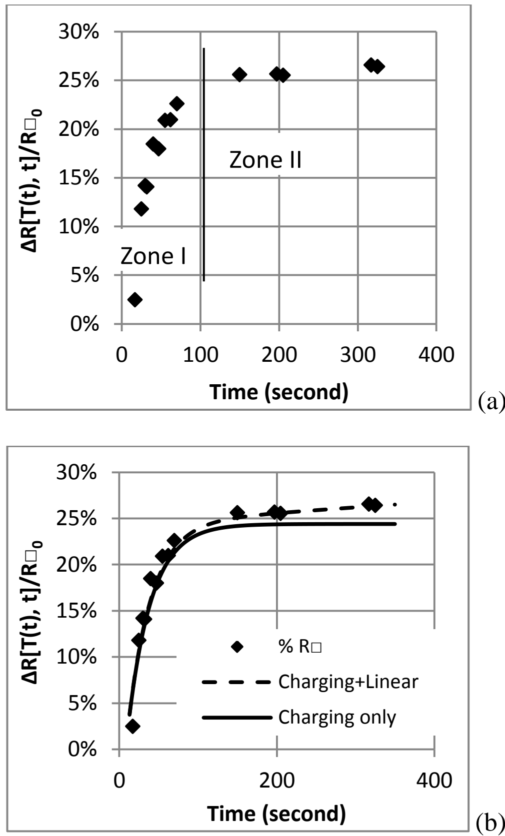


FIGURE 3. THE WNISI SHEET RESISTANCE CHANGE DURING THE ANNEAL PROCESS. (A) RAW DATA AND (B) WITH A CHARGING ONLY AND CHARGING PLUS LINEAR MODEL FITTINGS

The temperature dependence of $\Delta R[T(t), t]/R_{\square 0}$ is shown in Figure 4 with an activation energy Ea of 0.19eV. The sample was annealed in the hot plate system with time of 300 seconds and temperature from 300 to 400°C. A TEM cross section image of the sputter deposited WNiSi film is shown in Figure 5 as the dark area in the middle. Based on the target formation, it is a Si rich $WSi_2$ and $NiSi_2$ film and in amorphous form. This also can be seen from the XRD analysis shown in Figure 6. The sharp peak at about 16° on all three charts is from the substrate. The small wide peak at about 22° is from the WNiSi film and indicates that there are only clusters of $WSi_2$ or $NiSi_2$ and there is no significant formation of hexagonal crystallization of $WSi_2$ as seen in CVD deposited $WSi_2$ film in Ref. [9]. The reasons of the difference are the lower anneal temperature range and the method of the film deposition.

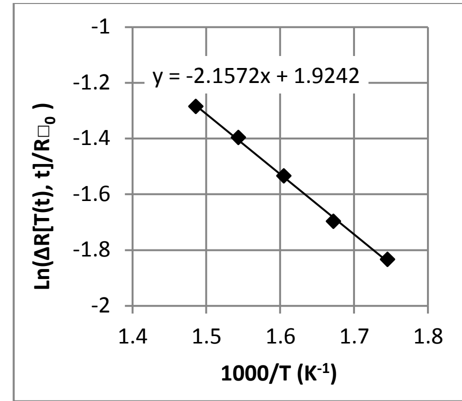


FIGURE 4. THE CORRELATION OF THE WNISI SHEET RESISTANCE AND THE TEMPERATURE

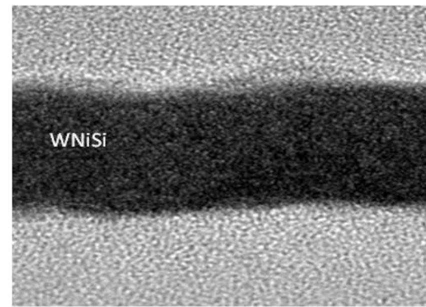


FIGURE 5. A TEM IMAGE OF THE WNISI FILM

## CONCLUSIONS

The thermal property of WNiSi was investigated. Its room temperature sheet resistance depends on the annealing condition. The annealing temperature dominates the sheet resistance change and the time is only with the impact of 6 to 40ppm/s in the temperature range of 250°C to 350°C. The activation energy of WNiSi TFR is 0.19eV. This property can be used for different applications, such as a thermal tunable resistor [11]. A full understanding of the sheet resistance change with temperature is still needed.

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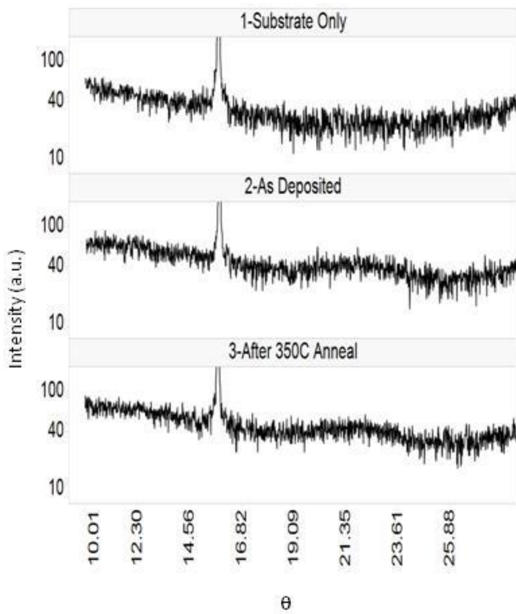


FIGURE 6. XRD ANALYSIS OF THE WNISI FILM DEPOSITED WITH A SPUTTER

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ACRONYMS

TFR: Thin Film Resistor
TCR: Temperature Coefficient of Resistivity
WNiSi: Tungsten-Nickel-Silicon
NiCr: Nickel-Chromium
WSi: Tungsten-Nickel-Silicon
TiN: Titanium Nitride
PVD: Physical Vapor Deposition
CVD: Chemical Vapor Deposition