An Optical 150-nm Y-Gate Process for InAlN/GaN HEMTs

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***Abstract* —— An optical 150-nm-gate-length Y-gate process was successfully developed for InAlN/GaN high-electron mobility transistors (HEMTs). This simple process is suitable for low cost production. With this process technology, we could obtain a high transconductance of 460 mS/mm and a high current gain cutoff frequency f_T of 70 GHz for InAlN/GaN HEMTs on high-resistance silicon substrates.**

1. Introduction

Recently, high-speed operations of a current gain cutoff frequency f_T more than 200 GHz have been reported for InAlN/GaN HEMTs with a gate length L_g less than 100 nm [1–3]. However, complicated processes e.g., an electron beam lithography and a regrowth technology were necessary. Therefore, we focused on low cost and simple technologies suitable for mass production. We first used a high-resistance silicon substrate; it is more cost-effective than a semi-insulating SiC substrate. Secondary, we developed a Y-gate process without using an electron beam lithography. We used a conventional i-line stepper. This process enables us to obtain short L_g of 150 nm and low parasitic gate capacitance.

In this paper, we describe the details of the device fabrication process. Then, we show DC and RF characteristics of InAlN/GaN HEMTs.

2. Device Fabrication Process

2.1 Wafer preparation

InAlN/GaN HEMTs epitaxial layers were grown by metal-organic chemical vapor deposition on 100 mm high-resistance silicon substrates. The typical structure consists of an AlGaN buffer layer, a GaN buffer layer, an AlN interlayer, a nearly lattice-matched InAlN barrier layer and a GaN cap layer. Sheet resistance is approximately 500 Ω/sq.

2.2 Resist shrinkage

An optical Y-gate process flow is shown in Fig. 1. First of all, a SiN film was deposited on the surface by sputtering using an electron cyclotron resonance plasma (Fig. 1(a)). This deposition method can create denser films than those of conventional plasma-enhanced chemical vapor deposition. The refractive index and the thickness of the SiN film were 2.02 and 40 nm, respectively. Then, a resist pattern with 1.0-μm-thick and 270-nm-width was obtained by an i-line stepper (Fig. 1(b)). In order to obtain the precise gate length, the shape of the resist pattern shall be as rectangle as possile.

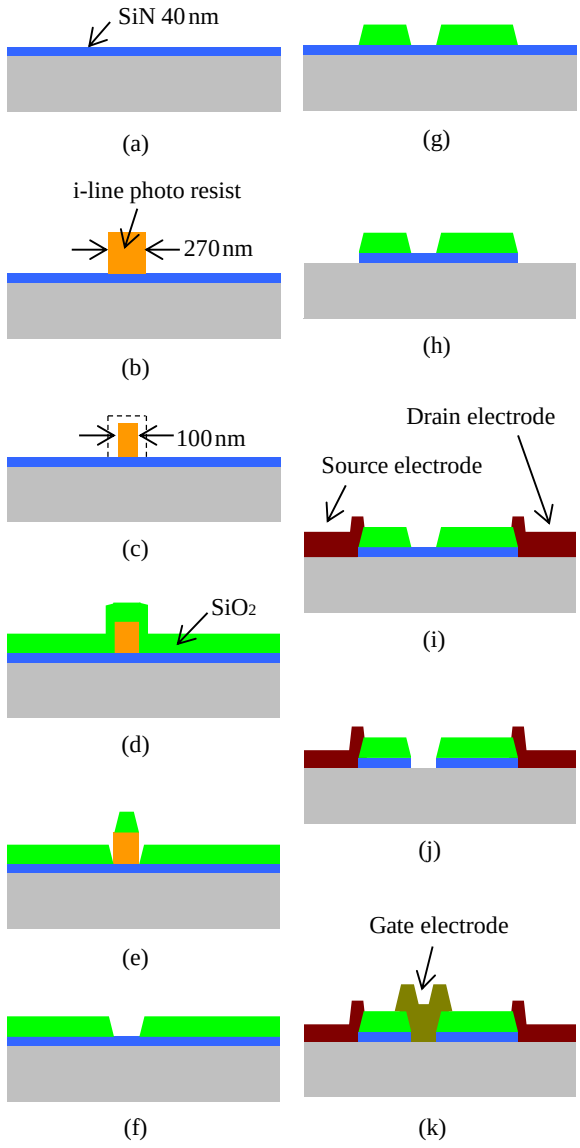

Fig. 1 Y-gate process flow using an i-line stepper

The resist pattern was shrunk by an O_2 plasma etching. (Fig. 1(c)). The scanning electron microscopy (SEM) upper views and schematic cross-sectional images of the resist pattern before and after the O_2 plasma etching are shown in Fig. 2. The SEM views indicate that the shape of the dummy gate was maintained. The width of the dummy gate was shrunk from 270 nm to 100 nm.

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2.3 SiO_2 sputtering

300-nm-thick SiO_2 film was deposited on the pattern by a sputtering (Fig. 1(d)). The SiO_2 film adhering to the sidewall of the resist was removed by a buffered hydrofluoric acid (BHF) solution (Fig. 1(e)). When SiO_2 film is deposited by a conventional sputtering, SiO_2 covers the dummy gate isotropic, i.e., SiO_2-thickness at the bottom and that adhering to the sidewall are almost the same as shown in Fig. 3. In this case, the bottom width after BHF etching, which corresponds to gate length, wider than that before BHF etching.

To avoid it, we have developed a collimated sputtering. The sputtering can form porous SiO_2 adhering to the sidewall of the resist. The SEM bird's-eye views of the dummy gate before and after the BHF etching are shown in Fig 4. Although SiO_2 at the bottom is dense, that adhering to the sidewall is porous. So, the SiO_2 adhering to the sidewall is removed faster. Therefore, expansion of the bottom width is prevented as short as possible.

2.4 Electrode formation

After the dummy gate was lifted off (Fig. 1(f)), SiO_2 of the ohmic region was removed. Since SiO_2-thickness is as thick as 300 nm, an opening process is difficult. So we took four-steps opening as shown in Fig. 5. First, 50% thickness of SiO_2 was etched by a Cl_2/BCl_3 reactive ion etching (RIE) with relative high etching rate. Then rest 30% thickness of SiO_2 was etched by the same RIE but with low power condition. Finally, we used BHF solution due to low damage and high SiO_2/SiN selectivity (Fig. 1(g)). Since an etching ratio of SiO_2 to SiN by a BHF solution is approximately 100, etching is stopped at the SiN surface. Then, the SiN film and the GaN cap layer were etched by CF_4-RIE and Cl_2/BCl_3-RIE, respectively (Fig. 1(h)).

Next, source and drain electrodes were formed on the InAlN barrier layer by a conventional lift-off technique (Fig. 1(i)). Ohmic annealing was performed by a rapid thermal annealing.

We compared *I-V* curves between different opening methods. We evaluated the pattern which electrode distance was 2.2 μm. The *I-V* curves of the conventional opening, i.e., only RIE with constant etching condition, and that of four-steps opening are shown in Fig. 6. The current of four-steps opening is almost two times higher at 2 V than that of conventional opening.

Next, SiN film on the gate was etched by CF_4-RIE with SiO_2 mask (Fig. 1(j)). Finally, a gate electrode was formed on the GaN cap layer, and was lifted off by a conventional technique (Fig. 1(k)).

2.5 TEM observation

A transmission electron microscopy (TEM) view of cross section of the InAlN/GaN HEMT is shown in Fig. 7. L_g, source-gate distance L_{sg} and gate-drain distance L_{gd} were 150 nm, 1.0 μm and 1.3 μm, respectively. The gate sidewall was tapered and its angle was approximately 60°. We can control this angle by changing the SiO_2-thickness and RIE conditions. The angle is important, since it determines the parasitic gate capacitance and the electric field at the gate edge.

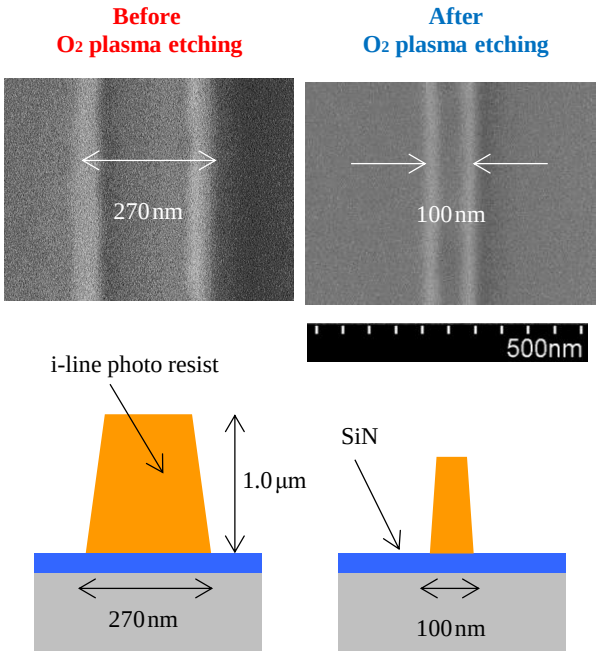


Fig. 2 SEM upper views and schematic cross-sectional images of the resist pattern before and after the O_2 plasma.

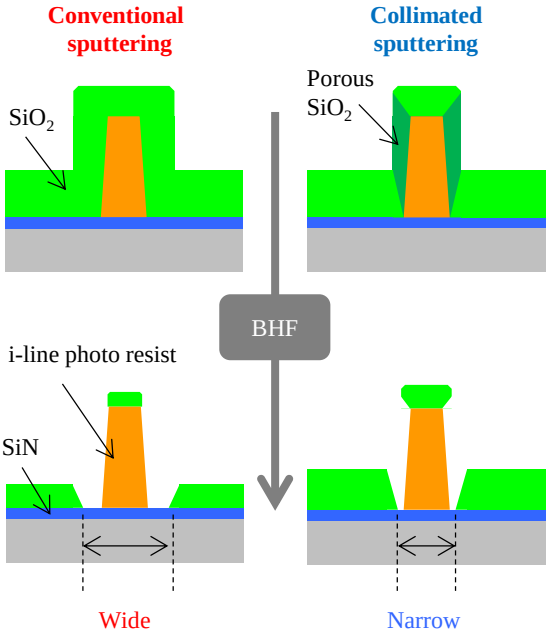


Fig. 3 Comparison the sputtering methods. Schematic cross-sectional images of the resist pattern before and after the BHF etching.

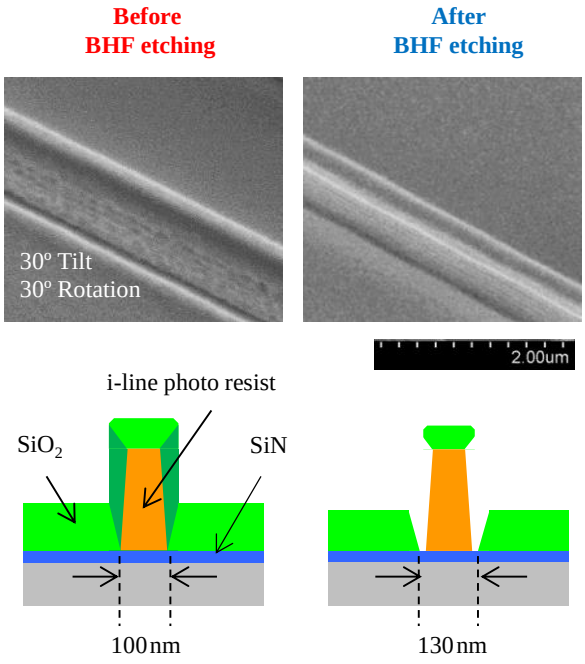


Fig. 4 SEM bird's-eye views and schematic cross-sectional images of the resist pattern before and after the BHF etching in collimated sputtering method.

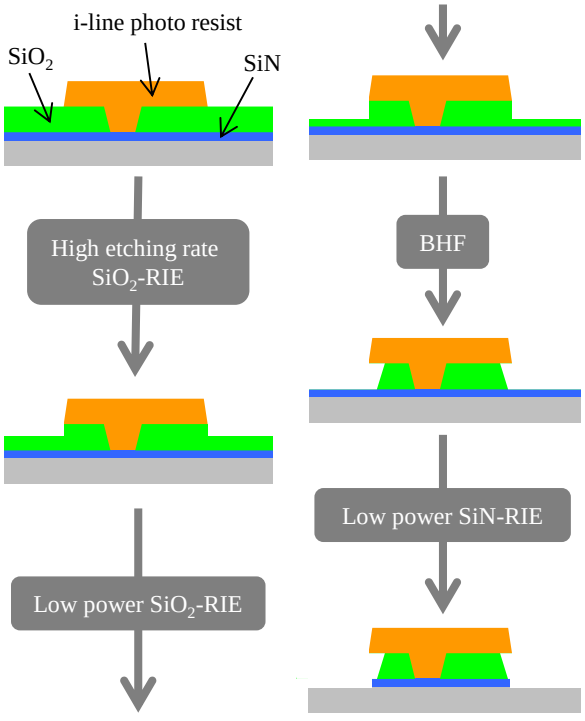


Fig. 5 Process flow of four steps SiO_2/SiN opening.

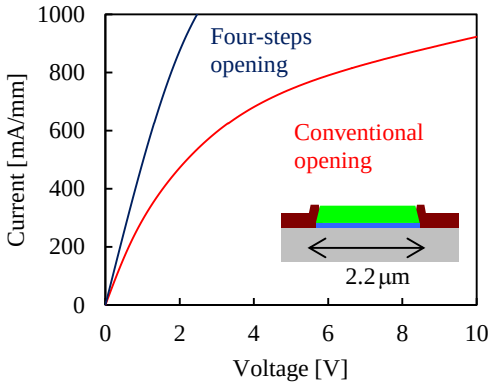
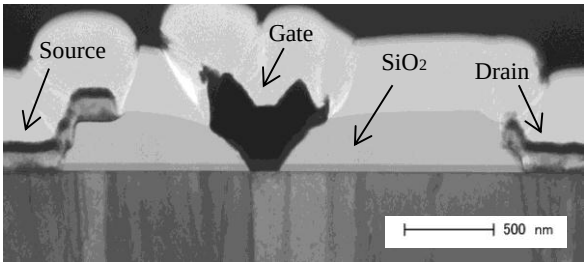
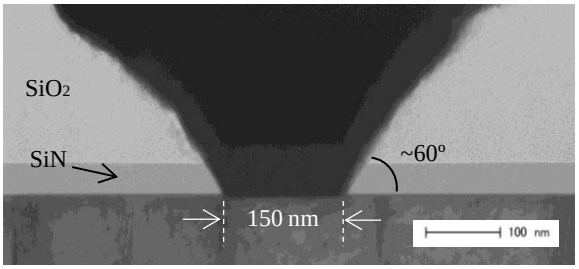


Fig. 6 *I-V* characteristics of different SiO_2/SiN opening methods.



(a) The whole.



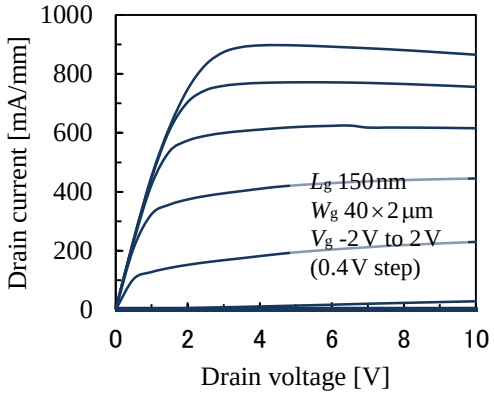
(b) Enlargement of the gate.

Fig. 7 Cross-sectional TEM views of the InAlN/GaN HEMT.

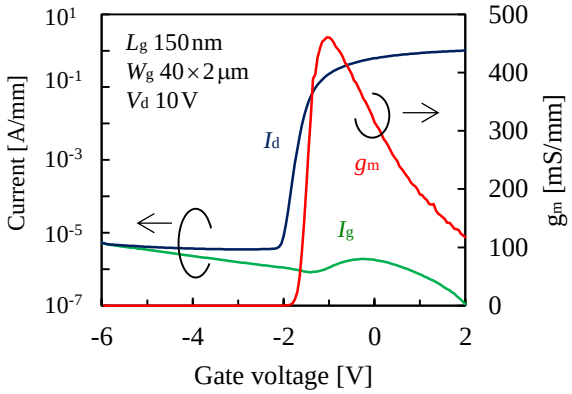
3. DC and RF Characteristics

3.1 DC characteristics

We measured the DC characteristics of the InAlN/GaN HEMT. The *I-V* curves are shown in Fig. 8. Figure 8(a) indicates the drain current I_d and the drain voltage V_d curves of the InAlN HEMT with L_g of 150 nm and the gate width W_g of 40 × 2 µm. The gate voltage V_g was swept from -2 to 2 V with 0.4-V-step. Maximum current of 900 mA/mm was obtained. The on-resistance R_{on} extracted at V_g 2 V and V_d in the range between 0 and 1.0 V was 1.8 Ωmm. Figure 8(b) indicates transconductance g_m, I_d-V_g and the gate current I_g-V_g curves at V_d of 10 V. Even if an InAlN barrier layer was used, low I_g less than 1×10^{-5} A/mm was obtained due to introduction of the GaN cap layer. Good pinch-off characteristics were observed while L_g is as short as 150 nm. The peak g_m of 460 mS/mm was achieved.



(a) Drain characteristics.



(b) Transconductance and I_d-, I_g-V_g characteristics.

Fig. 8 DC characteristics of the InAlN/GaN HEMT.

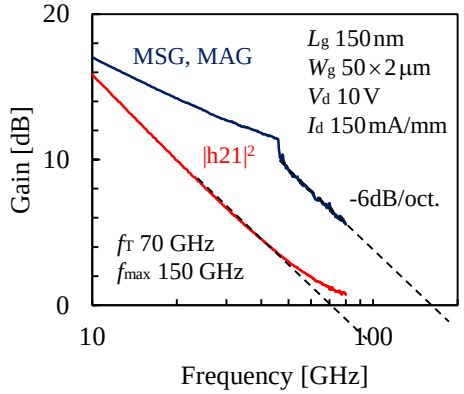


Fig. 9 Small-signal frequency response of the InAlN/GaN HEMT.

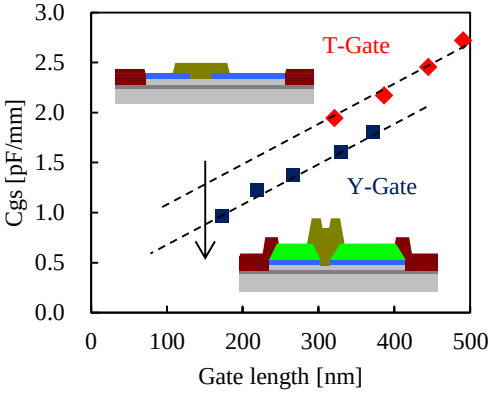


Fig. 10 C_{gs} comparison between T-gate and Y-gate of the InAlN/GaN HEMTs.

3.2 RF characteristics

The RF characteristics are shown in Fig. 9. We measured the *S*-parameters using an Agilent 8510C network analyzer for the InAlN/GaN HEMT with L_g of 150 nm and W_g of 50 × 2 μm from 10 to 80 GHz. After the pad parasitic was de-embedded, f_T of 70 GHz and maximum oscillation frequency f_{max} of 150 GHz were obtained under the bias condition of V_d of 10 V and I_d of 150 mA/mm.

We also extracted the gate capacitance C_{gs} from an equivalent circuit model obtained from the measured *S*-parameters. As shown in Fig. 10, C_{gs} of the InAlN/GaN HEMT with Y-gate was reduced by two thirds than that with T-Gate at L_g = 150 nm. We confirmed that the Y-gate process is effective for reduction in parasitic C_{gs}, and suitable for high-speed operation.

4. Conclusions

We demonstrated an optical Y-gate process. This process enables us to obtain short L_g of 150 nm and C_{gs} reduction. As a result, high-speed operation of f_T 70 GHz was successfully achieved. This simple process is suitable for low cost and high performance fabrications.

References

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