Implementation of Slanted Sidewall Gates Technology in the Fabrication of S-, X-, and Ka-band AlGaN/GaN HEMTs.

K. Y. Osipov, S. A. Chevtchenko, O. Bengtsson, P. Kurpas, F. Brunner, N. Kemf, and J. Würfl

Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH),
Gustav-Kirchhoff-Str. 4, 12489 Berlin, Germany
E-mail: Konstantin.Osipov@fbh-berlin.de, Tel.: +49 30 6392 3207, Fax: +49 30 6392 2685

Keywords: Ka-band, GaN HEMT, embedded gate technology, ZEP 520A

Abstract

Currently the so-called "embedded gate process" where the gate is processed into an insulator trench is commonly used for AlGaN/GaN HEMT gate fabrication. In this work we present a new approach for fabricating slanted sidewall embedded gates with dimensions of 500 nm, 250 nm and 100 nm. In order to perform evaluation of a new technology, standard vertical gate approach was used for fabrication of reference transistors with gate lengths of 500 nm and 250 nm. Both technologies were used for fabrication of transistors using different heterostructures appropriate for the respective gate length. For slanted gate formation thermally reflowed ZEP520A e-beam resist has been applied in conjunction with anisotropic ICP etching of a SiN_x layer. DC and large-signal RF characteristics as well as transistor yield on 4 inch SiC wafers were similar for both technologies. DIVA measurements of devices with gate length 500 nm showed significantly different drain current collapse for slanted and vertical gate transistors fabricated on wafers from different vendors. A possible explanation of this difference is given.

INTRODUCTION

This work presents the results of embedded gates implementation with slanted sidewalls in a process flow towards S-band GaN HEMTs, and X- and Ka-band GaN MMICs. As it has been shown before [1], the newly developed technology of GaN HEMT gate fabrication using ICP etching with thermally reflowed ZEP 520A e-beam resist as etch mask, allows fabrication of gates with dimensions down to 50 nm and sloped sidewall profile. This technology has several advantages compare to the standard vertical sidewall gate approach. Firstly, it has flexibility that allows fabrication of gates with lengths ranging from 500 nm down to 50 nm using the same resist mask. Secondly, this technology provides a better trench sidewall coverage with gate metal, which is considered as one of the prerequisites for highly reliable devices [2]. Last but not least, the SiN_x etching process used in this approach has significantly lower bias voltage compare to our vertical sidewall technology. The low bias etching is necessary as it ensures high mask to SiN_x selectivity and allows fabrication of gate trenches with high aspect ratios, which is mandatory for short gate fabrication. As a side effect it also reduces the risk of radiation damage and associated disadvantages of high bias etching.

EXPERIMENT

In order to compare the newly developed slanted gate technology with a standard vertical approach, transistors with 500 nm and 250 nm gates were fabricated using both technologies on wafers from different vendors. Ka-band transistors with 100 nm gates were fabricated using slanted gate technology only, because our vertical gate approach does not allow fabrication of short gates. Device heterostructures were grown by low-pressure MOVPE both on n-type and semi-insulating 4H-SiC substrates. Wafers from different vendors with nominally the same epitaxial structures were processed together in order to distinguish between epitaxial layer and process related effects. Table 1 lists the details of the epitaxial layers and basic technological features for devices optimized for the different frequency bands. Gates with lengths of 500 nm, 250 nm and 100 nm were used for S-, X- and K-band devices, respectively. In order to avoid short channel effects the gate length to gate-to-channel distance ratio needs to be adjusted [3]. However, as a short gate-to-channel distance results in a reduced 2DEG concentration this effect has to be compensated, for example, by increasing the Al mole fraction in the AlGaN

TABLE I
EPITAXY AND PROCESS DETAILS FOR DIFFERENT KINDS OF TRANSISTORS

Band	Epitaxy details				Process details		
	Cap	Barrier	Channel	Buffer	L_g (nm)	Gate profile	d_{SiNx} (nm)
S	5 nm GaN	uid 25 nm $Al_{0.18}GaN$	850 nm GaN	~1000 nm GaN:Fe	500	Slant/ Vert.	150
X	5 nm GaN	uid 18 nm $Al_{0.25}GaN$	850 nm GaN	~1200 nm GaN:Fe	250	Slant/ Verti.	100
Ka	2 nm GaN	n^+ 12 nm $Al_{0.32}GaN$	50 nm GaN	~2200 nm $Al_{0.04}GaN$	100	Slant	100

10

barrier. Thus, the gate to channel distance of S-, X- and Ka-band devices decreases from 25 nm to 18 nm and 12 nm, respectively. At the same time the Al concentration in the barrier has been increased from 18 % to 25 % and 32 %, respectively. All wafers were passivated with SiN_x deposited at 325 °C by PECVD. For slanted gate fabrication ZEP 520A resist diluted by 50% was spun and subsequently baked for 3 min at 115 °C, resulting in a final thickness of ~210 nm. After development, a resist reflow process was performed at 155 °C for 20 min followed by etching in CHF_3/SF_6 gas mixture using ICP plasma. For vertical gate trench technology the etch mask consists of two layers of 300 nm thick ARP 639.10 resist subsequently spun towards a final thickness of 600 nm. After development, etching was performed in SF_6/He gas mixture using ICP plasma. Size and profile of trench openings in SiN_x were analyzed using scanning electron microscopy (SEM). After wafer processing DC, load-pull and DIVA measurements were performed in order to obtain electrical properties and estimate transistors yield.

RESULTS AND DISCUSSION

In order to prove reliability and repeatability of the slanted gate technology, 10 different wafers were processed using vertical and slanted gate approaches. Figure 1 shows the evolution of gate trench dimensions measured in the layout and after different process steps such as resist development, resist reflow and dry etching in SiN_x. As can be seen, all transistors have the same change in trench dimensions according to the process steps. This means that the process is practically free of sizing phenomena. After trench fabrication, SEM measurements revealed that the slanted gate technology provides a good uniformity of trench dimensions on a wafer (± 5 % of nominal gate length), together with trench sidewall slopes uniformity in the range

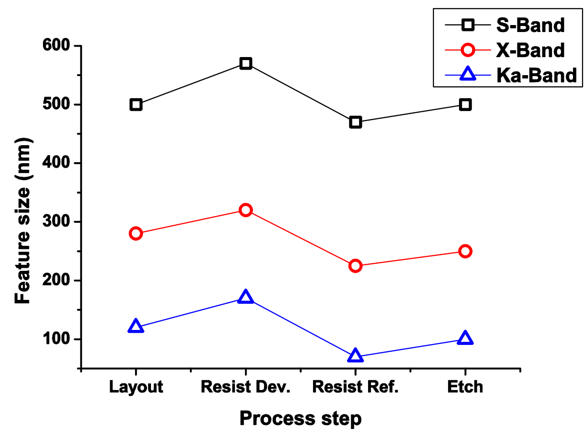

Figure 1 – Trench size after different process steps

of 72 ± 2 degrees. Wafer to wafer repeatability of trench sizes was ± 10 % of nominal gate length, with a uniformity of sidewall slope similar to that in a wafer. A first comparison of electrical characteristics was performed immediately after gate fabrication. Transistors with the same gate length showed very similar results in terms of I_{DS_max}, g_m and V_{th}, which means that both gate fabrication technologies are comparable in terms of DC properties of the resulting devices. As an example Figure 2 shows the pinch-off properties of devices fabricated on respective epitaxial designs using different gate technologies. As can be seen from the figure, V_{th} depends only on heterostructure design, but is almost independent from technology used for the gate fabrication. Moreover, good threshold voltage uniformity can be observed for transistors fabricated using both technologies. After finishing the process, large signal parameters of S- and X-band transistors with a total gate periphery of 8×250 µm and 8×125 µm, respectively, were estimated. Table 2 summarizes the results of load-pull measurements. S-band devices were measured at 2 GHz and

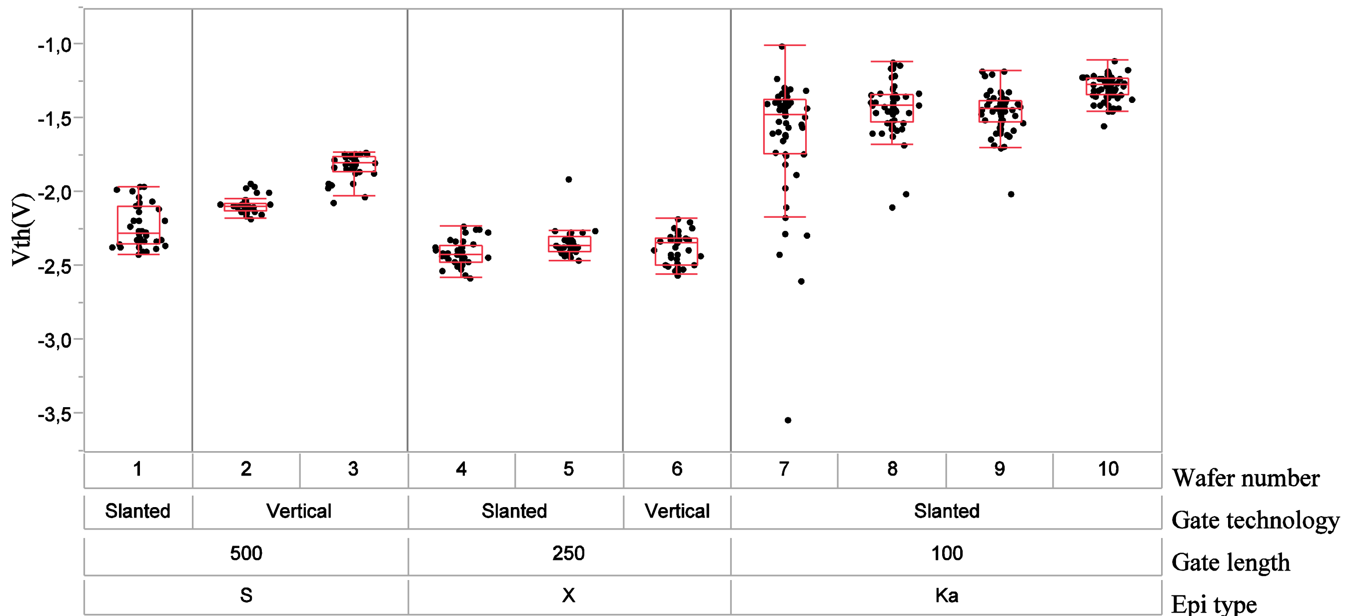

Figure 2 – Results of threshold voltage measurements for S-, X- and Ka-band transistors, fabricated using slanted and vertical gate technologies.

TABLE II
RESULTS OF LOAD-PULL MEASUREMENTS OF S- AND X-BAND TRANSISTORS

Band	Gate module			
	Vertical		Slanted	
	Pout(W/mm)	PAE (%)	Pout(W/mm)	PAE (%)
C	3,3	51	3,5	53
X	4,8	48	5	49

quiescent bias point with V_{DS} = 28 V and I_{DS} = 0.3×I_{DS_max}. X-band transistors were biased at V_{DS} = 28 V, I_{DS} = 0.1× I_{DS_max} and measured at 10 GHz. As can be seen from the table, transistors with slanted gates demonstrate comparable large signal performance with reference transistors in both frequency bands. DC functional testing was performed in order to estimate transistors yield. As an example, Figure 3 shows the results for two wafers with X-band transistor, fabricated using different gate technologies. As can be seen, for both technologies transistor yield is about 85 %-90 %, a similar result was achieved for all tested transistors with different gate lengths.

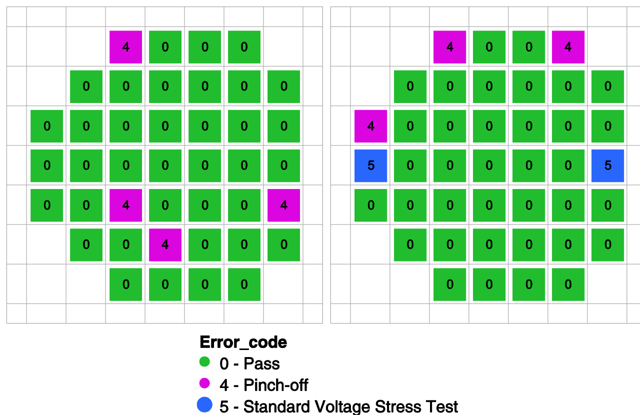

Figure 3 – Results of functional tests of X-band transistors with 12×250 um total gate periphery fabricated on 4 inch s.i. SiC wafers using slanted gate technology (right) and vertical gate technology (left).

Results of DIVA measurements of S-band transistors are presented in Figure 4. During these measurements transistors were biased at different quiescent bias points and values of drain current were extracted at instantaneous voltages V_{DS} = 10 V and V_{GS} = 1 V. At quiescent bias V_{DS} = 0 V and V_{GS} = 0 V all transistors showed very similar drain current of about 0.65 A/mm. This value was used for normalization of all results obtained at different bias conditions. For the quiescent point V_{DS} = 0 V and V_{GS} = -7 V a decrease of the drain current by 10 % to 20 % can be observed for all transistors fabricated on wafers from vendor 1, and for slanted gate transistors on wafers from vendor 2. At the same time, significantly higher (from 25 % to 65 %) drain current collapse was measured for vertical gate transistors on wafers from vendor 2. Further increase of stress at quiescent points V_{DS} = 30 V and 50 V gives proportional decrease of instantaneous drain current for all transistors. This behavior points out that current collapse up to 80 % observed for standard transistors on wafer from vendor 2 is caused by gate lag phenomena and therefore related to processes that occur at the vicinity of the gate rather than in buffer layer.

In order to explain the mechanism of current collapse we analyzed gate leakage current measurements and found that the mean gate leakage currents on wafers from vendors 1 and 2 were 8.3×10^{-5} A/mm and 4.1×10^{-7} A/mm, respectively. The main path of the leakage current on wafers from vendor 1 is through the AlGaN barrier. Thus, the electric field in the vicinity of the drain-side gate edge is

10

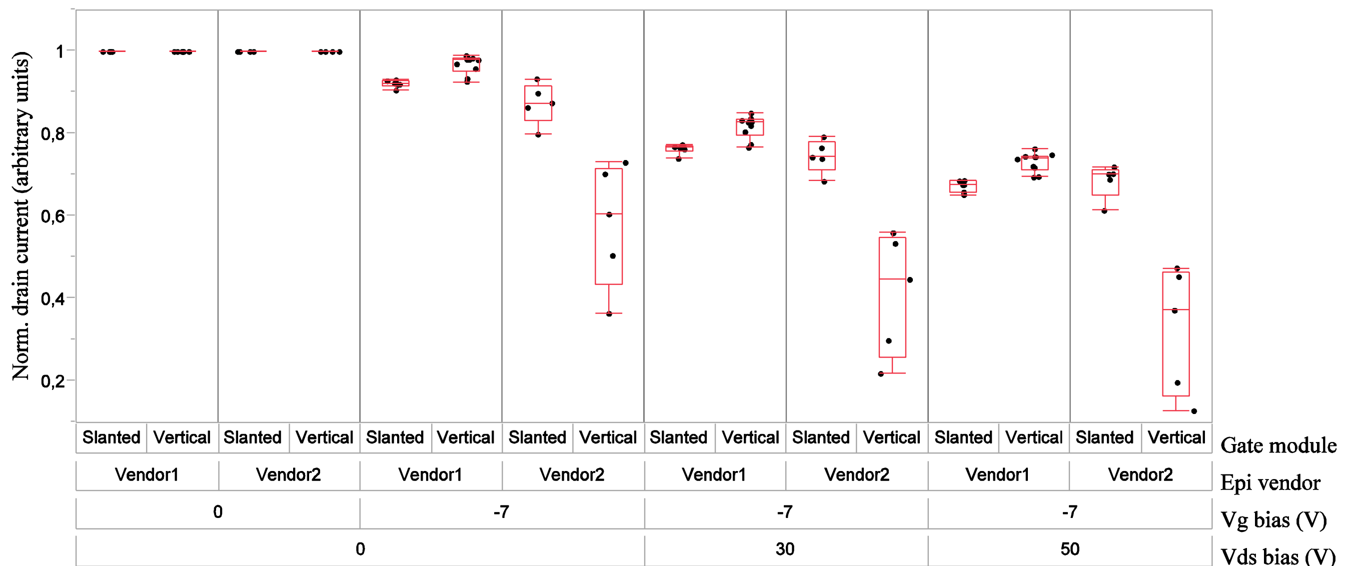

Figure 4 – Normalized DIVA results of drain current measurements at different quiescent bias points (and instantaneous voltages V_{DS} = 10V and V_{GS} = 1V) for S-band transistors fabricated using both technologies on wafers from two different vendors.

reduced, which also reduces the probability of trapping electrons injected from the Schottky gate at reverse bias and no trapping occurs. On the other hand wafers from vendor 2 have highly resistive barrier, which means that initially the electric field at the drain-side edge of the gate is relatively high leading to a pronounced injection of electrons at high reverse gate bias. These electrons get trapped immediately providing a negatively charged area in the vicinity of the gate. This is causing dispersion phenomena as the traps cannot be de-trapped within short time frames. On these wafers the difference between slanted and standard gates can be explained by a significantly lower concentration of traps induced during the SiN_x etch process used in slanted gate technology. The lower trap concentration under slanted gates is most probably the result of less damage of the semiconductor surface due to the different SiN_x etching conditions. Another explanation of this phenomenon can be the slanted gate, working as a local field plate and causing a reduction of the electric field peak, which prevents trap charging and eliminates dispersion. In order to clarify the mechanism of this process, further investigation is required.

CONCLUSIONS

The newly developed technology of embedded GaN HEMT gate fabrication has been successfully implemented in the process flow of S-, X- and Ka-band transistor fabrication. Reference devices with gate lengths of 500 nm and 250 nm and vertical sidewalls were used for comparison in order to evaluate the quality of the new technology and possible drawbacks. Transistors with 100 nm gate lengths were fabricated using slanted gate technology only. Measurements of DC and large-signal characteristics of S- and X-band transistors showed similar performance and process yield for both vertical and slanted sidewall gates. Results of DIVA measurements unveiled significant improvement of drain current dispersion for slanted gate transistors fabricated on wafers with a highly resistive AlGaN barrier layer. This phenomenon can be explained by less damage of the semiconductor surface during SiN_x etching, or by local reconfiguration of the electric field under the gate due to the slanted gate trench profile.

ACKNOWLEDGEMENTS

The authors would like to thank the team of microwave department for the transistor measurements. Additionally, support from the process technology department is appreciated. This work was supported by “GaNSaT” project (EC – Contract nº 606981) in boundaries of 7th Framework Program Research.

REFERENCES

[1] K. Y. Osipov, W. John, N. Kemf, S. A. Chevtchenko, P. Kurpas, M. Matalla, O. Krüger, and J. Würfl, “Comparison of different methods for GaN HEMTs gate fabrication”, WOCSDICE, 2013.

[2] K. Y. Osipov, W. John, N. Kemf, S. A. Chevtchenko, P. Kurpas, M. Matalla, O. Krüger, and J. Würfl, “Fabrication technology of GaN/AlGaN HEMT slanted sidewall gates using thermally reflowed ZEP resist and CHF3/SF6 plasma etching”, CS Mantech Conf., 2013.

[3] G.H. Jessen, R.C. Fitch, J.K. Gillespie, G. Via, A. Crespo, D. Langley, D.J. Denninghoff, M. Trejo, E.R. Heller, “Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices,” IEEE Trans. on Electron Dev., vol. 54, no. 10, pp. 2589 - 2597, Sep. 2007.

ACRONYMS

RF: Radio Frequency
DC: Direct Current
HEMT: High Electron Mobility Transistor
ICP: Inductively Coupled Plasma
2DEG: 2 Dimensional Electron Gas
MMIC: Monolithic Microwave Integrated Circuit