Sputtered Iridium Gate Module for GaN HEMT with Stress Engineering and High Reliability

Richard Lossy[1], Hervé Blanck[2] and Joachim Würfl[1]

[1]Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Gustrav-Kirchhoff-Straße 4, 12489 Berlin, Germany
e-mail: lossy@fbh-berlin.de, Phone: +49 30 63922774 Fax: +49 30 63922685

[2]United Monolithic Semiconductors, Wilhelm-Runge-Strasse 11, 89081 Ulm, Germany

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Abstract

A new gate module with iridium as a degradation resistant Schottky contact for GaN based HEMT devices is developed. Conformal deposition of Schottky and barrier metal in the gate trench provides sealing of the semiconductor. Sputtering is the enabling technology that provides low stress iridium contacts from low damage processing. Patterning of the gate contact is achieved by a subtractive method. Robustness and reliability of the devices were investigated by step-stress-test, IDQ-test, storage test and DC life-test. Results are compared to a conventional deposition method with evaporated platinum contacts.

Introduction

AlGaN/GaN HEMT RF transistors are rapidly developing due to their high output power density, high operation voltage and high input impedance. Impressive progress has been achieved in improving the performance of such devices. Many RF systems already rely on GaN transistors. Open points still remain related to current collapse and leakage current and its relation to reliability issues. The quality of the epitaxial material can have a strong impact on the transistor performance. But as the epitaxial quality has matured it has become more obvious that process modules such as gate and ohmic contacts as well as surface passivation influence and limit the power performance of GaN HEMTs significantly. Due to the combination of high electric fields and large current densities close to the drain side edge of the gate, most of the heat generation takes place in this region. Therefore, a thermally stable Schottky barrier is a key condition for acceptable reliability behavior. Generally, the gate leakage current has to remain at a low level, as excess leakage current decreases the breakdown voltage significantly. In many cases leakage current increases as the device degrades. For the traditionally used NiAu gates fabricated by physical vapor deposition a thermal instability of the metal stack has been reported by different sources [1]. This results in a gradual electric degradation of the gate contact. The mechanisms associated to this are quite complex in nature. Nickel silicide formation between Ni and the SiNx passivation and subsequent Au diffusion to the Ni-GaN interface is under debate. Gold diffusion from the gate head is another source for deterioration of HEMT performance and reliability. It has been found that gold may be diffusing via the gate foot sidewall towards the Schottky barrier [2]. The shadowing effect from directional deposition by evaporation prevents full coverage of the Schottky metal in the gate trench and in this way enables sideway diffusion. This in turn not only demands for more resistant Schottky metallization but also requests hermetic sealing of the Schottky metal interface from diffusion.

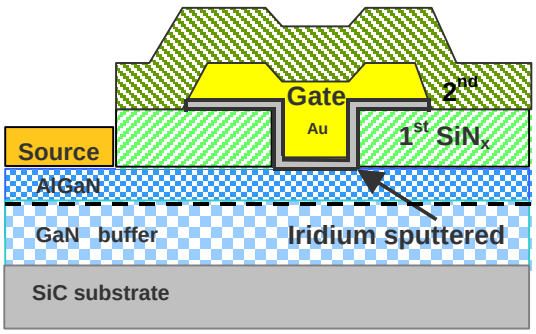

Fig.1: Sketch of gate module with sputtered Schottky gate

Several attempts have been made to replace the Schottky gate metal by more resistant metallization schemes. In particular, refractory metals exhibiting very high melting point are promising candidates [3]. On the other hand, stress in evaporated thin films is rather high for high melting point metals. This and the extreme lateral dimensional ratio of the gate could lead to poor adhesion and roll up of the gate contact. Therefore, stress engineering is highly desirable to promote well adhering Schottky metal in the gate trench.

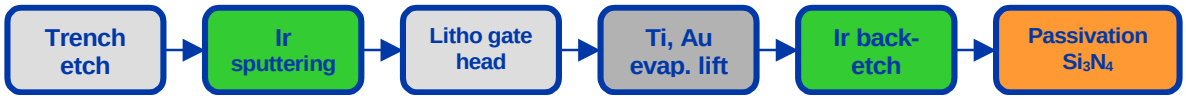

Fig.2: Processing scheme of gate module with sputtered Schottky gate

Approach

In this study a new approach has been investigated which aims to overcome the reliability and yield problems from evaporation and lift-off.

The metallurgical barrier effect of the Schottky contact metal and hermetic sealing are accomplished by conformal deposition of the Schottky metal over the gate trench and the adjacent area. Isotropic deposition methods are required for conformal growth of the Schottky metal. Thus, sputter deposition is the preferred method here. Iridium as a refractory metal with a melting point of 2460 °C and simultaneously providing a high work function > 5 eV is a prime candidate.

Isotropic deposition methods are not compatible with traditional lift-off as a masking technique. Particularly, lift-off technologies require strict anisotropic deposition. Therefore, forming of the Schottky contact electrode has been changed from an additive structuring method, i.e. lift-off, to subtractive structuring.

Refractory metals tend to build rigid layers due to their high mechanical elastic modulus. This is beneficial for a metallurgical barrier but may adversely effect performance when mechanical stress during film growth is not properly managed and may even lead to delamination of the film. Sputtering technology typically yields compressive metal films but by choosing appropriate plasma parameters stress can be adjusted from compressive to tensile. Here, iridium films are adjusted to stress levels much lower than 100 MPa.

Both RF-power as well as high voltage-switching applications suffer from electronic traps that are responsible for poor performance under dynamic operation. Trap generation in the vicinity of the gate contact due to energetic particles from the sputter plasma has to be avoided by choosing suitable processing parameter. RF-data will be chosen as a benchmark of this technology against the evaporated standard.

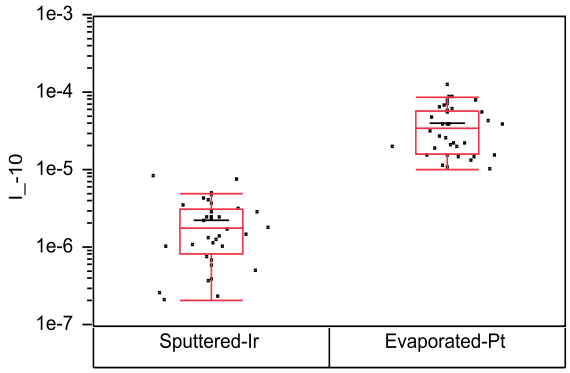

Fig.3 Gate diode reverse leakage I_-10V measured at V_G = -10 V and RT

Experimental

HEMT devices are grown on semi-insulating SiC substrate material by MOVPE. The AlGaN/GaN heterostructure is fabricated on an iron doped buffer layer. Device fabrication starts with ohmic contacts and device isolation. After this the gate module is processed with silicon nitride deposition and dry etch of the slanted gate trench. All electrical data presented here are from devices having 0.25 µm gate foot. We use a subtractive technique for definition of the contact metal. First, the Schottky gate metal is deposited by sputter deposition of iridium. Parameters for deposition are chosen in a way that conformal coverage of the surface as well as low film stress and low surface damage are achieved. Low stress of the Schottky metal in contact with the semiconductor is beneficial to minimize degradation related to the inverse-piezo-effect (IPE). On the contrary, deposition of the Schottky contact by evaporation always results in high tensile stress of deposited metal thus adding to stress from lattice mismatch and IPE.

Results

Here, we report data collected for the experiments performed on identically processed GaN-on-SiC devices, except for the gate metallization module. The gate length is 0.25 µm. Sputtered iridium gate metallization is compared with evaporated platinum.

Comparison of the dc data from the 2 metallization schemes shows only minor differences for g_m (240 mS/mm), pinch-off (-3.2 V) and I_{DSmax} (700 - 750 mA/mm). There are remarkable differences in leakage currents as shown for the gate diode reverse bias (Fig. 3). For the sputtered iridium leakage is slightly above 10^{-6} A whereas evaporated platinum is more than a decade higher. Also, a difference in barrier height is observed (Fig. 4). Since the work function of both materials is very close (5.5 - 5.8 eV)

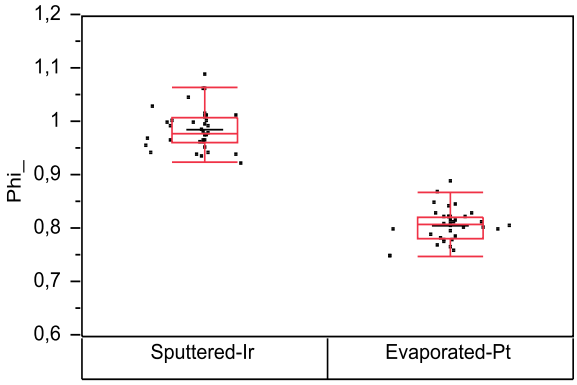

Fig.4 Gate diode barrier height Phi_B (eV)

the different stress levels of the metal films may come into consideration. Annealing studies that generate different stress pattern support this argumentation.

S-parameters are compared for the 2 gate modules. Small signal operation at a bias of 40 V, 50 mA/mm is performed for devices of 0.1 mm total gate width and MAG values are extracted for the frequencies of 2, 10 and 18 GHz. For sputtered iridium devices at these frequencies the MAG values are 22.7, 15.5 and 11.5 dB and the corresponding data for evaporated platinum are 22.2, 15.1 and 11.3 dB showing minor differences only.

Load pull data are taken on devices having a total gate width of 1 mm operated at 50 V_D, and 2 GHz. Large signal gain Gt is in the range 26.5 ± 0.5 dB for both deposition methods. RF-power for iridium sputtered devices yields 4.8 W/mm, whereas evaporated Pt shows a slightly higher power density of 5.9 W/mm which in part is due to slight differences in sheet resistance. The power added efficiency is of huge importance not only for optimum design of amplifiers but here also serves as an indicator of additional traps introduced by the sputtering process during metal deposition. PAE ranges here from 59 - 61 % for both deposition methods, showing no difference between both types. This is indicating that deposition conditions for sputtering can be chosen in an appropriate way for gate metal deposition.

ON-WAFER ROBUSTNESS

Step-stress-tests were performed under high temperature reverse bias condition (HTRB). Test conditions for the devices are a base plate temperature of 150 °C and pinch-off condition at V_{GS} = -7 V. Starting at a drain voltage of V_{DS} = 25 V the drain voltage is increased by 5 V every hour up to a limit of 100 V. If the leakage current exceeds 1 mA/mm before 100 V the test is stopped and the device is treated as failed and not considered for further reliability investigations. The devices used in this test have a total gate width of 250 µm (2x125 µm). For all tested devices leakage currents for gate and drain have equal absolute values, indicating a current path between gate and drain contacts (Fig. 5).

For transistors with sputtered iridium metallization the leakage current starts with a few µA and ends typically in the 10 - 30 µA range corresponding to 40 - 120 µA/mm never exhibiting any catastrophic failure or steep increase. At lower voltages up to 50 V_D both currents increase slightly when the drain voltage increases one step but then settle at a lower level until the stress is increased again. Above 60 V no reaction on the drain voltage is visible and only a ripple most likely from the temperature regulator is visible. Similar to the results of Fig. 3 the level of leakage is more than a decade higher for evaporated platinum. Also a pronounced ripple is visible here that could indicate trapping effects.

IDQ stability test is performed at V_{DS} = 50 V and I_{DS} = 50 mA/mm at a base plate temperature of 150 °C. This test is performed on-wafer for a time of 16 hours. At the starting point the gate voltage is adjusted for the required drain current and then the gate voltage is kept constant for the entire test (Fig. 6). After the initial phase of 2 - 3 h gate and drain currents are constant. For the sputtered iridium devices a gate current of typically 5 µA is measured. For the evaporated platinum gates a current of 100 - 200 µA flows under the same condition.

LIFE TEST

DC life testing is done using thermal acceleration as a means for measurement of the useful lifespan of the devices. Here the Arrhenius model is used for quantification which implies a pure thermal acceleration and additional acceleration mechanisms like field related acceleration have to be excluded during this test. Thermal stress is applied by a heated base plate and DC power dissipation in the device with power held constant. The later is accomplished by regulating the gate voltage at constant drain current during the test. Prior to stressing the device a calibration of the transistor channel temperature is performed by Raman spectroscopy. The peak temperature located under the gate edge to the drain which is not accessible by the laser beam is calculated from measurements of the visible part in conjunction with thermal modelling. Intermediate points during the test at 24, 48, 96, 192, 384, 768 and 1000 h are used for a thorough characterization of the devices at room temperature. From these data I_{DS_max} is taken as a measure for degradation. The time for a 10 %

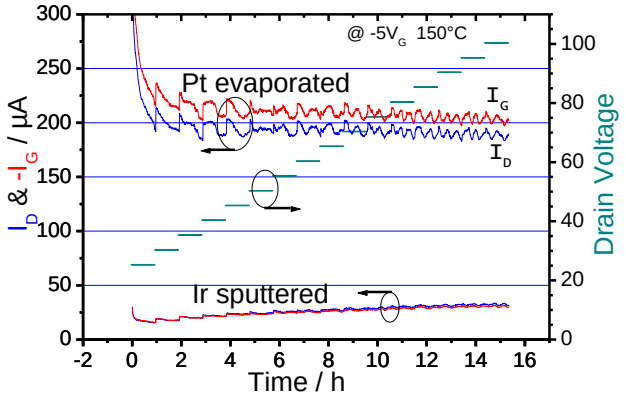

Fig.5 Step-Stress-Test under high temperature reverse bias condition (HTRB), -5 V_G, 150 °C

decrease of I_{DS_max} is taken for further calculation. The life test is performed on packaged devices with 8 x 125 µm total gate width.

Taking the 10 % degradation of I_{DS_max} from the data sets an Arrhenius plot for lifetime estimation can be obtained (Fig. 7). Channel temperatures were set from 290 °C to 355 °C. From the averaging procedure a line for estimated lifetime is obtained. Taking this line 10^8 h (~11,000 years) for a channel temperature of 175 °C could be calculated. Furthermore, the activation energy calculated from this lifetime line is 2.0 eV.

Conclusion

A gate module using iridium sputter technology with stress engineering and low sputter damage was developed. The technology was tested with 0.25 µm gates.

Comparison of sputtered iridium to evaporated platinum shows much lower leakage for the sputtered gate module. Sputter gates exhibit reverse leakage currents around 20 µA. Devices prepared with evaporated platinum have a gate leakage more than one decade higher than those prepared by the sputter

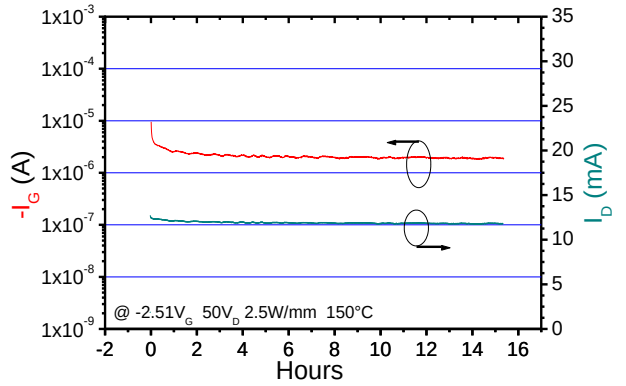

Fig.6 IDQ-Test at 50V_D , 50 mA/mm and 150°C sputtered iridium gate metallization

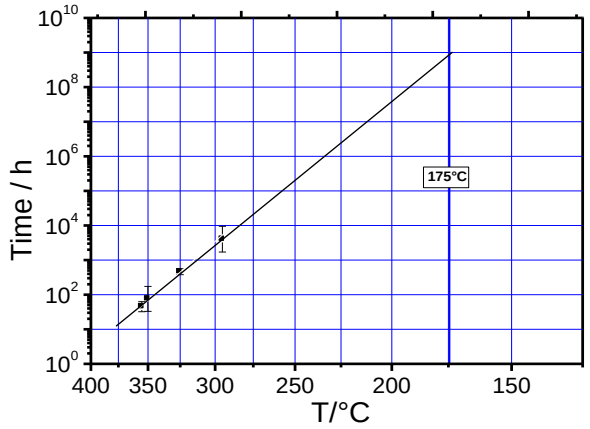

Fig.7 Arrhenius plot of sputter deposited Iridium gate module

process.

On-wafer HTRB step-stress-tests at 150 °C are performed up to 100 V_{DS}. Tests reveal no sign of substantial increase of leakage current and also no onset of any catastrophic behavior could be detected. Again, a comparison of sputtered iridium shows gate currents of 20 µA whereas the evaporated platinum has leakage currents around 200 µA.

Also, IDQ-tests remain at low and stable leakage level in the 10^{-8} A/mm range.

DC life-tests were performed. Thermal acceleration was used with channel temperatures ranging up to 355 °C. From the Arrhenius figure an expected lifetime above 10^8 hours at 175 °C channel temperature is calculated.

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Acronyms

HEMT: High Electron Mobility Transistor
HTRB: High Temperature Reverse Bias
IDQ: Quiescent Drain Current
MAG: Maximum Available Gain
PAE: Power Added Efficiency