Surface Recombination and Performance Issues of Scaling Submicron Emitter on Type-II GaAsSb DHBTs

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Abstract

Type-II GaAsSb DHBTs have been designed, grown and fabricated. DC and RF performances of devices with varying emitter widths have been characterized and compared. It is found that the emitter size effect limit the current gain of scaled devices and emitter ledge can help mitigating the emitter size effect. Also, RF measurement and modeling show that the base resistance is the limiting factor for the high frequency performance of the scaled device.

INTRODUCTION

Type-II GaAsSb/InP DHBT has a staggered Type-II base collector band alignment, which eliminates the current blocking issue found in Type-I InGaAs/InP DHBT [1]. Due to its high breakdown voltage, high gain, and better linearity, Type-II DHBT has found wide applications in RF, mixed-signal IC, and communication instrumentation [2]. To improve the current gain and high frequency performance, composition-graded GaAsSb, InGaAsSb, and AlGaAsSb base and doping-graded GaAsSb base have been studied [3-11]. Currently, f_T/f_{MAX} = 670/185 GHz has been reported for a 0.52x7.6 μm^2 DHBT with composition graded InGaAsSb base [6]. A 0.22x4.4 μm^2 composition graded GaAsSb base DHBT has demonstrated f_T/f_{MAX} = 428/621 GHz [5]. Doping graded base GaAsSb DHBT has also reported f_T/f_{MAX} = 470/540 GHz [11].

To push the Type-II GaAsSb DHBT operating frequency toward THz frequency range, lateral scaling is needed to reduce device capacitances and resistances. However, as the emitter width of a DHBT is scaled down, the current gain and 1/f noise of the device will degrade due to the emitter peripheral surface recombination current [12, 13]. Recently, Type-I InGaAs/InP HBTs with a thin InP ledge structure have demonstrated significant improvements in the current gain and reliability due to the reduction of emitter peripheral surface recombination current [14]. A Type-II GaAsSb/InP DHBT with a thin InGaAsP ledge and Pt-sinking-through base contact has also been proposed [15]. In this paper, we studied the emitter size effect of Type II GaAsSb DHBTs with three different epi-layer structures of varying doping and composition grading. It was found that emitter peripheral recombination current can seriously reduce the current gain of all three Type-II GaAsSb DHBTs. An emitter ledge process has been developed and found to be effective in improving current gain for Type-II GaAsSb DHBT. In addition, RF characterization was performed and it showed that the base resistance is the limiting factor for the high frequency performance of the scaled device.

LAYER STRUCTURE AND DEVICE FABRICATION PROCESS

The epitaxial layer for the devices in this paper was grown by Molecular Beam Epitaxy on semi-insulating InP substrate. The detailed layer structure of a doping graded base Type-II GaAsSb DHBT (DHBT A) is shown in Table I. Devices with emitter widths ranging from 0.38 to 0.16 μm were fabricated in a standard triple-mesa wet etch process [4].

	Material	x	Thickness (Å)	Dopant	Level (/cm^3)	Type
Cap	In(x)Ga(1-x)As	0.53 to 1	350	Si	Maximum	N+
Cap	In(x)Ga(1-x)As	0.53	100	Si	Maximum	N+
Emitter	InP		700	Si	Maximum	N+
Emitter	InP		100	Si	2.0E+18	N
Emitter	InP		200	Si	4.0E+17	N
Emitter	In(1-x)Al(x)P	0.1 to 0	175	Si	4.0E+17	N
Base	GaAs(x)Sb(1-x)	0.5	200	C	8.24E+19 to 1.7E20	P+
Collector	InP		1,200	Si	2.0E+16	N
Subcollector	InP		500	Si	Maximum	N+
Subcollector	In(x)Ga(1-x)As	0.53	350	Si	Maximum	N+
Subcollector	InP		3,500	Si	Maximum	N+
Etch Stop	In(x)Ga(1-x)As	0.53	100		UID	
Substrate	InP					

TABLE I: EPILAYER STRUCTURE OF DHBT A

EMITTER SIZE EFFECT OF TYPE-II GAASSB DHBTS

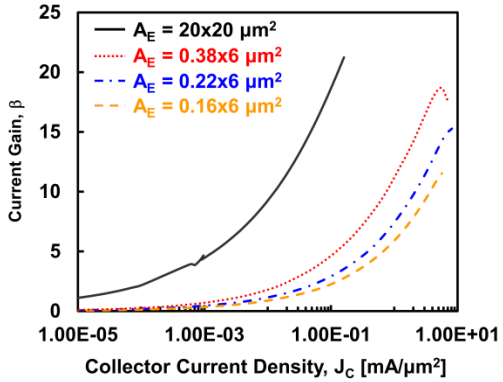

Fig. 1. (Color online) Current gain vs collector current density for devices with different emitter widths.

Figure 1 shows the DC current gain vs collector current density for the doping graded Type-II GaAsSb DHBTs with different emitter widths. Due to emitter peripheral recombination current, the maximum current gain decreases from 19.5 to 13.1 as emitter width decreases from 0.38 μm to 0.16 μm. To extract emitter peripheral surface recombination current density coefficient K_{SURF}, we plot base current J_C/β as a function of P_E/A_E at a given collector current density. The total base current could be written as $J_C/\beta = J_{IN} + K_{SURF} \cdot P_E/A_E$. Here J_{IN} is the intrinsic base current, K_{SURF} is the emitter peripheral surface recombination current density, P_E is emitter peripheral length, and A_E is the emitter area. Figure 2 shows the J_C/β vs P_E/A_E plot at collector current density J_C of 100 μA/μm^2.

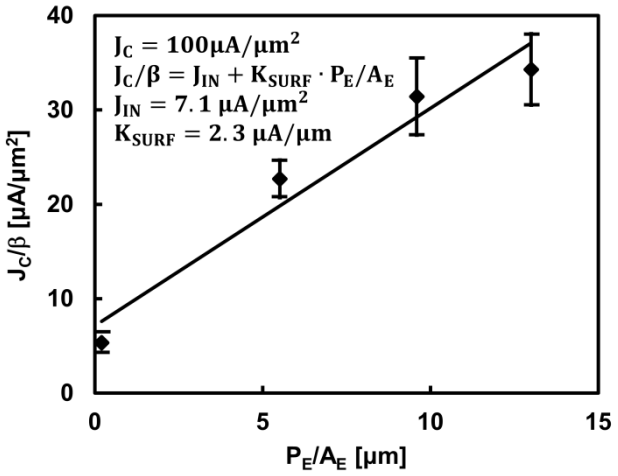

Fig. 2. (Color online) $J_C/\beta = J_{IN} + K_{SURF} \cdot P_E/A_E$ for different emitter widths at collector current density of J_C = 100 μA/μm^2.

Figure 3 shows the extracted K_{SURF} value of three different Type II GaAsSb DHBTs at different collector current densities. DHBT A is the doping graded DHBT described in Table I. DHBT B has a composition graded GaAsSb base [4] and DHBT C has a composition Graded AlGaAsSb base [9]. From Figure 3, we can see that for all three Type-II GaAsSb DHBTs, K_{SURF} increases almost linearly as J_C increases, even at high collector current densities (J_C ~ 4 mA/μm^2). Thus, emitter peripheral recombination current reduces current gain at both low and high current density. For DHBT A, when the device is biased at $J_C = 4\ mA/\mu m^2$, the intrinsic base current $J_{IN} = 144.0\ \mu A/\mu m^2$ and $K_{SURF} = 17.5\ \mu A/\mu m$. For a 0.22x3 μm^2 device, $P_E/A_E = 9.76\ \mu m^{-1}$, we can see that extrinsic base recombination current is $K_{SURF} \cdot \frac{P_E}{A_E} = 170.8\ \mu A/\mu m^2$, which is larger than J_{IN}. So, the emitter peripheral surface recombination current is a significant part of the base current and can seriously reduce the current gain of submicron DHBTs.

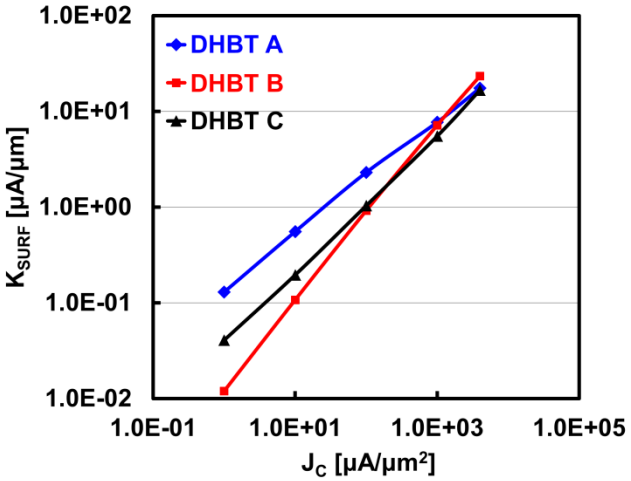

Fig. 3. K_{SURF} vs collector current density.

DHBTs With Emitter Ledge Structure

To reduce emitter peripheral recombination current, a controlled emitter etch process has been developed for DHBT A to form an AlInP emitter ledge. The process flow is shown in Figure 4. First, emitter mesa was formed by wet etch using emitter metal as the etching mask. The etching time of the InGaAs contact layer was controlled to form a desired emitter undercut. Then the InP and part of AlInP layer were etched away using diluted HCL. The etching time was controlled in order to leave a thin and lightly doped AlInP layer. After that, a layer of SiN_X was deposited using PECVD and etched back using RIE to form a SiN_X protection mask. Then, the remaining AlInP layer was etched away using HCL to expose the base surface for base metal deposition. Finally, the base metal is deposited in a self-aligned process to minimize the base resistance.

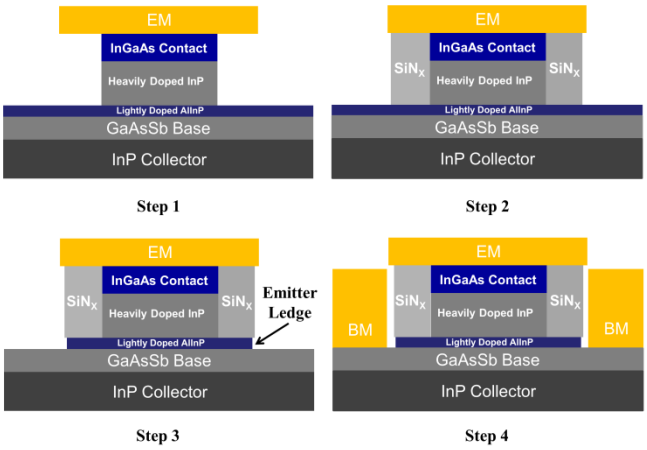

Fig. 4. Process Steps for Emitter Ledge

The InGaAs emitter contact layer etch time has been controlled to form the desired emitter ledge width (the distance between the emitter mesa and base metal). Figure 5

shows the Gummel characteristics of a 0.13x4 μm^2 device with emitter ledge width of 160 nm. The maximum current gain for the 0.13x4 μm^2 device is 33.5, which is about 2.5 times higher than that of the 0.16x6 μm^2 device without emitter ledge shown in Figure 1.

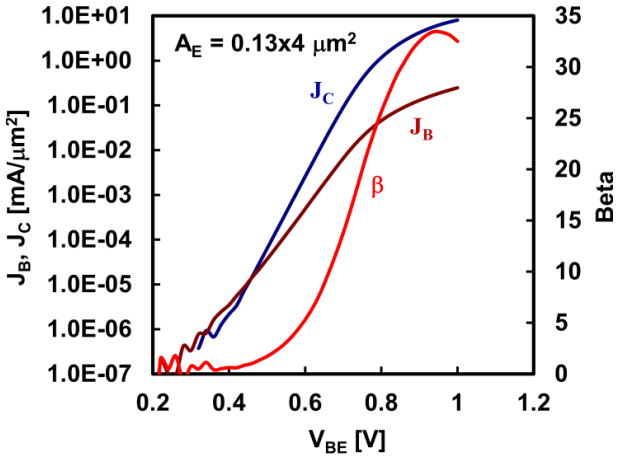

Fig. 5. Gummel characteristics of a 0.13x4 μm^2 device with emitter ledge width of 160 nm .

Figure 6 compares the extracted K_{SURF} value of the doping graded base Type-II GaAsSb DHBTs with varying emitter ledge widths. It is shown that devices with wider emitter ledge have lower emitter peripheral recombination current density. Thus, a wider emitter ledge is favorable for improving current gain and reducing 1/f noise. However, having a wider emitter ledge adversely affects the speed performance of the device, since it increases the base-collector capacitance and extrinsic base resistance. In addition, after a certain point, further increasing the emitter ledge width will have diminishing effect in reducing K_{SURF}, as shown in Figure 6. Therefore, there exists an optimal point for the emitter ledge width for a given DHBT structure.

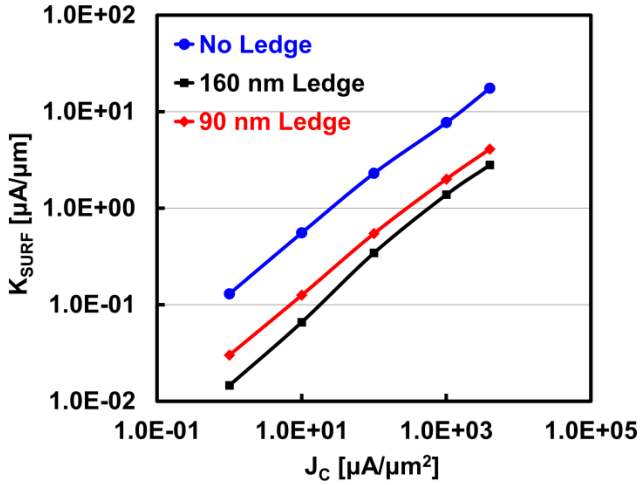

Fig. 6. K_{SURF} vs collector current density for devices with different emitter ledge widths.

RF Performance Of Deeply Scaled Type-II GaAsSb DHBTs

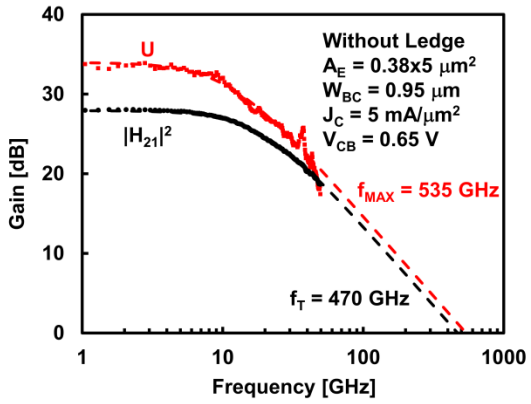

Fig. 7. (Color online) Current gain $|H_{21}|^2$ and Mason's Unilateral gain U as functions of frequency showing f_T/f_{MAX} = 470/535 GHz extracted using single-pole fitting method.

In order to study the RF performance, we performed small signal measurement and modeling for devices with different emitter widths. The devices' S-parameters were measured using an Agilent E8364A PNA. The network analyzer was calibrated using an off-wafer SOLT calibration standard, with measurements of an on-wafer open and short to de-embed pad capacitance and inductance. The maximum RF performance of a 0.38x5 μm^2 device is f_T/f_{MAX} = 470/535 GHz, measured at J_C = 5 mA/μm^2 and V_{CB} = 0.65 V, as shown in Figure 7. We also measured f_T/f_{MAX} = 455/580 GHz for a 0.19x5 μm^2 device with 90 nm emitter ledge, biased at J_C = 5 mA/μm^2 and V_{CB} = 0.65 V. Ideally, f_{MAX} performance should be proportional to $1/\sqrt{W_E}$, where W_E is emitter width, but this was not the case when scaling from 0.38 μm to 0.19 μm because the base-collector mesa and base-metal-to-emitter-mesa spacing could not be decreased proportionally with W_E.

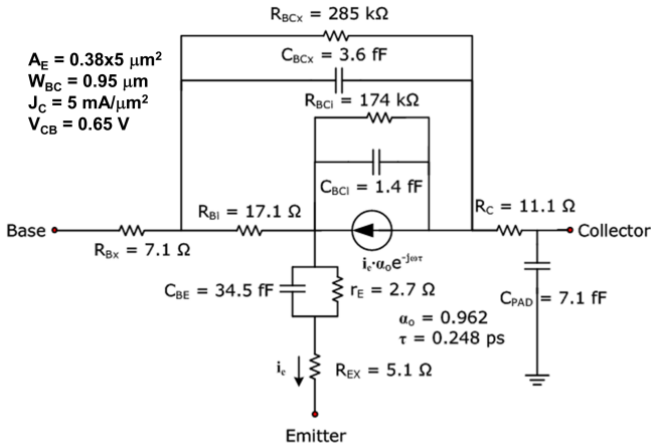

Fig. 8. (Color online) Small-Signal Model of a 0.38x5 μm^2 device.

To find the limiting factors of RF performance of scaled down devices, small signal modeling was performed. Figure 8 shows the small-signal model for the 0.38x5 μm^2 device with W_{BC} = 0.95 μm, biased at J_C = 5 mA/μm^2 and V_{CB} = 0.65 V. Here, W_{BC} is the base-collector mesa width. Important small-signal model parameters such as C_{BCi}, C_{BCx}, R_{Bi} and R_{Bx} for the two devices are compared in Table II.

	f_T (GHz)	f_{MAX} (GHz)	C_{BCi} (fF)	C_{BCx} (fF)	R_{Bi} (Ohm)	R_{Bx} (Ohm)
A_E = 0.38x5 μm^2 W_{BC} = 0.95 μm, No Ledge	470	535	1.4	3.6	17.1	7.1
A_E = 0.19x5 μm^2 W_{BC} = 0.8 μm, 90 nm Ledge	455	580	0.7	3.3	23.3	9.2

Table II: Small signal model parameters for the two devices

As shown in Table II, base-collector capacitance C_{BC} is reduced as emitter width is reduced from 0.38 μm to 0.19 μm, however base resistance is increased due to the increased distance between the base contact metal to emitter mesa. So, to improve the high frequency performance of DHBTs with emitter width less than 0.2 μm, both base sheet resistance and base contact resistivity need to be reduced. Reducing the base sheet resistance would reduce the resistance between the base contact metal to emitter mesa. Reducing base contact resistivity would not only reduce base contact resistance but also the base transfer length, allowing a narrower base contact and leading to reduced base-collector capacitance, which will further improve the high frequency performance of the device.

CONCLUSIONS

Type-II GaAsSb DHBTs with different emitter widths are characterized and compared. We found that emitter peripheral recombination current limits the current gain for submicron DHBTs. An AlInP emitter ledge was found to reduce the emitter peripheral recombination current and improve current gain. The base resistance limits the further improvement of the high frequency performance of deep submicron devices. To further improve the DC and RF performance of these devices, emitter ledge width has to be optimized; base sheet resistance and base contact resistivity have to be reduced.

REFERENCES

[1] R. Bhat, W-P. Hong, C. Caneau, M. A. Koza, C-K. Nguyen and S. Goswami, Appl. Phys, Lett. 68, 985 (1996).

[2] T. S. Low, M. W. Dvorak, M. Farhoud, R. E. Yeats, M. Iwamoto, G. K. Essilfie, T. Engel, B. Keppeler, J. S. C. Chang, J. Hadley, G. Patterson, F. Kellert, N. Moll, S. R. Bahl, C. P. Hutchinson, E. Ehlers, M. E. Adamski, M. K. Culver, D. D'Avanzo, and T. Shirley, IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Palm Springs, CA, USA, 30 October–2 November 2005, pp. 69-72.

[3] Y. Oda, N. Watanabe, K. Kurishima, M. Uchida and T.Kobayashi, extended abstract of the 24th electronic materials symposium, pp. 93-94, July 2005.

[4] K. Y. (Donald) Cheng, C.C. Liao, H. Xu, K.Y. Cheng, and M. Feng, Appl. Phys. Lett. 98, 242103 (2011).

[5] R. Lövblom, R. Flückiger, M. Alexandrova, O. Ostinelli, and C. R. Bolognesi, IEEE Electron Device Letters, Vol. 34, No. 8, pp. 984 – 986 (2013).

[6] W. Snodgrass, B. R. Wu, K. Y. (Norman) Cheng, and Milton Feng, IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 10-12 December 2007, pp. 663–666.

[7] Y. Oda, K. Kurishima, N. Watanabe, M. Uchida, and T. Kobayashi, IEEE Indium Phosphide and Related Materials Conference (IPRM), Princeton, NJ, USA, 8-11 May 2006, pp. 92-95.

[8] B. R. Wu, M. W. Dvorak, P. Colbus, T. S. Low, and D. D'Avanzo, IEEE Indium Phosphide and Related Materials Conference (IPRM), Newport Beach, CA, USA, 10-14 May 2009, pp. 20-23.

[9] H. Xu, E. W. Iverson, C.-C. Liao, K. Y. (Norman) Cheng, and M. Feng, IEEE Electron Device Letters, vol. 34, no. 1, pp. 33–35, (2013).

[10] B-R. Wu, M. W. Dvorak, P. Colbus, T. S. Low, and D. D' Avanzo, IEEE Indium Phosphide and Related Materials Conference (IPRM), Berlin, Germany, 22-26 May 2011, pp. 1-3.

[11] H. Xu, B-R. Wu, E. W. Iverson, T. S. Low, and M. Feng, IEEE Electron Device Letters, vol. 35, no. 1, pp. 24-26, (2014).

[12] O. Nakajima, K. Nagata, H. Ito, T. Ishibashi, and T. Sugeta, Jpn. J. Appl. Phys., vol. 24, no. 8, pp. L596–L598, Aug. 1985.

[13] H. H. Lin, et al., Appl. Phys. Lett. 47, 5 (1985)

[14] Y. K. Fukai, K. Kurishima, M. Ida, S. Yamahata, and T. Enoki, Electron. Commun. Jpn., Pt. 2, vol. 90, no. 4, pp. 589–596, Mar. 2007.

[15] H. G. Liu, H. D. Chang, and B. Sun, IEEE Transactions on Electron Devices, Vol. 58, No. 2, Feb, 2011.

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ACRONYMS

DHBT: Doulbe Heterojunction Bipolar Transistor
f_T: Currrent gain cutoff frequency
f_{MAX}: Power gain cutoff frequency
SOLT: Short-Open-Load-Through