Improvement of Transconductance Flatness of GaAs MESFETs

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Keywords: Transconductance, MESFET, GaAs, push-pull amplifier

Abstract

The flatness of the transconductance (Gm) curve was improved by optimizing the gate recess etch time and exposure in chemical during the lift-off process. It was found that the wide ungated channel and long exposure in chemical reduced the flatness of the Gm curves. An optimized gate recess etch time and exposure in chemical provided flat Gm curves. This process was used for the fabrication of a push pull amplifier, which provided OIP3 and OIP2 of 45 and 80 dBm, respectively.

INTRODUCTION

The fabrication of amplifiers with good linearity requires a clear understanding of the process. Previously published results have shown that the characteristics of the ungated area play an important role in determining the linearity of the amplifiers [1]. Generally, the surface states between GaAs and the nitride passivation layer as well as the material etching in the ungated area reduce the flatness of the transconductance curve (Gm versus gate voltage). High gate leakage current of the devices can also degrade the transconductance [2]. Transconductance needs to remain constant in the operating range of the gate bias to achieve low third order intermodulation distortion (IM3) and high third order intercept point (IP3) [3]. In this investigation the fabrication process was optimized to obtain flat Gm curves and manufacture amplifiers with high linearity.

DEVICE STRUCTURE AND PROCESSING

GaAs high (+) low (-) high (+) epitaxial structure with an InGaP etch stop layer was used for the fabrication of the MESFET devices. The process flow starts with a formation of ohmic contacts, followed by boron implantation for isolation, Tgate photo, gate recess, gate metal deposition, nitride passivation, overlay metal, and final passivation. Half micron T shaped gates were formed by using a standard optical photolithography process. After gate recess etch, the InGaP etch stop layer was removed prior to deposition of the gate metal.

Three different types of experiments were carried out to study the effect of ungated channel length and exposure time in the lift-off process chemical to the flatness of the transconductance curves. In the first experiment, two different gate recess etch times were used. The exposure in chemical during liftoff process was long. In the second experiment, gate recess etch time was fixed, but the exposures in lift-off process chemical were different. In the final experiment, the wafers were etched, (gate recess), for three different intermediate times and the exposure in the lift-off process chemical was short.

RESULTS AND DISCUSSIONS

The MESFET devices were characterized by using a semiconductor parameter analyzer. The transconductance was extracted from the Ids versus Vgs curves, where Ids is the drain to source current and Vgs is the gate to source voltage. Figure 1 shows the plots of Gm versus Vgs at drain source voltage (Vds) of about 3.5 V for the wafers with two different gate recess etch times. The Gm curves of the devices are not flat. The reduction of Gm from the peak to 0.75 V of Vgs was found to be 20 ms/mm for the devices with breakdown voltage of about 17V. This is less than the reduction of 28 ms/mm for the devices with breakdown voltage of about 19 V. The longer ungated channel is likely the reason of higher reduction of Gm from the peak value, since the exposure in chemical during liftoff process was the same for both wafers. The width of the ungated channel is increased with the increase of gate recess etch time due to the presence of InGaP etch stop layer. Therefore, the edge of the n+ layer is away from the gate metal edge, which resulted in high breakdown voltage.

Figure 2 shows the plots of Gm versus Vgs of the wafers with the same gate recess etch time but different exposures in lift-off process chemical. The long exposure in chemical generated a Gm curve not as flat as the short exposure in chemical. For short exposure, Gm reduced from 168 ms/mm

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(peak) to 150 ms/mm (at Vgs = 0.75 V). However, for long exposure in chemical, Gm reduced from 168 ms/mm (peak) to 144 ms/mm (at Vgs = 0.75 V).

The above observations indicate that the recess etch time and exposures in lift-off process chemical have a significant role in determining the Gm flatness. Therefore, in the final experiment the exposure in lift-off process chemical was kept short, and the wafers were etched for three different intermediate times. The gate PCM test was removed and nitride deposition was performed within a few hours after

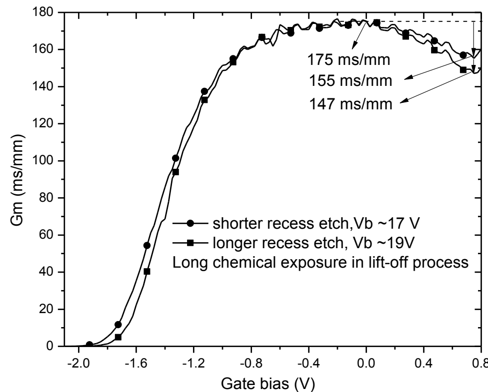

Fig. 1. Plot of Gm versus gate bias obtained at Vds of about 3.5 V for different recess etch durations

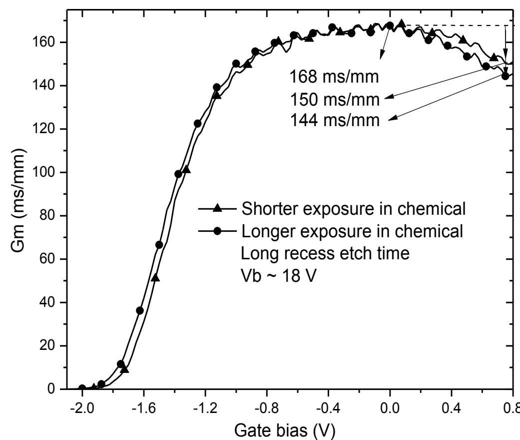

Fig. 2. Plot of Gm versus gate bias obtained at Vds of about 3.5 V for different exposures in lift-off process chemical

gate metal liftoff, in order to minimize the oxidation in the ungated channel. Figure 3 shows the Gm curves of the wafers with three intermediate recess etch times and short exposure in lift-off process chemical. All Gm curves are flat up to around 0.75 V of Vgs, which is likely due to less surface states resulting from the shorter ungated channel than the previous wafers. It is also due to reduction of material etching in the ungated channel for less exposure in the chemical. The median breakdown voltages increased from 13 V to 15 V with the increase of recess time.

Ids versus Vgs transfer characteristics of three devices- (i) short gate recess etch time and short exposure in chemical, (ii) intermediate recess etch time and long exposure in chemical, (iii) long recess etch time and long exposure in chemical are shown in Fig. 4. In order to understand the linearity of the devices, polynomial fitting of the linear portions of the curves were analyzed. The transfer characteristics can be expressed by a 5th order polynomial as shown below [4]:

$$I_{ds}= B_0 + B_1V_{gs} + B_2V_{gs}^2 + B_3V_{gs}^3 + B_4V_{gs}^4 + B_5V_{gs}^5 \quad (1)$$

where, B_0 is defined by Ids at Vgs = 0 V, and the B_n (n = 1 to 5) coefficients are different independent variables, which can be correlated to the linearity of the devices. The polynomial fitting parameters of the transfer characteristics (Fig. 4) are reported in table I. Higher B_0 of the devices with short recess etch time indicates higher Idss than the wafers with intermediate and long recess etch times. Long recess etch resulted in more ungated channel which increased the channel resistance. In order to compare the distortion, the values of B_n (n≥2) were normalized by B_1. The values of B_n (n≥2) can be considered as a linearity index. High values of B_n (n≥2) indicate poor linearity of the devices. The second harmonic distortion is related to B_2/B_1, which is much lower for short recess etch time than the devices with intermediate and long recess etch times. The rest of the B_n (n≥2) values for short recess etch time are much lower than the other devices, which indicate better linearity performance. The value of B_3/B_1 representing third order inter-modulation distortion are much lower for the devices with short recess etch time. Therefore, these devices would provide much higher output power and power added efficiency by suppressing the third order intermodulation.

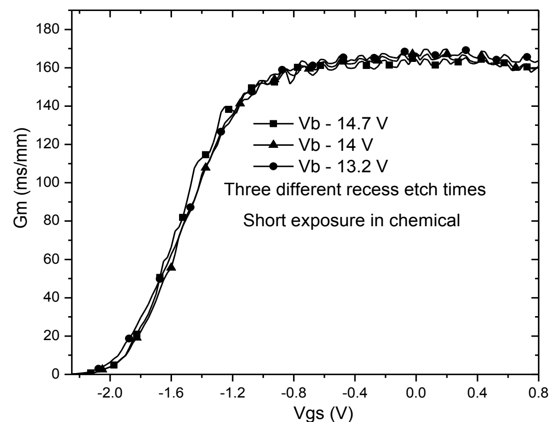

Fig.3. Plot of Gm versus gate bias obtained at Vds of about 3.5 V for three different recess etch times and short exposure in chemical

Finally, a push pull amplifier was manufactured using the optimized process. Several devices were packaged and tested to find out the characteristics of the amplifiers. The results are shown in table II. The key parameters (OIP2, OIP3) of the push pull amplifier indicate the good quality of the devices.

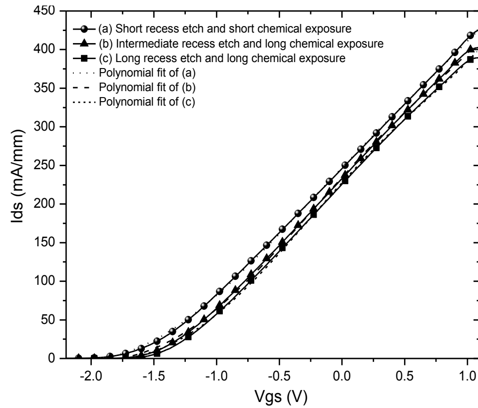

Fig.4. Ids versus Vgs plots with polynomial fitting

TABLE I

POLYNOMIAL FITTING PARAMETERS

Bn	Short recess etch, short exposure in chemical	Intermediate recess etch, long exposure in chemical	Long recess etch, long exposure in chemical
B0	247.06	234.64	227.63
B1	170.02	178.82	178.89
B2	-7.15	-15.94	-21.91
B3	-5.87	-18.28	-23.23
B4	6.96	10.59	14.05
B5	0.35	4.95	8.02
B2/B1	-0.042	-0.089	-0.1221
B3/B1	-0.0345	-0.1022	-0.1298
B4/B1	0.0409	0.0592	0.0785
B5/B1	0.0020	0.0277	0.0448

TABLE II

MEASURED PARAMETERS OF THE PUSH PULL AMPLIFIER

Parameters	Test Conditions 50 MHz to 1000MHz	Measured values
Gain (dB)	In to Out	20
Gain Flatness (dB)	In to Out	0.5
Noise Figure (dB)	>150 MHz	4.5
Input Return Loss (dB)	Input	22
Output Return Loss (dB)	Output	15
OIP2 (dBm)	500 MHz, 6MHz, +8dBm Out	80
OIP3 (dBm)	500 MHz, 6MHz, +8dBm Out	45
Idd (mA)	+8 V	325

CONCLUSIONS

The longer gate recess and exposure times in chemical during gate metal liftoff process impacted the flatness of the Gm curves of the MESFET devices. The flatness of the Gm curve was improved by reducing the recess etch time, exposure in chemical, and depositing nitride layer just after gate metal liftoff. Polynomial fits of the Ids versus Vgs curves indicated better linearity of the devices with less recess etch time and exposure in chemical. Finally, a push-pull amplifier was fabricated with the optimized process and good characteristics were observed.

ACKNOWLEDGEMENTS

The authors wish to acknowledge David Hoag for the encouragement and support of this project. James Ritchie and Taranath Yarabothu are acknowledged for the post FAB support and GaAs IC database, respectively.

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ACRONYMS

MESFET: Metal-Semiconductor Field Effect Transistor
IM3: Third order Intermodulation distortion
IP3: Third order Intercept point
OIP2: Output Second-Order Intercept Point
OIP3: Output Third-Order Intercept Point
PCM: Process Control Monitor.