High Performance GaAs RF Switch with a P-Type Capping Layer

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Abstract

Due to its low insertion loss and the high linearity, the Junction Pseudomorphic High Electron Mobility Transistor (JPHEMT) is widely used for RF switches in wireless communications. In this paper, we describe a JPHEMT with a p-type capping layer from the gate to source/drain regions for improving the off-state characteristics. The device parameters of the p-layer are optimized using device simulation technology to enhance the off-state characteristics. It has been demonstrated that gate-source breakdown voltage (BV_{gs}) is 11 V higher, off-state capacitance (C_{off}) is 25 % lower, the power handling capability is better and the 3rd harmonic distortion is 6 dB lower than those of the conventional JPHEMT. The obtained R_{on}*C_{off} product of < 160 fsec is very favorable compared with RF switches based upon conventional JPHEMT, silicon-on-insulator (SOI), and silicon-on-sapphire (SOS) technologies.

INTRODUCTION

We have been developing JPHEMT, which is widely used in RF switches for GSM, CDMA, UMTS, and LTE handsets due to its superior characteristics of insertion loss and linearity compared with other switches [1]. Increasing the number of frequency bands for high speed wireless communications requires further improvement to the inherent advantages of JPHEMT switches. Low insertion loss can be achieved by low on-resistance (R_{on}) and high isolation can be achieved by low C_{off}. Therefore, a low R_{on}*C_{off} product is critical to ensuring low-loss multi-port RF switches. The R_{on} comprises a channel resistance from source electrode to drain electrode and source/drain contact resistance, which can be decreased by increasing the sheet electron concentration (N_s) at the InGaAs channel. On the other hand, C_{off} increases due to the reduction of the depletion layer width between the junction gate and the source/drain regions. Hence, there is a trade-off between R_{on} and C_{off}. The linearity of the RF switch is determined by the linearity of both the ON and OFF arms. In particular, the improvement of the OFF arms linearity is generally considered to be difficult due to the complex behavior of the capacitances in the off-state [2,3].

In this paper, we propose a new device structure of the JPHEMT with a p-type capping layer which expands the depletion layer width for reducing C_{off} in the off-state without sacrificing R_{on} in the on-state. As a result, a low R_{on}*C_{off} product and high linearity are realized.

DEVICE STRUCTURE AND FABRICATION

Figure 1 shows the schematics of the conventional JPHEMT (structure A) and the new device structure (structure B). A double-doped AlGaAs/InGaAs channel was adopted for both structures. The structure B has the p-type capping layer located on the n-AlGaAs layer between the gate and the source/drain regions. In the off-state, this p-layer creates depleted electrons in the InGaAs channel in the same way that the junction gate operates, resulting in a large depletion layer width between the gate and the source/drain regions compared with the conventional JPHEMT. Device fabrication for structure B was initiated by recess etching the epitaxially grown p-layer of the source/drain ohmic electrode regions. Then, both structure A and B adopted the same following fabrication process. A SiN film was deposited and opened as a mask for Zn diffusion to form the junction gate region followed by a device isolation using ion implantation. The gate and the source/drain electrodes were formed using Ti/Pt/Au and AuGe/Ni/Au metals, respectively. Finally, gate resistors and gold plating interconnects were formed.

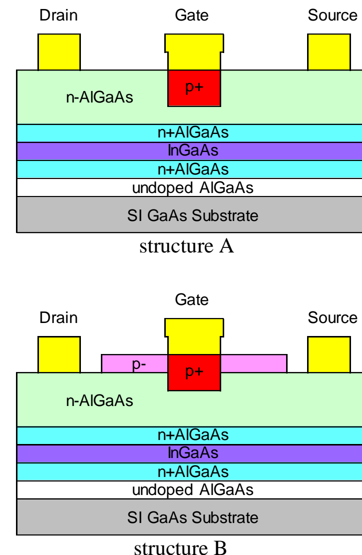

Figure 1. Schematics of conventional JPHEMT (structure A) and new device structure (structure B).

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RESULTS AND DISCUSSION

Using device simulation technology, we studied the contribution of the p-layer to the device operation. The electron concentration profiles of the structure A and B at the gate-source bias voltage (V_{gs}) of -10 V in the off-state are shown in Fig. 2 and those at the V_{gs} of 1 V in the on-state are shown in Fig. 3. In the off-state, the InGaAs channel between the gate and the source region of the structure A accumulates electrons. However for the structure B, electrons at the channel beneath the p-layer are depleted. Therefore, the depletion layer width between the gate and the source region of the structure B is larger than that of the structure A. Thus, the obtained C_{off} of the structure B becomes smaller than that of the structure A. In the on-state, as shown in Fig. 3, the electron concentration of the InGaAs channel between the gate and the source regions of both structures are similar and almost as much as a sum of the supplied impurities in the electron supply layer, since the thickness of the n-AlGaAs is sufficiently large to prevent the electron depletion at the InGaAs channel. Figure 4 shows the simulated relationship between N_s at the channel and the R_{on}, C_{off}, and $R_{on}*C_{off}$ product, normalized to the values of the structure A at N_s of 3.6x10^{12} cm^{-2}. As mentioned above, the impact of the p-layer to the R_{on} appears small. Although C_{off} increases with N_s, the structure B shows the significant decrease of C_{off} compared with the structure A. We confirmed that the structure B has an advantage of $R_{on}*C_{off}$ product due to low C_{off} while R_{on} is comparable to the structure A.

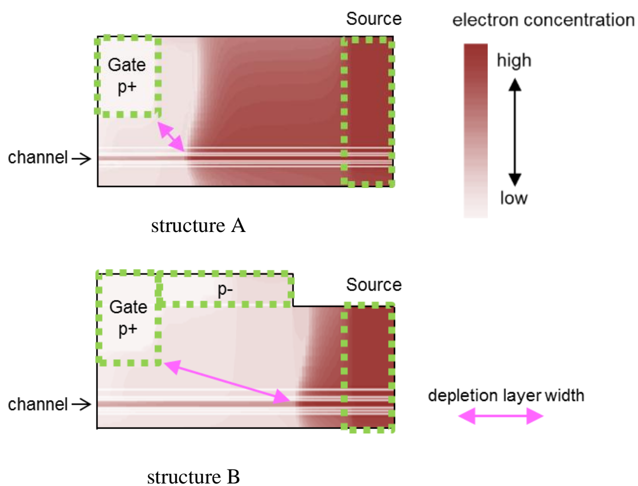

Figure 2. Electron concentration profiles at V_{gs} of -10 V. Drain and source electrodes are grounded.

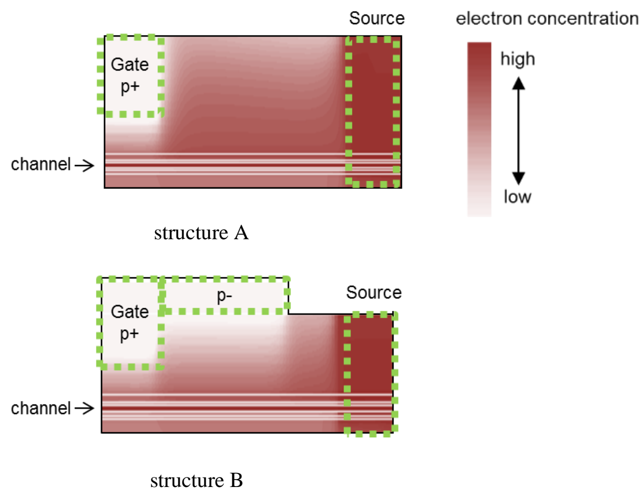

Figure 3. Electron concentration profiles at V_{gs} of 1 V. Drain and source electrodes are grounded.

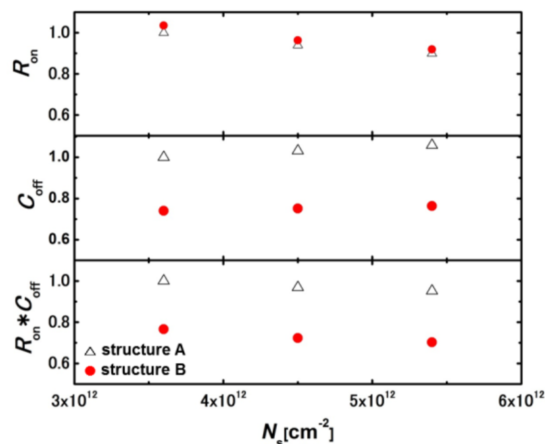

Figure 4. Simulated R_{on}, C_{off}, and $R_{on}*C_{off}$ product as a function of N_s at the InGaAs channel.

The DC characteristics and the small signal characteristics of both structures were measured at room temperature using a parameter analyzer and a network analyzer, respectively. The measured gate length and gate width of the transistors are 0.4 µm and 1 mm, respectively. The gate leakage current (I_g)-V_{gs} characteristics of both structures are shown in Fig. 5. The I_g of the structure B is significantly small and the obtained BV_{gs} at the I_g of 5 µA/mm is 26 V, which is 11 V higher than that of the structure A. In Table I, the threshold voltage (V_{th}) at the drain current of 0.5 mA/mm and the drain-source voltage of 0.1 V, BV_{gs}, and C_{off} at 2 GHz are compared between the structure A and B. The measured C_{off} of 153 fF/mm at V_{gs} of -10 V is 25 % lower than that of the structure A. Furthermore, C_{off} of 143 fF/mm at V_{gs} of -20 V was obtained, taking advantage of high BV_{gs} of the structure B. These results are in close agreement with the device simulation experiments shown in Fig.4.

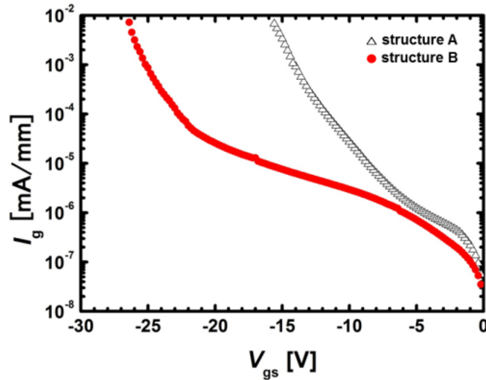

Figure 5. I_g – V_{gs} characteristics of structure A and B .

Table I.
Obtained parameters of structure A and structure B.

	structure A	structure B
V_{th} [V]	-1.2	-1.2
BV_{gs} [V]	-15	-26
C_{off} [fF/mm]	208 (V_{gs} -10 V)	153 (V_{gs} -10 V) 143 (V_{gs} -20 V)

The input power (P_{in})-output Power (P_{out}) characteristics of the off-state FET at V_{gs} of -9 V and the fundamental frequency of 900 MHz are shown in Fig. 6. Although the P_{out} of the structure A rolls off at around P_{in} of 32 dBm, the structure B maintains the P_{out} up to P_{in} of 34 dBm, indicating that the structure B shows at least 2 dB higher power handling capability than that of the structure A. The power handling capability defined by the 1 dB compression point, so-called P_{1dB}, at various V_{gs} is shown in Fig. 7. Since the P_{1dBm} at V_{gs} of -11 V for the structure B is above the measurement limit of 35 dBm, we added the trend predicted from the theory that the power handling capability is limited either by V_{th} at low V_{gs} or BV_{gs} at high V_{gs} [4]. As is seen in Fig. 7, although the power handling capability at V_{gs} of -7 V is similar for both structures, that at V_{gs} of -11V for the structure B is larger than that for structure A. This higher power handling capability of structure B is a result of the higher BV_{gs} characteristics associated with the structure. Figure 8 shows the circuit employed for the off-state distortion measurement, in which 3-stacked off-state FETs are connected to the GND and signal lines. Figure 9 shows the P_{in} dependence of the measured 3rd harmonic distortion using this circuit. An applied V_{gs} of -9V was chosen for structure A and -13 V for structure B based upon the difference in the power handling capabilities. The 3rd harmonic distortion of structure B at P_{in} of 35 dBm is 6 dB lower than that of structure A due to the improvement in off-state characteristics.

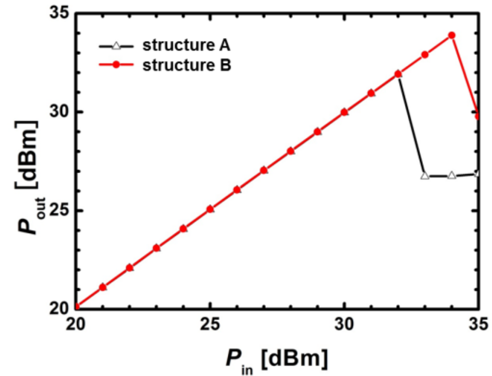

Figure 6. The relation between P_{in} and P_{out} at V_{gs} of -9 V for structure A and B.

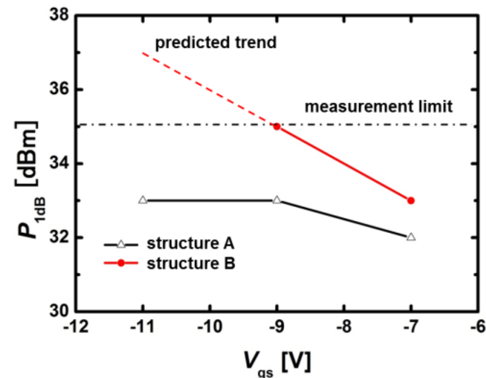

Figure 7. The relation between V_{gs} and P_{1dB} of structure A and B

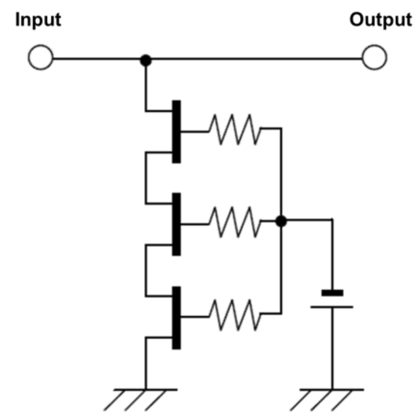

Figure 8. Schematic of distortion measurement of 3-satcked off-state FETs.

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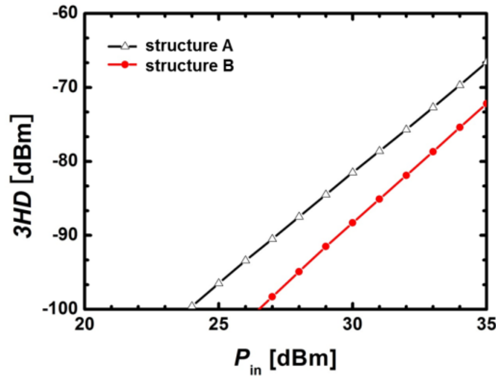

Figure 9. P_{in} dependence of 3rd harmonic distortion generated from 3-stacked off-state FETs at V_{gs} of -9V for structure A and -13 V for structure B.

In Table II, $R_{on}*C_{off}$ products are compared among GaAs JPHEMT (this work), state of the art SOI, and SOS technologies [5]. $R_{on}*C_{off}$ product obtained in this work is superior to that of other technologies.

Table II.
Comparison of $R_{on}*C_{off}$ product of GaAs JPHEMT, SOI, and SOS technologies.

	GaAs JPHEMT (This work)	SOI	SOS
$R_{on}*C_{off}$ [fsec]	< 160	200	270

CONCLUSIONS

We propose a new JPHEMT device structure with a p-type capping layer extended from the gate to source/drain regions. An optimized structure using device simulation technology shows improved C_{off} without significant R_{on} increase, resulting in low $R_{on}*C_{off}$ product. The fabricated new structure shows 25% lower C_{off} than that of the conventional JPHEMT without sacrificing R_{on}. Due to the high BV_{gs}, high power handling capability is realized. In addition, the measured 3rd harmonic distortion generated from an off-state FET is 6 dB lower than that of the conventional JPHEMT. The obtained $R_{on}*C_{off}$ product is superior to those of RF switches based on other technologies.

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