The First 0.2μm 6-Inch GaN-on-SiC MMIC Process

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Abstract

The world's first 0.2μm 6-inch GaN-on-SiC MMIC high power and high yield process is reported. Utilizing Dual Field Plate technology and 4-mil substrates, we have created a GaN HEMT process that provides excellent performance for applications at frequencies up to Ka-band. DC characteristics have excellent uniformity across the wafer with very high spec yield. The developed 6-inch HPA MMIC process technology provides a cost advantage for military system insertions.

INTRODUCTION

There is an increasing demand for high power GaN-on-SiC technology for both military and commercial microwave applications. The need to reduce the cost of GaN MMICs has become a driving force as their use for power applications becomes increasingly widespread. One method is to scale wafer size from the standard 4-inch (100mm) diameter to 6-inch (150mm) [1] to provide substantially more area for a lower unit chip cost, as shown in Table I.

Table I Anticipated cost advantage of 6-inch vs. 4-inch processes (normalized to 4-inch)

	4-Inch	6-Inch
Usable Wafer Area*	1	2.4
Process Cost	1	1.2
Epi Cost	1	1.2
Chip Out Per Lot	1	2.4
Chip Unit cost**	1	0.5

Excluding 5mm around edge circumference of wafers due to epi/processing ring, assuming processing cost = ¾ total cost and epi cost = ¼ total cost.

The conversion to 6-inch is further justified with the 6-inch GaN epi cost approaching that of 4-inch wafers due to volume demand. In addition to reducing cost, the 6-inch line has several advantages – better visual and line yield due to increased automation and reduced number of wafers required for qualification. BAE Systems has been working on a 6-inch GaAs PHEMT technology since 2003. Based on our extensive 6-inch GaAs experience, we have now developed a 0.2μm GaN MMIC process on 6-inch SiC substrates, as shown in Figure 1.

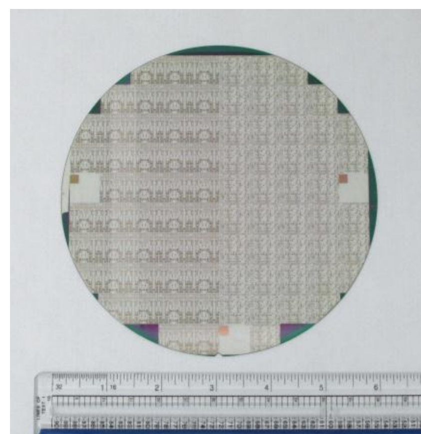

Fig. 1 A fabricated 6-Inch GaN HEMT MMIC wafer.

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6-INCH MATERIAL TECHNOLOGY

The 0.2μm 6-inch dual field-plate (DFP) GaN-on-SiC MMIC fabrication heavily utilizes automated cassette-to-cassette equipment in the foundry, reducing manual wafer handling for higher yield. BAE Systems GaN epi is based on an AlGaN/GaN structure with a thin GaN cap layer and Fe-doped GaN buffer. The material structure is designed to provide a high sheet charge density for high full channel current and output power, while maintaining good reliability.

The MOCVD 6-inch GaN epi has low density of defects – most are substrate-related micropipes and polytypes (Figure 2). The sheet resistance uniformity of the 6-inch wafers is ~1.2% -- slightly better than the 4-inch counterpart. Al% uniformity of better than 1% from the 6-inch AlGaN/GaN HEMT structure has also been achieved. The 6-inch GaN-on-SiC starting wafer is 500μm thick – similar to the 4-inch one. Epitaxial wafer warping was initially a

challenge for the 6-inch wafers due to the reduced thickness-to-diameter ratio compared to 4-inch. A set of DOEs was carried out and, as demonstrated in Figure 3, IQE/RF has successfully reduced the epitaxial wafers' bow and warp from >100µm to ~40µm over the 6-inch wafers, suitable for wafer processing.

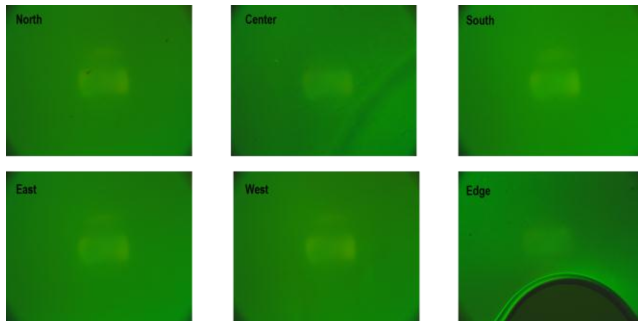

Fig. 2 Defect density from epi growth is very low, including inside the edge exclusion zone. Most defects are substrate related micropipes, polytypes, etc.

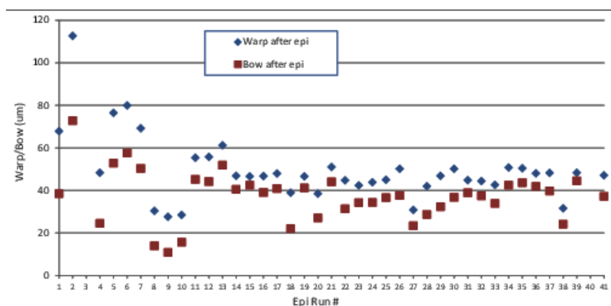

Fig. 3 Improved warp/bow to ~40µm from 6-inch GaN epi wafers.

6-INCH WAFER PROCESSING CHALLENGES

The 6-inch GaN-on-SiC wafer has a notch that is 45° off from that of industry-standard 6-inch GaAs PHEMT wafers. Some of our 6-inch GaAs tools failed to recognize the GaN notch due to wafer transparency and the different notch position. We also observed a substrate "leakage" (i.e., leaking photoresist through micropipes in the SiC substrates during lithography process) on some early wafers.

After working with the epi/substrate vendors and adjusting our tools to resolve these issues, the remaining effort was quite straightforward – largely put into optimizing the existing 4-inch GaN mesa, ohmic, nitride deposition and via-hole formation processes using 6-inch tools to achieve good uniformity and yield over 6-inch wafers.

DEVICE CHARACTERISTICS

Figure 4 is a SEM photograph of the fabricated 0.2µm DFP GaN devices. The 0.2µm gates and field plates are formed through electron beam lithography. Two-terminal gate-to-drain breakdown of >90V was measured, similar to the 4-inch case. Shown in Table II, the GaN HEMT exhibits average normalized maximum current of 1,124 mA/mm and extrinsic transconductance of 372 mS/mm at a drain bias of 10V and pinchoff voltage of -3.1V.

Table II also shows the tight distribution and near 100% spec yield of device DC characteristics. These DC characteristics are all within ±5% of typical 4-inch GaN ones. The tight distribution and high process yield are attributed to the excellent material quality and improved manufacturability obtained by utilizing the 6-inch foundry line.

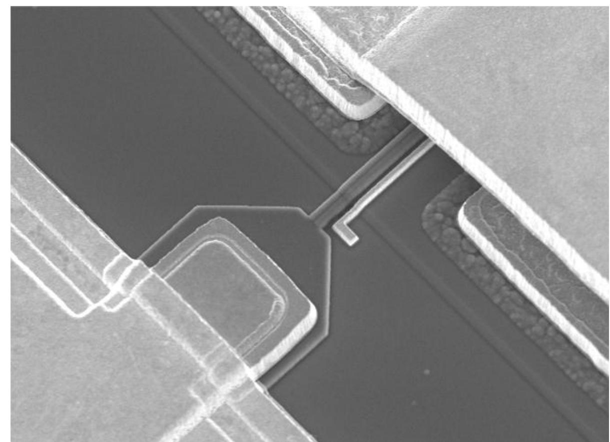

Fig. 4 0.2µm dual field plate GaN HEMT device.

Table II 0.2µm GaN HEMT device uniformity and yield.

Parameter	4-Inch Value	6-Inch Value	6-Inch Spec Yield
I_{max} (mA/mm)	1075 (±10%)	1124 (±5%)	100%
g_m (mS/mm)	355 (±10%)	372 (±5%)	100%
V_{po} (V)	-3.3 (±5%)	-3.1 (±5%)	100%
V_{bd} (V)	>90	>90	80%

I_{max}: full channel current, g_m: peak transconductance, V_{po}: pinchoff voltage, V_{bd}: breakdown voltage at I_d 1mA/mm. Spec yield: 30 sites from 6-inch wafer.

As can be seen from Figure 5, the typical pulsed I-V characteristics (pulsed at V_g = -5V, V_d = 30V) of GaN HEMTs from the 6-inch wafer are good and comparable to those from a 4” GaN wafer. Figure 6 shows the mapping of 0.2µm GaN HEMT pulsed I-V characteristics on an entire 6-inch GaN-on-SiC wafer. Excellent pulsed current uniformity and device yield have been achieved.

The 6-inch GaN-on-SiC backside process is being developed. Although some of the tools needed for 6-inch backside process (such as 6-inch SiC grinding machine) take time to establish, no 6-inch backside process related issues have been noted.

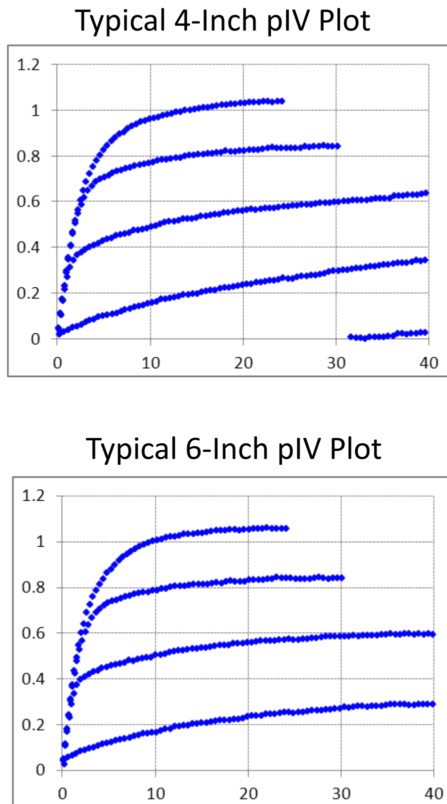

Fig. 5 Comparison of 0.2µm GaN HEMT device pulsed I-V characteristics. Devices were pulsed at V_{gs}=-5V, V_{ds}=30V. (Vertical scale: I_{max}, A/mm, horizontal scale: V_{ds}, V. Top curve: V_{gs}=+1V, -1V per gate step towards pinchoff.)

Conclusions

We have demonstrated the world’s first 0.2µm 6-inch GaN-on-SiC HEMT process on 4-mil substrates with excellent yield and uniformity. Utilizing the established dual field plate GaN technology, we have observed no compromise in 6-inch material quality, processing yield and device performance, when comparing to 4-inch. The 6-inch GaN HEMT process technology reported herein provides a ~2:1 chip cost advantage over 4-inch for military system insertions.

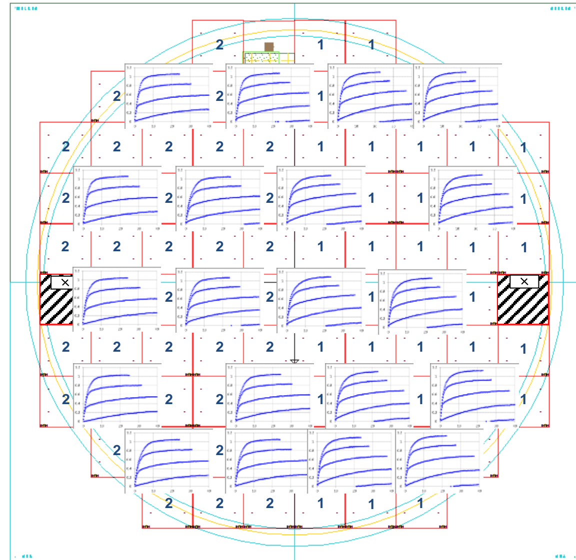

Fig. 6 Mapping of 0.2µm GaN HEMT pulsed I-V characteristics (pulsed at V_g = -5V, V_d = 30V) on a 6-inch wafer. Excellent pulsed current uniformity and device yield have been achieved.

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