Translating Epi Structures into Growth Recipes: Manufacturability Concerns

Guoliang Zhou and Mark Borek

Skyworks Solutions, Inc., 20 Sylvan Road, Woburn, MA 01801, guoliang.zhou@skyworksinc.com

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Abstract

This paper discusses the general requirements and guidelines for translating an epi structure into an MBE growth recipe. Particularly, we use a pHEMT device as an example to demonstrate how sensitive yield and device performance can be to the MBE growth process, and concentrate our discussion on manufacturability aspects of MBE recipe defining and generating procedures. We share the lessons we have learned at Skyworks and discuss the strategies that can achieve consistent manufacturing yield and best product performance.

INTRODUCTION

Design and optimization of a compound semiconductor device usually starts with design and optimization of an epi structure. An epi structure that is defined by a material spec is typically an ideal structure. Any imperfections introduced by a growth process such as spreading of doping profiles and intermixing of heterostructure interface are usually not defined in a material spec. The process of generating a growth recipe is a process of interpreting a material spec. Those growth processes related imperfections undefined by a material spec must be taken into account during recipe creating process, and the translation is not always unique. The complexity of an MBE growth recipe will not only depend on the required device structure, but also on reactor hardware (such as cell configurations), and other important considerations such as manufacturability of the products. The way how the recipe is setup can have huge impact on the robustness of the overall production process. In this paper, we will use pHEMT structure as an example, to discuss the strategy and concerns (especially manufacturability aspects) associated with MBE recipe generating process.

RESULTS AND DISCUSSIONS

When designing and optimizing an epi structure, the focus has always been on how to achieve the best possible material quality. The best material quality means minimum crystal defect density, abrupt and smooth interfaces, and minimum unwanted impurities. A common heterostructural device such as pHEMT consists of at least two different types of materials. The growth condition that is optimized for one material type may not necessarily be the optimum condition for another one. When translating an epi structure into a growth recipe, we will have choices to either tailor the growth condition for each individual layer within a growth recipe or choose a unified but compromised growth condition for all layers. In either scenario there are tradeoffs and limitations. In some cases, the growth condition can be optimized for each individual layer, but it requires transitions to switch growth condition from one layer to another. Such transition usually requires a growth stop. In other cases when individual layer thickness is too thin, or there are other limitations such as source configuration, strict doping or contamination requirements, etc., inserting a growth stop may not be an option.

One of the important aspects, which is often overlooked during initial epi structure design process, is manufacturability. An epi structure that has been optimized for achieving the best performance of a device during development phase may not always yield well consistently after being transferred into production phase. This is usually due to the manufacturability aspect not being taken into account during the initial device design and optimization phase. Here, we use a typical pHEMT device (shown in Fig. 1) as an example, to illustrate how different ways of translating an epi structure into a growth recipe can make huge difference to overall production yield and device performance.

Fig.1 shows a typical pHEMT device used for switch applications. The structure consists of active device layers, such as n-GaAs, InGaAs channel, AlGaAs Schottky, and barrier layers. The optimal growth conditions for different materials are usually quite different. In this case, for example, the growth of a strained InGaAs channel layer requires

relatively lower growth temperature, while the AlGaAs Schottky layer is preferred to be grown at a higher temperature in order to achieve the best material quality. Si delta-doping, on the other hand, requires lower growth temperature for retaining a sharp profile. When generating a production recipe, material quality is not the only important factor that need be considered. Other factors such as production throughput (the total cycle time of a growth process), yield consistency (sensitivity to variations of process condition), reactor configuration, etc. can also have high impact to overall product quality and cost. The common approach to grow the pHEMT epi shown in Fig. 1 is by growing both the lower AlGaAs spacer and InGaAs channel at a relatively lower temperature to retain the smoothness of InGaAs channel layer and minimize dislocation generation and Si delta-doping spreading into the channel. The growth process is then paused for a short period of time (so called growth-stop) after InGaAs growth to allow temperature ramping up to an optimal value for AlGaAs, and then continue for the remaining layers at a higher temperature. This process, although can be optimized for the best material quality, sometimes shows high sensitivity to a small variation of process condition for certain products, which can result in a very inconsistent device and yield performance.

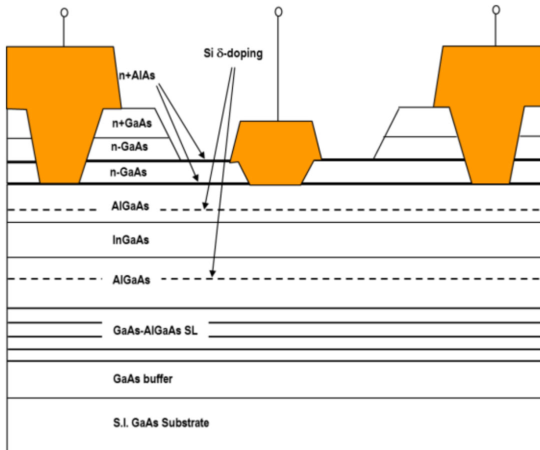

Fig.1. A typical AlGaAs/InGaAs double hetero-structure pHEMT device.

Fig. 2 shows SIMS depth profiles of Si from four pHEMT epi wafers grown at normal growth condition with a slight variation of growth temperature (in the range of 45ºC). It is very clear that the top delta-doping spread is very sensitive to as little as 10ºC of growth temperature variation. As it is well known, the spreading of delta-doping into the gate region can cause gate leakage failure for final finished devices. Such high sensitivity is very prone to process variations, which will result in inconsistent manufacturing yield and device performance. As shown in Fig.2, the bottom delta-doping peak, on the other hand, remains a sharp profile regardless of temperature change. The spreading of Si delta-doping profile is mainly driven by two possible mechanisms: surface segregation and bulk diffusion. The activation energy of a typical bulk diffusion process is usually much higher than that of surface segregation. At the typical growth temperature range of 450-650ºC for our pHEMT structure, the bulk diffusion process is still very limited, as evidenced by the fact that the bottom delta-doping profiles remain unchanged regardless of the ramping of growth temperature for AlGaAs Schottky. Therefore, we safely ignore the contribution of bulk diffusion to doping spreading. Surface segregation mechanism, however, due to its much lower activation energy, is the only mechanism that can significantly broaden Si doping profile under certain growth conditions within our normal temperature range. The surface segregation process remains inactive at the lower range of our growth temperatures, as evidenced by the fact that all bottom delta-doping and the top delta-doping grown at lower growth temperature remain a sharp profile. However, when growth temperature is set at the high end of the temperature range, the broadening of top delta-doping profile becomes evident and appears to be very sensitive to the small variation of growth temperature, as shown in Fig.2. 10˚C of temperature variation can cause significant broadening of doping profile. The results reveal that when the growth temperature is close to the high end of the range, the process must be also very close to the cusp of triggering surface segregation process, which is exactly what should be avoided from the manufacturability perspective for delivering consistent product and yield performance.

In the above example, in order to improve leakage performance, we have to make sure that the growth temperature is low enough to stay away from the region where the Si surface segregation process will become active. On the other hand, however, AlGaAs Schottky layers require higher growth temperature to ensure good crystal quality and

minimum defects. Therefore, in order to include both sides of restrictions, the optimum process window for this type of process will become very narrow, which is not in favor for making consistent products. Any normal process variations that can cause temperature change, such as measurement calibration, thermocouple reading fluctuation, and surface emissivity change of platens (that can be affected by coating conditions), can have significant impact on product yield and performance.

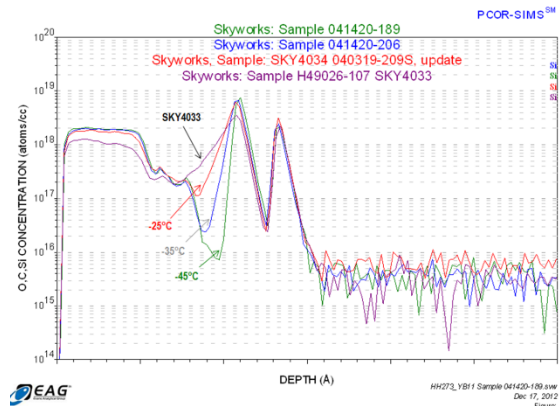

Fig.2. SIMS delta-doping profiles of Si from four pHEMT epi wafers grown at slight different temperatures within the normal range of process.

Fig.3 shows the leakage current data from device probe test for the same group of wafers grown at four different temperatures as shown in Fig.2. The starting temperature is T_0, and then we reduced growth temperature by 25C˚, 35C˚, and 45C˚, respectively. The results show that the leakage current of finished devices is very sensitive to the growth temperature in the range of initial temperature T_0 and 35C˚ below T_0. When we further lower the growth temperature by 45C˚, the leakage current remained the same as those grown at -35C˚ and become insensitive to the growth temperature when it is further reduced. For certain leakage sensitive applications, in order to improve the consistency of leakage performance, we have to push the growth temperature low enough to avoid triggering surface segregation process of Si dopant. However, there is a trade-off to how much we can lower the growth temperature. As we mentioned previously, AlGaAs Schottky layer requires a relatively high growth temperature to ensure good crystal quality and minimum defect density. Devices built on the epi that is grown at low growth temperature can fail for RF failures such as harmonic peaking, low switching speed, and/or droop failures.

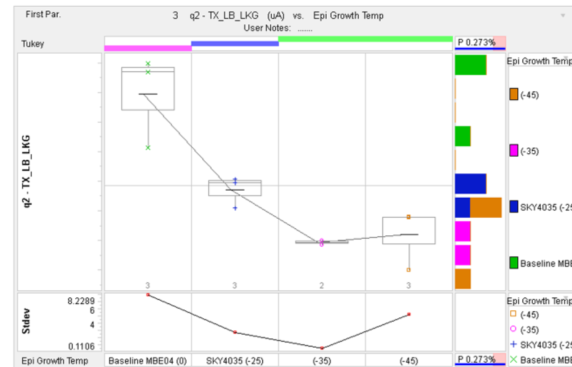

Fig.3. Probe test leakage data from four MBE lots grown at different growth temperatures. The corresponding Si delta-doping profiles are shown in Fig.2.

Although the growth conditions can be optimized to achieve both low leakage and good RF performances, the problem associated with this growth process is that for certain product applications, the optimum process window is too narrow to tolerate any process variation, i.e., the manufacturability is poor. In order to improve process robustness, it is necessary to reduce the sensitivity of leakage current to the growth temperature, but at the same time still maintain good crystal quality of all critical epi layers, especially the AlGaAs Schottky layer. One way that we can achieve this goal is by slightly modifying our growth recipe by delaying temperature up-ramping until completion of the top delta-doping layer. A growth stop has to be placed within AlGaAs Schottky layer approximate to Si pulse doping. Under this growth condition, the majority of AlGaAs Schottky will still be grown at high temperature to ensure good crystal quality and minimum defects, but Si pulse doping is grown at relative low temperature and covered by a thin layer of AlGaAs before the temperature ramping. Therefore, the surface segregation process can be avoided because the growth temperature is low enough relative to its thermal activation energy. The broadening mechanism of the Si doping profile will be only driven by bulk diffusion process, which is very limited under typical MBE growth temperature range. As a result, the sensitivity of device performance to process variations can be

significantly reduced. Fig.4 shows drain (Idss) and leakage (LKG) current comparisons of final finished devices processed from the wafers grown before and after MBE growth recipe modification. The SKY5042 was grown with a previous recipe, i.e., the growth temperature was ramped up immediately after InGaAs channel growth, while the SKY4116 was grown with the modified recipe with the top and bottom Si delta-doping layers grown at the same low temperature as the InGaAs channel, and growth temperature was not ramped up until the top Si delta-doping layer was covered by a thin AlGaAs layer. Because the growth temperature for Si delta-doping layer was much lower than the triggering point of the surface segregation process, the doping profiles remained sharp and relatively insensitive to the growth temperature variation. The AlGaAs Schottky layer was still grown at high temperature to ensure good crystal quality. To verify the insensitivity of the new process to growth temperature, we grew the SKY4116+20 and the SKY4116+40 20˚C and 40˚C higher than that of the SKY5042, respectively. Even though the drain current of finished devices is 10% higher than that of the wafers grown with the previous recipe, the leakage current is 30% lower, and remains consistent regardless of 20˚C of temperature variation.

BoxPlot

Box Plot - 'TX_LB_Idss',page 1 of 1

Q-lot	Units	Count	Mean	Std Dev	Median Q2	Min	Max	Q1	Q3	Bar Count	Par Value	Sigmas
SKY4116+20	mA	17742		14.14								
SKY4116+40	mA	17751		14.12								
SKY5042	mA	17760		6.943								

BoxPlot

Box Plot - 'TX_LB_LKG',page 1 of 1

Q-lot	Units	Count	Mean	Std Dev	Median Q2	Min	Max	Q1	Q3	Bar Count	Par Value	Sigmas
SKY4116+20	uA	17713		7.517								
SKY4116+40	uA	17704		8.697								
SKY5042	uA	17672		9.692								

Fig.4. Drain (Idss) and leakage (LKG) currents from the devices fabricated on three groups of epi wafers. The SKY5042 was grown with a previous MBE recipe. The SKY4116+20 and the SKY4116+40 were both grown with a modified recipe at 20 and 40˚C higher growth temperatures, respectively. All three groups were processed in the same lot.

This example illustrated how a small difference from MBE growth recipes can have big impact on the consistency of device performance. We also learned from the example that in order to achieve high process yield, device manufacturability concern must be included in the very early stage of the epi design phase. The initial epi DOE (design of experiment) that runs to define the epi process should not only include common structural variables, such as layer thickness, composition, and doping concentration, but also growth parameters, such as temperature (both set point and ramping profile), flux (growth rate, group III to group V ratio, etc.), growth stop, and in some cases, even cell configurations. A flowchart of basic steps that examines both structural and growth parameters to define the epi growth process is shown in Fig.5. As one can imagine, by including those growth parameters, the complexity of initial epi defining process will be greatly increased. The overall benefit, on the other hand, to production yield, cost, and quality control can be very substantial.

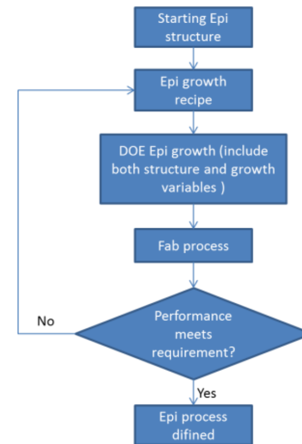

Fig.5. Flowchart includes the steps that examine both structural and growth related parameters to define the epi growth process.

CONCLUSION

The translation of a growth recipe from an epi structure is often not unique. From a manufacturing perspective, the best growth recipe may not necessarily be the one that can produce the best epi material, but the one that can consistently produce good materials with good tolerance to manufacturing variations. We used a pHEMT device as an example to demonstrate how sensitive the yield and device performance can be to the MBE growth process, and provided a solution to improve process consistency and manufacturability. The results also taught us that manufacturability must be taken into account in the process of generating MBE growth recipes to achieve the best yield, cost, and overall quality.