GaN-on-Silicon Growth by MOCVD: A Mechanistic Approach to Wafer Scaling

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Keywords: GaN, silicon, MOCVD, strain, plastic deformation, HEMT

Abstract

GaN-on-Silicon growth by MOCVD is discussed in the context of stress and strain management. Specifically, a physical and semi-quantitative mechanistic model is presented to better explain the fundamentals of GaN epitaxy on Si (111) substrates. Using the understanding gleaned from this approach, high quality GaN films have been demonstrated on Si substrates with diameters ranging from 100-200 mm.

INTRODUCTION

It is well-understood that GaN-on-Si (GOS) power electronics offer great promise to extend power levels and switching frequencies beyond the capabilities of silicon. However, due to the large lattice constant and thermal expansion coefficient (TEC) mismatch between III-nitrides and silicon, GOS growth techniques are quite different from those typically employed for GaN epitaxy on 'traditional' substrates like sapphire and SiC. If not appropriately managed, stresses from these material differences can lead to epilayer cracks, wafer warp/bow, and/or wafer breakage, particularly for thick films required by LEDs and high voltage HEMTs. Still, GOS optoelectronics and electronics technologies have matured such that high volume production integration has become an area of active focus. For widespread adoption of this technology, availability of low cost, high yield GOS epitaxial wafers at substrate sizes of 100 mm, 150 mm, and even 200 mm is desired. Although stress management and wafer scaling are two topics of significant commercial importance, there have been few -- if any -- reports linking them. This work aims to connect these topics and to provide insight linking GOS growth challenges with fundamental substrate limits. The understanding gleaned from this study has been used to demonstrate multiple production campaigns of 100 mm, 150 mm, and 200 mm GOS HEMT wafers, representing a major step toward the long-desired availability of a foundry-based supply chain for large diameter, low cost GaN manufacturing.

EXPERIMENTAL

All growths for this studywere performed in a state-of-the-art Veeco Turbodisc K465i MOCVD. This system is capable of producing (14) 100 mm wafers in a single growth run. The reactor is fully automated from load through unload, with robotic wafer staging and handling. The reactor design enables uniformity of key parameters such as alkyl and hydride flow pattern, substrate temperature, and boundary layer thickness. At the materials level, this translates to excellent thickness, compositional, and doping uniformity for reactions in both the kinetic and mass flow-limited regimes. Also, high gas velocities and laminar flow over the entire growth zone lead to low residence time and excellent interfacial abruptness. In-situ metrology consisting of emissivity-corrected pyrometry, thin film reflectance, and deflectometry was used to monitor temperature, growth rate, and wafer curvature, respectively. All growths were performed on Si (111) on-axis substrates with thicknesses adhering to SEMI standards for the given substrate diameter.

DISCUSSION

GOS is a complex process where both tensile and compressive stresses are (often intentionally) introduced through growth of different (Al,Ga,In)N alloys. This can be accompanied by strain relaxation and dislocation elimination or generation. The Timoshenko model [1] has been widely used to study residual stress in macroscopic thick films and has been further developed to accommodate strained bilayer films systems at the nanoscale [2]. Taking TEC effects into account, Hsueh developed a model for multilayers with residual stresses and external bending [3]. However, all these models only apply for elastic cases. Silicon is brittle at room temperature and experiences brittle-to-ductile transition when temperature is increased to >60% of its absolute melting point (1412ºC) [4]. Since MOCVD GOS growth is typically performed at ~1000℃, the silicon substrate is ductile and able to deform plastically in the reactor chamber during epitaxy. Thus to understand the GOS growth process, it is necessary to study deformation in both elastic and work hardening regions.

Based on analysis of wafer curvature in heterostructures [5], Fig. 1 represents a generalized model to calculate strain at the nitride/Si interface. From this model it can be shown that the strain at any location in the Si substrate is given by $\varepsilon = \frac{t_s}{2R-t_s} \sim \frac{t_s}{2R} = \frac{t_s k}{2}$ with wafer curvature defined as $k = 1/R$. When a 100 mm GOS growth process is transferred to a 150 mm or 200 mm platform, the first issue to be addressed is stress/strain control and the resultant wafer curvature.

13

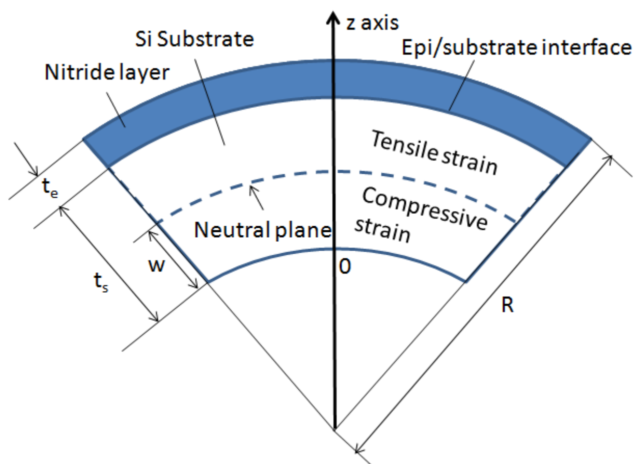

Figure 1. Strain model for nitride-on-silicon heteroepitaxy.

Fig. 2 shows curvature evolution for two identical MOCVD growths, one of them with the reactor loaded with 100 mm substrates and the other with 150 mm substrates. The total nitride epi thickness was ~5µm in both cases. In this figure, positive values of curvature refer to convex shape (as in Fig. 1) and negative values indicate a concave (i.e., bowl) shape. Despite all layers and reactor conditions held constant, post-growth wafer bow was ~0µm for the 100 mm substrates and approx. -200 µm (concave) for the 150 mm substrates. This huge difference is attributable to several factors. The thickness of SEMI-standard substrates increases with increasing wafer diameter, a fact that benefits 150 mm and 200 mm growths due to additional mechanical substrate strength. However, a much more significant impact stems from the leverage effect of increasing vertical displacement at a constant value of wafer curvature for increasing substrate sizes. From a simple geometric calculation, at a given level of concave curvature, vertical displacement at the wafer edge increases by 125% for 150 mm and 300% for 200 mm wafers relative to 100 mm. Thus, GOS growth on 150 mm and 200 mm substrates requires much larger compressive strain in the epitaxial films to achieve wafer bow at or near the same level as for 100 mm wafers. This problem is made increasingly difficult by the desire in many applications (e.g., high voltage HEMTs) to grow very thick nitride layers on silicon, since growth of most GaN and AlGaN layers leads to accumulation of tensile strain.

Another fundamental limit is the wafer "curvature ceiling" for GOS processes, which has been rarely discussed [6]. The yield stress in silicon has been reported to be between 10-20 MPa at ~1000℃ [7]. As the stress gets larger, deformation is plastic and Hollomon's equation can be used to express the plastic stress $\sigma = K\varepsilon^n$, where K is the material strength index and n is the strain hardening exponent.

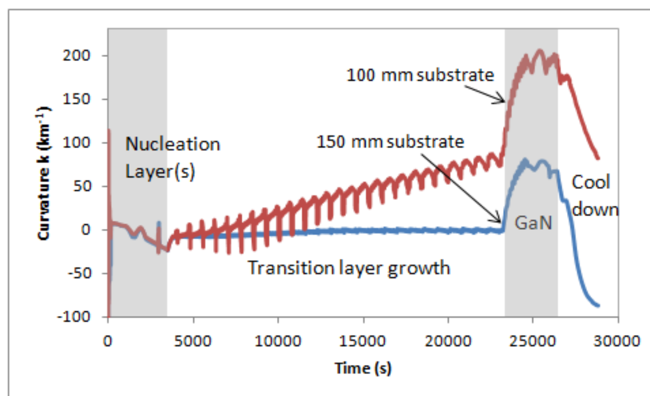

Figure 2. Comparison of wafer curvature evolution in 100 mm and 150 mm GOS wafers grown with identical recipes.

At high temperature n changes with the shear modulus, the dislocation density, Burger's vector, and other factors. When scaling substrate sizes, the upper limit for wafer curvature depends on the ultimate strength of silicon, beyond which cracks and fractures will occur. Inserting the strain model of Fig. 1 into Hollomon's equation, it is easy to see the upper limit for curvature is roughly proportional to the inverse of substrate thickness, which is consistent with upper limits we have experimentally observed during MOCVD GOS growth. Since the parameters n and K are unknown for our substrates, the maximum curvature k was estimated using the elastic strain relationship $\sigma = \frac{E\varepsilon}{1-\upsilon}$, where E is the Young's modulus and υ is Poisson's ratio. The calculated results are shown together with our experimental data in the insert table of Fig. 3.

In addition, Fig. 3 shows curvature during GaN growth and post-growth cool-down for two separate 150 mm growths. The red curve exhibits a decrease in wafer curvature during cool-down due to thermal stress from the grown films. However when the wafer curvature exceeded 142 km^{-1} during growth (blue curve), the substrate had deformed plastically and its curvature remained nearly constant until the wafer reached room temperature, at which point it exhibited a convex wafer bow of ~200 µm. Such a large wafer bow would preclude subsequent device fabrication due to loss of vacuum in automated wafer handling systems and/or excessive lithography depth-of-focus variation. Moreover, when plastic deformation occurs, dislocations are generated in the substrate. Slip lines and small cracks may also arise, potentially impacting device yield.

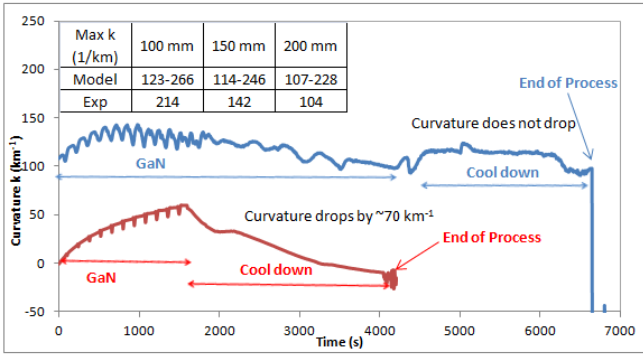

Figure 3. Demonstration of the existence of a "curvature ceiling" in GOS MOCVD growth caused by plastic deformation of the Si substrate.

With the above in-depth understanding of MOCVD GOS growth, IQE has developed growth schemes that effectively manage these issues and enable fine control of wafer bow for SEMI standard Si (111) substrate thicknesses of 625 µm, 675 µm, and 725 µm for 100 mm, 150 mm, and 200 mm diameters, respectively. Wafer bow of 0 ± 30 µm has been consistently obtained for epilayers of 5 µm total thickness on both 100 mm and 150 mm substrates. Likewise, this process has been successfully scaled to produce 2 µm thick epilayers on 200 mm substrates with the same wafer bow specification. Fig. 4 shows a 200 mm wafer bow map with post-growth bow of only 2.5 µm. This level of wafer flatness has enabled successful GOS device fabrication in multiple III-V and, importantly, silicon CMOS wafer fabs [8].

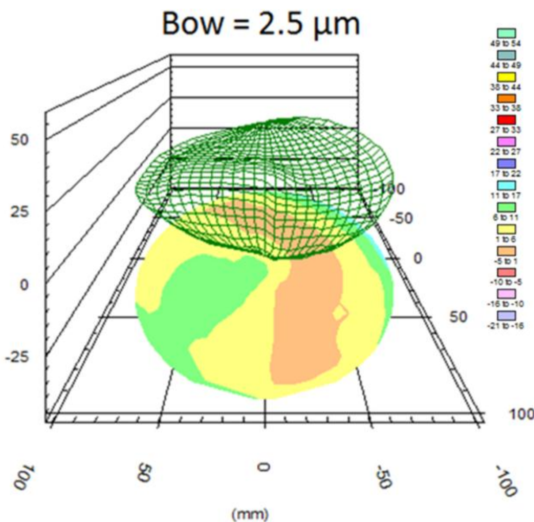

Figure 4. Post-growth flatness map of a 200 mm GOS HEMT wafer illustrating wafer bow of only 2.5µm. The total epi thickness for this wafer was ~2µm.

CONCLUSIONS

GaN HEMT growth on Si (111) has been demonstrated by MOCVD. Growth conditions were optimized within the constraints of substrate plastic deformation limits such that crack-free wafers with low final warp and bow were achieved. The availability of commercially-viable 200 mm GOS from a high volume epitaxial wafer foundry represents a major step toward integration of this technology into commercial applications such as RF infrastructure, LED-based general illumination, and high voltage power electronics. The ability of the GOS system to access the capacity, scale, and cost structure of CMOS factories is expected to open an entirely new chapter for III-V semiconductors.

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ACRONYMS

GOS: GaN-on-Silicon
MOCVD: metalorganic chemical vapor deposition
TEC: thermal expansion coefficient
LED: light-emitting diode
HEMT: high electron mobility transistor
SEMI: Semiconductor Equipment and Materials International
CMOS: complementary metal-oxide-semiconductor