Method for Forming Through Wafer Vias in GaN on SiC Devices and Circuits

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Abstract

Creating a manufacturable backside via process is a key challenge for achieving high-yield GaN HEMT devices. Backside via etch defect elimination and etch byproduct clean are critical process steps. We discuss optimizing the backside via process to eliminate pillar formation during SiC and GaN dry etching for GaN HEMT fabrication. Details of subsequent post etch cleaning to reduce byproducts is also discussed.

INTRODUCTION

GaN HEMTs on SiC have gained remarkable attention due to their potential to revolutionize power and RF electronics. Although much progress in HEMTs has been made, through vias in SiC and GaN remain critical routes to improve RF electrical performance. For ICP etch, a nickel mask is often used. This can achieve excellent selectivity rates for SiC etch at 30-40:1 [1], and the SiC acts as a self-aligned mask for the subsequent GaN etch. However, the byproducts leave traces of pillars that consist of a chemical combination of nickel and impurities from the etching process. Although considerable research has been devoted to the design of process sequence for optimizing structural properties of vias, less attention has been paid to the importance of forming clean vias. In this paper, a systematic reduction in the inherent defects is compared by alternating processes between etching techniques and cleaning procedures.

EXPERIMENTAL

The GaN/SiC wafers were temporarily bonded face down to a SiC carrier by using a liquid wax which has a cure temperature between 150 and 190°C. After SiC grinding to 100µm thickness, the samples were patterned to form 85µm diameter vias with electro-plated Ni mask. Following SiC etching, the wafers were wet cleaned to strip the mask and clean the etching byproduct. The GaN layer was then etched, using the SiC substrate as the mask, stopping on the front-side metal. The byproduct, from GaN etching, can be removed using a wet chemical etch procedure with ultrasonic agitation. The overview of the process flow is shown in Figure 1. All etching was carried out in an SPTS APS module. The etching processes used $SF_6/O_2/He$ and $Cl_2/Ar/He$ chemistries for the SiC and GaN, respectively.

RESULTS

An electro-plated Ni hard mask with typical thickness of 10 µm was patterned for the SiC

via etching and a unique descum step prior to SiC etching has been deployed to remove the hard mask seed layer and to reduce the defect level to <1%. As reported elsewhere in the literature [2], defects can cause potential problems with pillar formation that attributes to micro-masking. To reassure high yield prior to SiC etching, visual inspection is carried out and the result is shown in Figure 2.

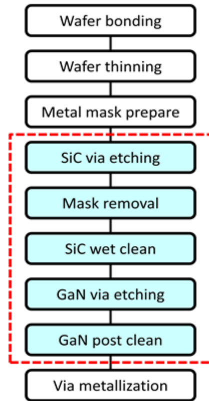

Fig.1 Overview of process flow for backside via formation

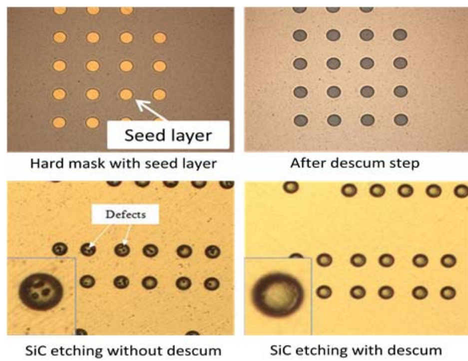

Fig.2 Optical images showing seed layer removal using the novel descum step prior to SiC etching

The hard mask, a plated Ni film, also predominately affects the etch result. Two types of Ni plating solutions were studied in this paper. The type A solution yields a current process of record (POR) low stress hard mask with typical 10μm thickness of Ni. The previous standard Ni mask which was plated by type solution B has only 50% of current thickness. Figure 3 shows improved SiC opening and sidewall profile with the lower stress mask than with the standard Ni film mask. The hypothesis for the corresponding reduction in the slope of the sidewall is lower lateral etch rates in the thicker Ni film.

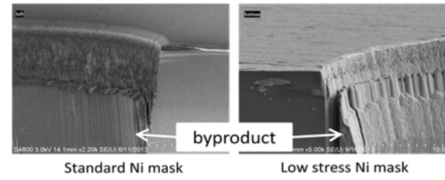

Fig.3 Comparison of the SiC etch profile using different Ni masks

After Ni hard mask removal by wet etching, the sidewall of the via hole sometimes can have a serious byproduct formation due to high ion bombardment and thermal-induced chemical reactions in the ICP process. The inductively-coupled plasma process parameters enable a 1.2 μm/minute etch rate of SiC for increased throughput at the expense of more byproduct formation. The left hand side of the images in Figure 4 show small and large areas of possible post Ni hard mask strip debris in the center and edge of the vias.

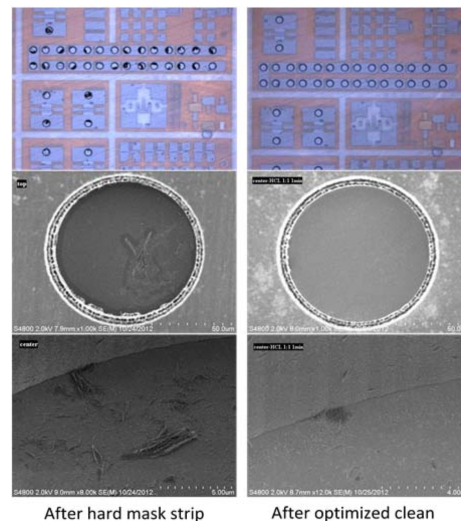

Fig.4 Comparison of the defect level after SiC mask removal and cleaning

The defect topography shown on the right hand side of Figure 4 after the clean process shows over 90% reduction of byproducts. Although there are still some undesired defects on the SiC and GaN interface or GaN surface, the subsequent process is able to remove small byproducts by pretreatment along rim of the edge. Figure 5 shows an Ar pre-treatment step prior to GaN etching which can significantly remove a large amount of surface defects.

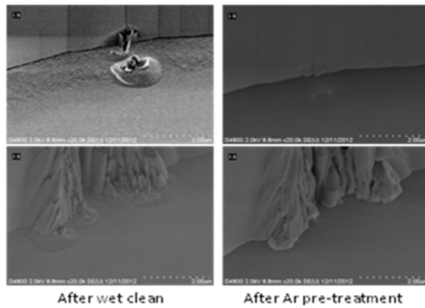

Fig.5 SEM displaying defect level in different steps before GaN etching

The GaN layer was etched using the SiC as the hard mask and stopping on the front-side metal using endpoint detection. The etch conditions of the standard process at WIN was optimized and uses Cl_2/Ar/He chemistries in replacement of the typically used Cl_2/BCl_3 chemistries [3, 4].

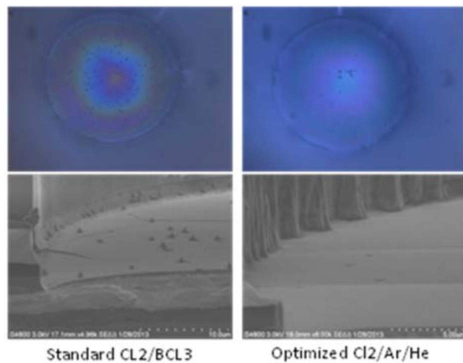

Fig.6 Comparison of the amount of pillars present for various plasma conditions

A systematic reduction in the inherent defects, which can lead to the formation of pillars, is realized. The GaN etch results showing the presence and absence of pillars using different process conditions is shown in Figure 6. To be not mistaken, the pillars formed after etching can't be removed completely.

The sidewall byproduct from GaN etching, however, can be removed using a wet chemical etch procedure with ultrasonic agitation. Either on the sidewall or bottom of the vias, it is noticeable that the byproducts have strong adherence due to a longer ICP etch process time creating more re-depositions. It is possible that due to the anisotropic vertical bombardment of the ICP etch, the chloride byproduct, normally found on the sidewall, can be stripped off the sidewall after being treated in a 2.38% TMAH etchant. The byproduct present at the bottom of the backside via, however, can be mixture of compounds and metal materials that can be removed much better with the aid of ultrasonic agitation in a weak acid such as dilute HNO_3.

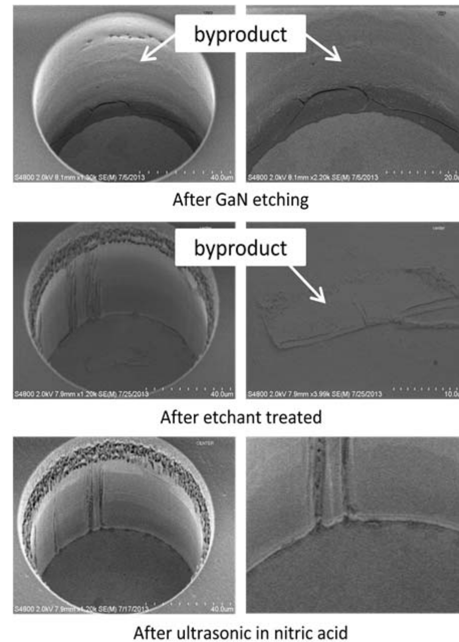

Fig.7 SEM of the clean progression from GaN etching to ultrasonic clean

The backside via cleanliness post GaN etching and prior to and after ultrasonic agitation is shown in Figure 7, wherein the bottom two images are showing improved sidewall and bottom surfaces.

After seed layer metal is deposited by sputtering, a 5µm thick Au layer was electroplated to connect BS metals to FS electrodes. A seamless connection between metallization to both SiC and GaN are critical to the HEMT's electrical performance. A BS via with voids not only results in poor conductivity, but also poses potential reliability issues. The SEM image shown in Figure 8 is illustrating good metal fill inside the backside via, as well as to the bottom of the via, where the BS metallization connects to the FS metal stacks.

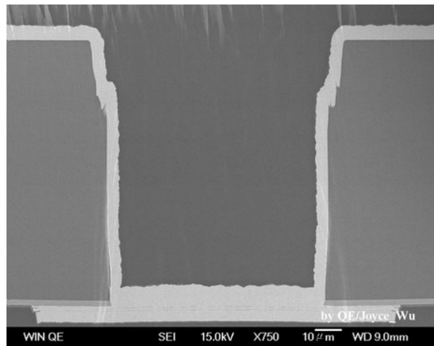

Fig.8 SEM image of the metallized backside via

CONCLUSIONS

The GaN on SiC HEMTs with BS via have been fabricated with controlled etching steps and cleaning procedures. The process yield increased by more than 50% with the outlined critical steps by avoiding pillars and inter-step surface defects. The uniformity of the cleaning process was also verified over a large area of the wafer with the optimized descum clean. The self-aligned substrate mask for GaN etching, with effective end point detection, successfully demonstrates the completed through substrate via process and the successful development of a manufacturable backside via process for GaN/SiC HEMT technology on 100mm wafers.

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