Productivity Improvement Using Plasma-based Die Singulation

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Abstract

Relevant to improved productivity for GaN-on-silicon LED and power device manufacturing, new work is presented on the development of a plasma-based die singulation process for thin Si wafers. The gain in productivity and important benefits through implementation of this enabling technology are discussed.

INTRODUCTION

Over the last two decades, GaN has developed from a novel material with some unique properties into a material system that supports a rapidly growing new industry in both solid state lighting and power electronics.[1,2] In this industry, a significant effort in recent years has focused on lowering manufacturing costs by, for example, exploring growth of GaN on large-area Si wafers as a less expensive alternative substrate to the traditional substrate materials of sapphire and silicon carbide. GaN LED and power devices with acceptable performance have been successfully fabricated on 150mm Si [3,4] and developing on 200mm Si.

Following similar trends in the silicon industry, these GaN devices are being produced on thin Si wafers on the order of 100µm thick. This brings immediate advantages in terms of both device performance and more compact packaging. However, there are new challenges with thin wafers to be addressed that can directly affect yield and hence productivity.

The most notable challenge is for conventional die singulation wafer dicing technology. In this process a high-speed rotating saw is used to separate or singulate each die after their fabrication on wafer substrates prior to final packaging. For substrates with thickness on the order of 100µm or less, productivity is compromised by both the serial nature of the process and the necessary reduction in linear saw cutting speed to prevent wafer breakage. A compounding issue with saws is the induced cracking and crack propagation leading to reduction in die strength. A third limitation with saws is the street width required due simply to the minimum blade size. Singulation using lasers has been introduced with limited success due to a variety of complex issues including alignment, incompatible materials (absorption/reflection), contamination (ablation), and heat affected zones (HAZ).

In this paper**,** we introduce an approach that addresses these issues using plasma based etching on industry standard tape frames. The technology is based on the time-multiplexed deep reactive ion etching (DRIE) technique, originally developed for applications in MEMS.[5] To date, full wafer Si die singulation mounted on standard tape frames has been successfully completed on a variety of different wafer sizes and types including GaN-on-Si.

In the following sections, the plasma-based singulation technology and performance results are discussed. Specifically, the benefits in productivity achieved by high Si etch rates, more die per wafer through reduced street widths, and enhanced yields through improved die strength due to elimination of saw and laser damage are presented. Additional results are also presented showing a unique capability of this technique to produce non-orthogonal die of any shape or geometry.

EXPERIMENTAL

All process work on this project was conducted on a new and uniquely designed production system specifically for plasma dicing of silicon wafers on tape frames at Plasma-Therm LLC. The system, a model MDS™ 100 micro die singulator etch machine is fully automated with a dual cassette tape frame loading station and robotic handler. Following the same procedures as for conventional die singulation, prior to processing the wafers are mounted on conventional tape frames. Wafers sizes up to 200mm can be accommodated on each tape frame. To maintain downstream compatibility with existing packaging work flows, the form factor of the tape frames used follows current industry standards. Both from a logistics and a cost perspective, this is extremely important when introducing a new technology into an existing manufacturing process line.

The etch reactor module on the system is equipped with an inductively coupled plasma (ICP) source and RF-biased lower electrode. During processing the wafer and tape frame are clamped and cooled. Process gases SF_6 and C_4F_8 are used in the time-multiplex alternating etching/deposition cycles to etch the silicon in the streets and fully singulate all the die stopping on the underlying dicing tape.

The system has been specially engineered to handle the wafer mounted on a dicing frame and avoid degradation of the tape during plasma etching. Process termination, when complete wafer dicing has occurred, is achieved by an optical endpoint technique.

RESULTS AND DISCUSSION

A) Productivity Improvement: More Good Die Per Wafer

For conventional die singulation by mechanical saw, the minimum street width is typically limited to about 90µm to accommodate the saw blade. In plasma-based singulation, this restriction no longer applies and streets have now been reduced down to widths of only 10 to 15µm. This frees up a significant amount of valuable real estate to allow more good die to be accommodated on the wafer.

Figure 1 shows the calculated gain in good die per wafer versus die size when the street width is reduced from 90µm down to 15µm. The calculation based on typical die sizes is for a 200mm wafer with a 3mm edge exclusion. From Figure 1, as an example, the percentage gain in available good die per wafer possible by plasma-based singulation ranges from about 3.5% for large die of area 20mm^2 to 31% for small die of area, 0.25mm^2.

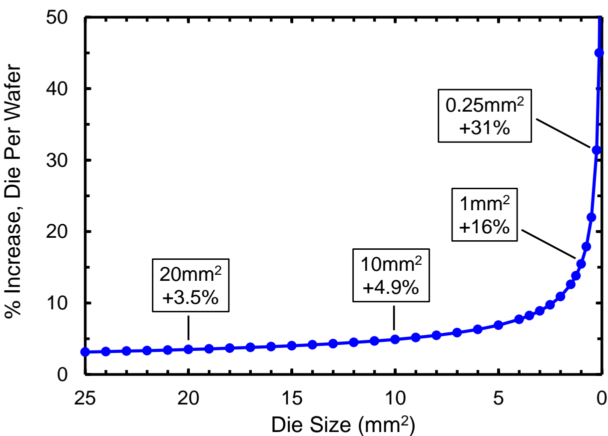

Figure 1. Calculated percentage increase in available complete good die *versus* die size through reduction of street widths from 90 to 15µm. Wafer size is 200mm with 3mm edge exclusion.

Current wafer sizes for GaN range from about 100mm up to 200mm in diameter. It is therefore instructive to translate the percentage gain in good die per wafer for a typical die size into numerical values for these different wafer sizes.

Table I shows, as an example, a comparison of the calculated number of good die available for a typical GaN LED die size of 1mm x 1mm. An edge exclusion of 3mm is assumed for all wafer sizes. The number of additional die that can be achieved to increase manufacturing productivity is significant especially at the larger wafer sizes.

TABLE I: PRODUCTIVITY COMPARISON
GOOD DIE PER WAFER FOR 90 & 15 MICRON STREETS

Wafer Size:	**100mm**	**150mm**	**200mm**
90µm Streets	5,650	13,400	24,500
15µm Streets	6,530	15,500	28,300
Die Gained:	880	2,100	3,800

B) Larger Die: Increased Die Active Area

The advantage of narrowing the street widths is not limited to increasing the number of good die per wafer. The additional real estate gained can be used to increase the existing die size. This increase in active area can be beneficial to device performance. As an example, for power devices, the increased active area leads to a highly desirable reduction in ON resistance. Figure 2 shows the calculated increase in die size available by implementation of the plasma-based singulation when the street width is reduced from 90 to 15µm. A practical demonstration of this concept is reported elsewhere.[6]

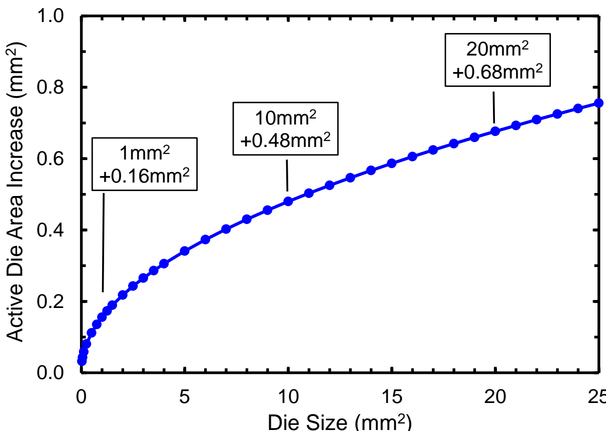

Figure 2. Calculated increase in die active area *versus* die size through reduction of street widths from 90 to 15µm. Wafer size is 200mm with 3mm edge exclusion.

C) Throughput: High Silicon Etch Rate

Throughput in semiconductor manufacturing is often expressed in wafers per hour. In the case of plasma-based etching, this usually depends directly on the etch rate. In this regard, the DRIE process with the capability of high etch rates, controllable feature profiles at high aspect ratios is well suited for high throughput applications. The DRIE Si etch rate is dependent primarily on two parameters, the feature aspect ratio and the exposed Si load. The etch rate increases significantly as the aspect ratio decreases. This is beneficial for die singulation especially for thin die surrounded by narrow streets. The ability to narrow the street width greatly reduces the exposed Si load resulting in higher etch rate. Etch rates on the order of 20µm/min are not uncommon. Typical process times to fully singulate 1mm x 1mm die separated by 15µm streets on a 100µm thick 200mm wafer is about 5 minutes.

D) Productivity: Wafer Start Savings

Figures 3 and 4 shows examples for two common die sizes of the throughput gain achieved with adoption of the plasma-based singulation process. The calculations are done based on predicted process times for 1mm x 1mm and for 3mm x 3mm die on 100µm thick wafers for 15µm streets for wafer sizes of 100, 150, and 200mm wafers. As the result

indicate irrespective of wafer size, for the smaller die, the gains in additional die and wafer start per month savings are significant. For larger die, the wafer starts per month savings begins at a wafer size of 150mm.

Throughput modeling assumes running a mechanical saw system and a single chamber MDS plasma-dicing system over one year at an uptime of 95%. Wafer volume for plasma-dicing is approximately 3,000 wafers per month.

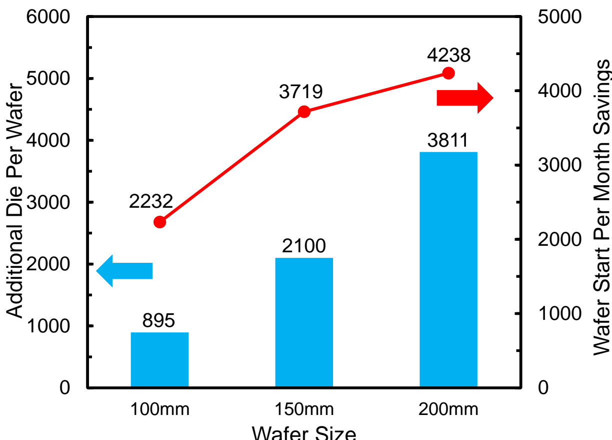

Figure 3. Plasma singulation system throughput showing gain in additional 1mm x 1mm die per wafer and savings in monthly wafer starts.

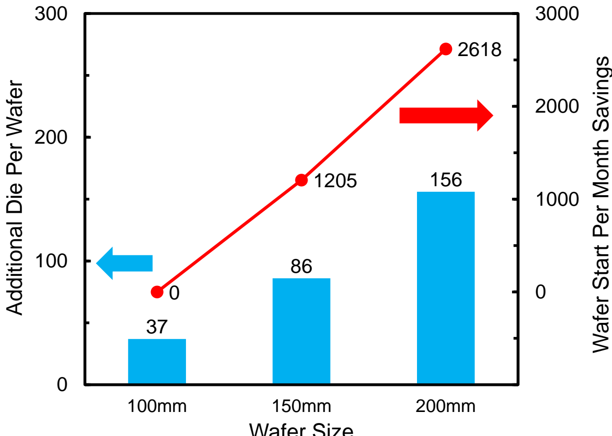

Figure 4. Plasma singulation system throughput showing gain in additional 3mm x 3mm die per wafer and savings in monthly wafer starts.

D) Die Fracture Strength

Die fracture due to the brittle nature of silicon occurs via crack propagation along the surface or from within the material itself. Crack propagation leading to breakage can occur at any time and without warning. It is therefore important to minimize the probability of crack formation and its propagation. This is extremely important for thinned Si wafers which are mechanically extremely fragile and can have high propensity to fracture.

To achieve high die fracture strength, it is therefore critical during the singulation process on these thinned wafers that no cracking or chipping occurs. Figure 5 summarizes the measured relative die fracture strengths for singulated 1mm x 1mm die on 120µm thick Si by mechanical saw, stealth laser, and plasma-based dicing. The die fracture measurements are done using the four-point bending method.

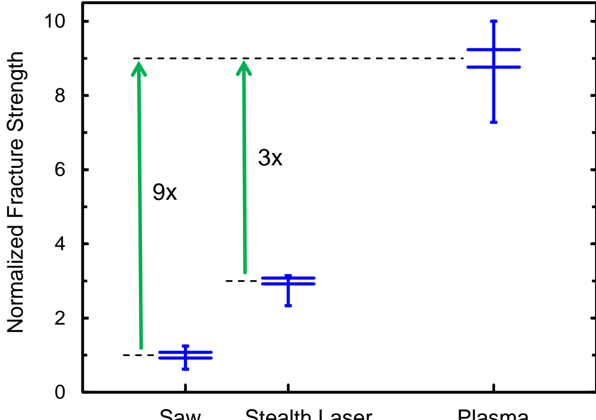

Figure 5. Die strength comparison between saw, laser, and plasma dicing.

As the results indicate, the plasma-based technique has a factor 9 higher improvement in die fracture strength compared to conventional mechanical saw, and about a factor of 3 higher than laser-based dicing. This asserts a key benefit of the plasma-based technique compared to the existing methods; allowing further die thinning compared to the incumbent dicing methods. Porter and Berfield also report improved die strength with the plasma approach compared to traditional mechanical saw.[7]

A weakness of orthogonal die is the localized high concentration of stresses in the small areas at the tips of the die corners. This can lead to fracture. Using the plasma-based singulation method, it is possible to round the corners of the die and thereby minimize the stress. This capability addresses packaging issues especially for very large and ultra-thin die. Figure 6 shows an example of die with rounded corners achieved by the plasma-based singulation process.

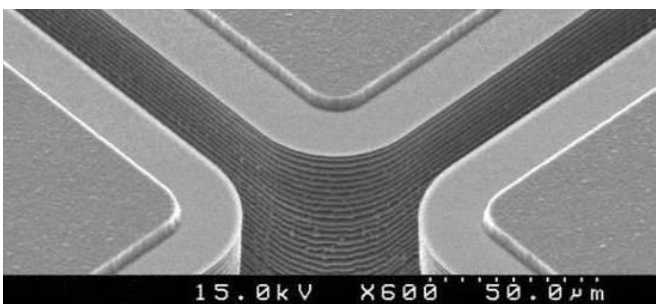

Figure 6. SEM of die with rounded corners separated by 15µm streets.

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E) Die Edge Quality

Figure 7 compares the die edge quality achieved by the die singulation techniques of mechanical saw, laser ablation, and plasma dicing. As indicated by review of the optical

images, in contrast to the saw and laser methods, the die edge quality of the plasma dicing approach is totally free of any defects, debris or cracks. In addition, the final die size is predetermined by the resolution of the lithography step which results in extremely well controlled dimensions.

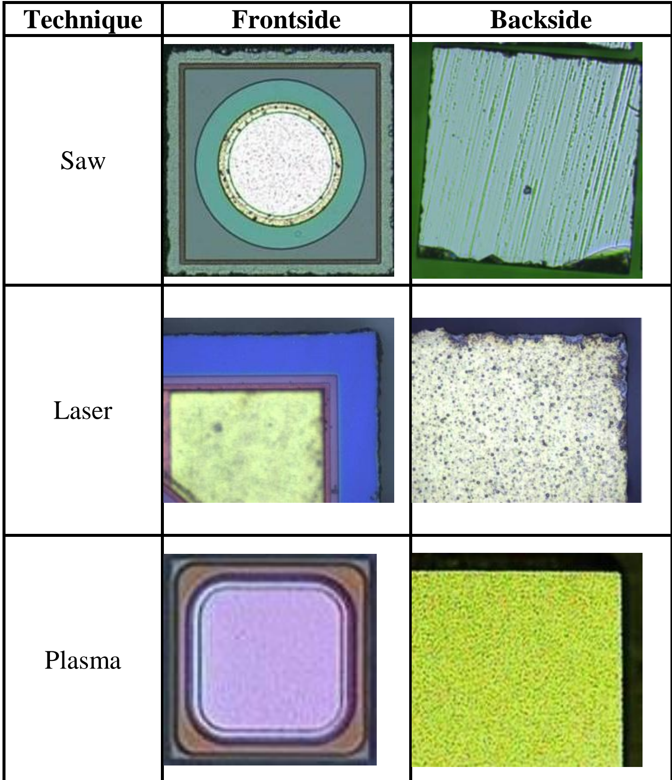

Figure 7. Comparison of die singulation edge quality between saw, laser ablation, and plasma dicing.

F) Non-Orthogonal Die Capability

Majority of die singulated by conventional techniques are either square or rectangular in format and orthogonally aligned on the wafer. With plasma-based singulation, any type of die shape is essentially possible. This opens up new possibilities for creative designers for many different device types in electronic, optical, and optoelectronic applications.

Figure 8 shows an example of hexagonal die singulated by plasma.

Figure 8. Hexagonal die produced by plasma-based singulation viewed by backlit illumination. Die are still on tape. Die dimensions are approximately 150µm.

Conclusions

DRIE-based plasma dicing on tape is an extremely promising technology that is expected to help in manufacture of GaN-on-Si LED and power devices. With this technology, the ability to singulate wafers on conventional dicing tape frames, making easier integration into existing process work flows. Key features of this technology demonstrated relative to conventional die singulation technologies are:

1. Higher Throughput
   More good die per wafer
   Reduced process times
2. Higher Yield
   High die fracture strength
   Low mechanical stress
   No shift in electrical performance
3. New Device Design Potential
   Exclusivity of orthogonal die lifted

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Acronyms

DRIE: Deep Reactive Ion Etching
GaN: gallium nitride
HAZ: Heat Affect Zone
ICP: Inductively Coupled Plasma
LED: Light Emitting Diode
MDS: Micro Die Singulator
MEMS: Microelectromechanical Systems
Si: silicon