

Diamond-coated High Density Vias for Silicon Substrate-side Thermal Management of GaN HEMTs

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Abstract

A process for the development of nanocrystalline diamond (NCD) coated vias in a Si substrate is developed. Vias designed with a nominal diameter of 5-20 μm were dry etched into Si samples, yielding aspect ratios of up to 18 using a three-step SF_6 -based inductively-coupled plasma process. After a multi-step clean, a nanodiamond seeding layer was dispersed inside the vias. NCD coating films of thickness up to 3 μm were grown by a chemical vapor deposition process. Scanning electron micrographs after diamond growth indicate coating along sidewalls of tapered vias. The NCD growth rate near via bottoms was about a third of that on the Si surface. A simulation of an AlGaIn/GaN high electron mobility transistor (HEMT) with an integrated NCD-coated via showed improved drain current due to reduced device operating temperature.

INTRODUCTION

Thermal concerns in semiconductor integrated circuits or discrete power devices need a solution for efficient heat transfer away from the vicinity of the transistor channel, where hot electrons are generated. In the case of III-Nitride based power switching devices, substrate-side thermal extraction would greatly benefit from a high thermal conductivity substrate with a low thermal boundary resistance to the buffer layer. We have previously reported on the electro-thermal benefits of HEMTs capped with nanocrystalline diamond (NCD) [1-4]. In this work, we develop thermal paths in a Si substrate by growing high thermal conductivity NCD films inside vias etched in the substrate. Similarly, filling of through-Si vias (TSVs) with a metal for electrical interconnects is widely employed in the Si industry.

SIMULATION

Table I shows the thermal properties of GaN, 4H-SiC, and single crystal diamond, as compared to Si. Due to the

large thermal conductivity of diamond, high thermal diffusivity can be obtained using this material.

TABLE I
THERMAL PROPERTIES OF RELEVANT DEVICE MATERIALS

Material	k W/cm-K	C_p J/g-K	ρ g/cm ³	a cm ² /s
Si	1.48· (300/T) ^{1,4}	0.7	2.33	0.91
GaN	1.6· (300/T) ^{1,3}	0.49	6.15	0.53
4H-SiC	4.0· (300/T)	0.69 (0.58)	3.1	1.87
Diamond	33	0.52	3.52	16.39

k – thermal conductivity, ρ – bulk density, C_p – specific heat, a – thermal diffusivity, $a=k/(\rho \cdot C_p)$.

The effect of placing such a diamond film in contact with the back side of an AlGaIn/GaN HEMT structure with a 100 μm thick Si substrate was simulated using the ComsolTM simulation package [5]. Details of the simulation procedures are outlined elsewhere in the literature [3, 4]. Figure 1 shows the heat flow distribution in the substrate for the reference device and one where a NCD-coated via has been placed underneath the channel. The effect of the added NCD thermal path along via sidewalls was twofold. First, the peak temperature near the heat source at the drain edge of the gate was reduced by about 50 °C, resulting in an approximately 15% lower device temperature. In addition, increased heat flow in the NCD coating reduced the temperature in the Si substrate adjacent to the via. In practice, such a structure could potentially allow for a reduced gate pitch and increased power density in a power HEMT device.

Figure 2 shows the corresponding recovery in drain current of about 40 mA/mm resulting from the improved thermal profile of a device with fully filled 15 μm -wide vias (7.5 μm thick diamond), compared to a control device with no vias. Note that due to insufficient heat sinking, the cases of HEMTs with vias coated by only 0.5 μm and 1 μm thick diamond yielded lowest drain currents.

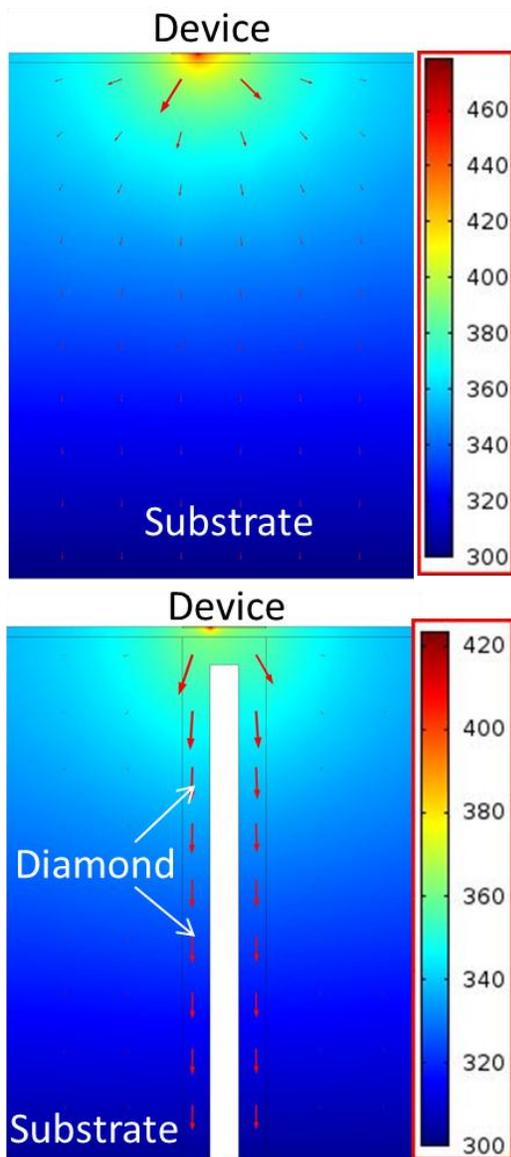
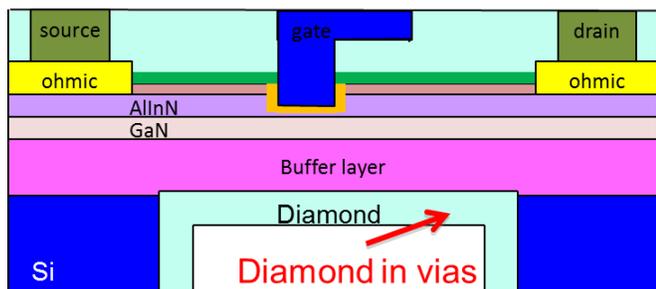


Fig. 1. Heat flow simulation of an AlGaIn/GaN HEMT with a Si substrate without and with a diamond-coated via placed directly underneath the device. The simulated output power was 9 W/mm.

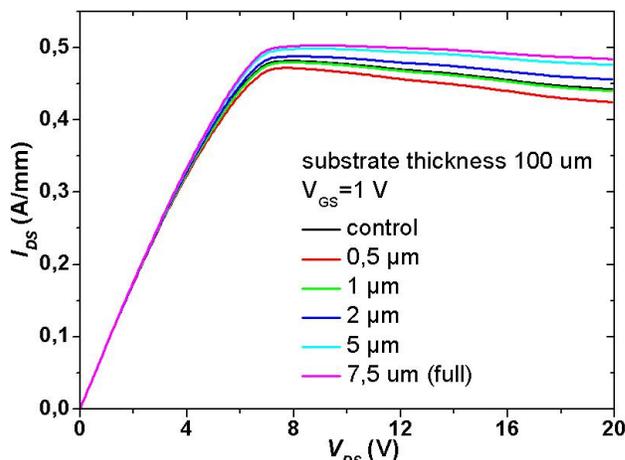


Fig. 2. I_{DS} - V_{DS} ($V_{GS} = 0$ V) curves of the simulated AlGaIn/GaN HEMT as a function of diamond thickness in the via.

EXPERIMENTAL

Table II outlines the three-step fabrication process for NCD-coated vias. First, deep trench patterns (a.k.a., vias) were etched in Si (111) using an SiO_2 mask and a cryogenic inductively coupled plasma (ICP) process (-100 °C, 100/5 sccm SF_6/O_2 , 1000/9 W ICP/RIE power, -56 V DC bias). The etch rate was highly dependent on via diameter (5-230 μm) and exposed Si wafer area (from $<5\%$ to $>95\%$), as shown in Fig. 3, but tended to saturate with increased feature size. Aspect ratios (depth/diameter) of up to 18 were routinely obtained with less than 1 hr etch time, depending on total exposed area of unmasked Si in the ICP reactor.

Following a multi-step cleaning process to remove debris in the vias, a seeding step with 5-25 nm diameter nanodiamond seed solution was performed, followed by the NCD growth process. NCD films with 2-3 μm thickness were grown by microwave plasma-enhanced CVD at 750 °C [6]. However, growth of NCD inside vias with aspect ratios above 10 was limited by vapor diffusion inside the trench. To increase the NCD growth rate and improve diamond film uniformity inside high aspect ratio vias, a via sidewall taper process was developed by introducing additional O_2 later in the ICP process to increase the sidewall etch rate [7]. Figures 4 and 5 present scanning electron micrographs (SEM) of top-side and cross section portions of tapered vias coated with NCD.

A 3° taper angle was experimentally determined to be sufficient for complete diamond penetration inside vias with effective aspect ratios of around 10. Here, we define effective aspect ratio as the depth/diameter aspect ratio where the diameter is averaged by top and bottom dimensions of a tapered via. Figure 6 shows a substantial (nearly a factor of 2) improvement in both sidewall diamond thickness ($d_{\text{NCD, sidewall}}$) and via aspect ratio using the tapered via process. Therefore, a 20 μm diameter via etched to a

depth of 200 μm can be filled with NCD using a tapered via etch process and a sufficient NCD growth time.

TABLE II
PROCESS SEQUENCE FOR NCD-COATED SILICON VIAS

Step	Description
I. Si etch	Temperature: $-100\text{ }^{\circ}\text{C}$, ICP/RIE power: 1000/9 W, pressure: 11-15 mT, etch rate: 1.5-3 $\mu\text{m}/\text{min}$. depending on total area of exposed Si. 1) Deep etch step: 100/5 sccm (20:1) SF_6/O_2 , 20-30 min. 2) Taper etch step: 80/20 sccm SF_6/O_2 , 20 min. 3) Lip removal step: 100/5 sccm SF_6/O_2 , 1-2 min.
II. Si clean	1) EKC265 TM , $75\text{ }^{\circ}\text{C}$, 10 min. 2) 3:1 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ (piranha), 10 min. 3) 1:1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (SC-1), 10 min., ultrasonic clean 4) Buffered-HF, 4 min.
III. NCD growth	1) Seeding phase: nanodiamond seed dispersion 2) Nucleation phase: Temperature: $750\text{ }^{\circ}\text{C}$, 10-20 Torr, 900 sccm H_2 , 3 sccm CH_4 , $750\text{ }^{\circ}\text{C}$, 800 W, 19 hrs ($\sim 0.1\text{ }\mu\text{m}/\text{hr}$). 3) Growth phase: Temperature: $750\text{ }^{\circ}\text{C}$, 15-25 Torr, 900 sccm H_2 , 3 sccm CH_4 , 800 W, 19 hrs ($\sim 0.1\text{ }\mu\text{m}/\text{hr}$).

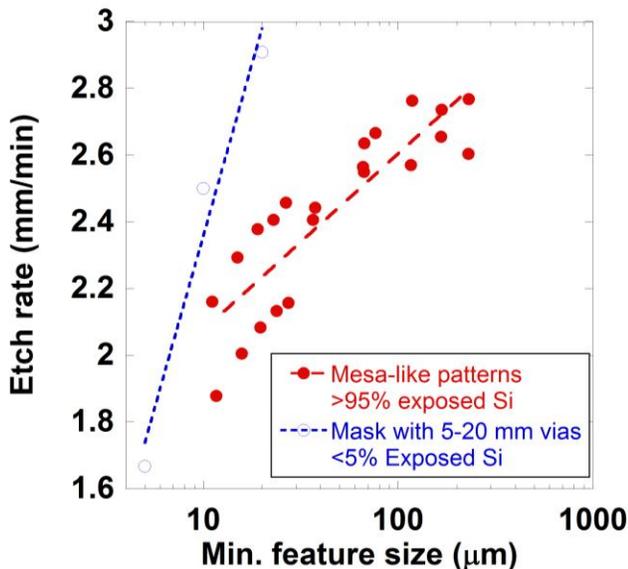


Fig. 3. Si etch rate versus feature size in the case of circular vias masked by SiO_2 (blue empty circles) and large mesa-like patterns (red filled circles). Etch rates were limited by the amount of unmasked Si during ICP etching.

DISCUSSION

The above-described process for NCD-coated vias allowed for a high density of diamond replacing a substantial volume of a Si substrate. This approach overcomes the slow growth rate of diamond, which historically has precluded this material from commercial development as a substrate for semiconductor devices and integrated circuits. By reducing via dimensions and increasing via packing density, the volumetric growth rate of NCD is increased. To that end, hexagonally-packed circular via patterns in Fig. 4 were an optimal structure for growing a maximum volume of diamond in the shortest period of time.

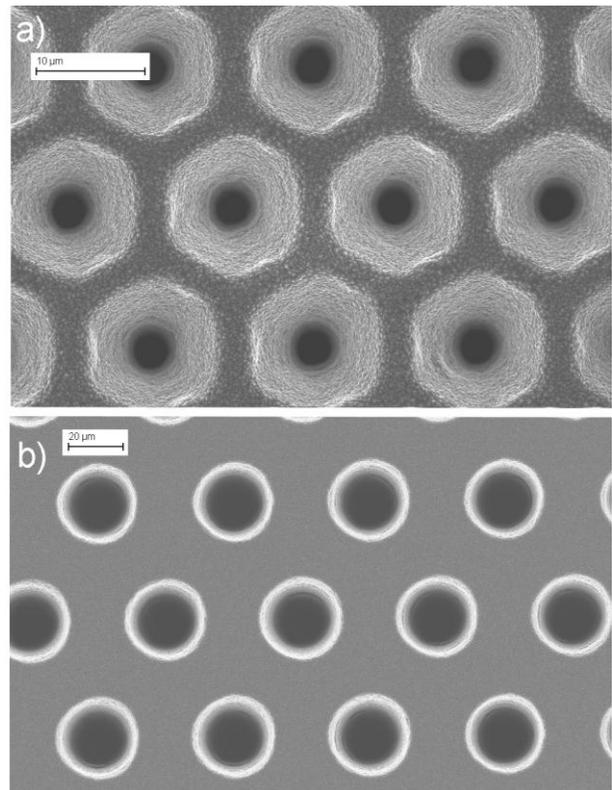


Fig. 4. Top-side micrographs of a) vias tapered to about 10 μm near the top-side and b) 20 μm wide NCD-coated vias.

This process requires several important optimizations in order for a GaN-based HEMT device grown on a Si substrate to be integrated with the proposed via process. First, the additional stress from the diamond films growing over via edges will cause excessive wafer bow. To this end, a selective diamond growth process has been proposed by Hobart et al. [8]. In addition, the Si etch must stop reliably on or near the GaN nucleation layer (usually AlN or AlGa_N, or a combination thereof) in order to bring the NCD as close as possible to the III-Nitride film. Finally, the lateral thermal conductivity of NCD (through column boundaries) must be improved as NCD columns grown laterally on via sidewalls will be placed perpendicularly to the heat flow.

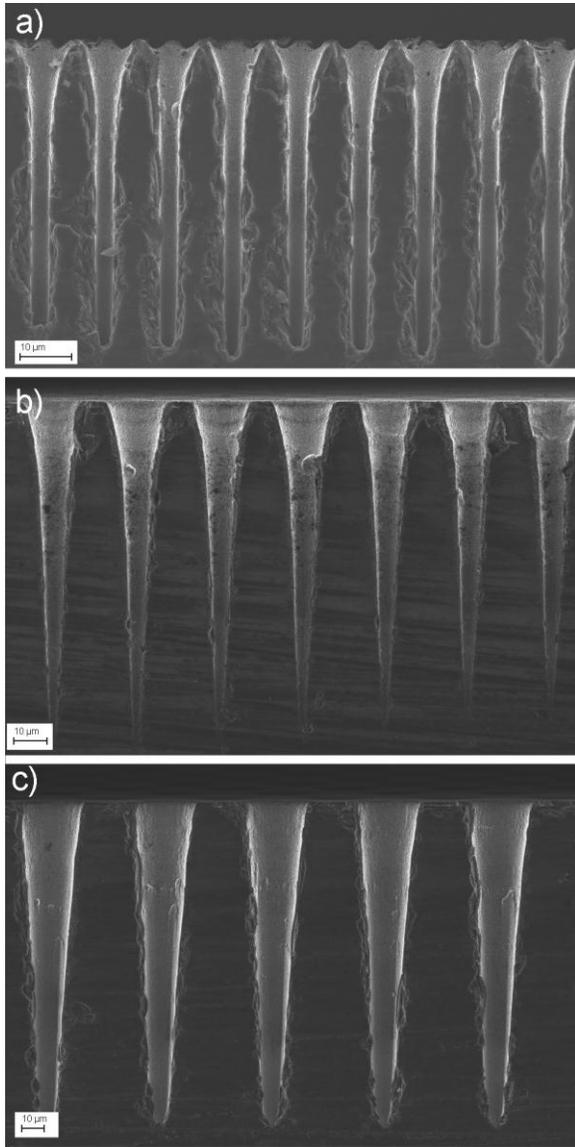


Fig. 5. Cross-sectional profiles NCD-coated vias with a) 5 μm , b) 10 μm , and c) 20 μm nominal top-side diameters. Wider opening diameters were induced by isotropic sidewall etching at a higher O_2 content in the SF_6 -based ICP chemistry.

CONCLUSIONS

In three dimensions, plasma-assisted dry etch processes develop a steady-state deposition rate defined by the precursor diffusion rate inside a lithographically-defined etch pattern. Applied to thermal management of GaN-based transistors, this method has the advantage of providing a substrate-side thermal management solution that avoids both blanket substrate removal and long diamond growth due to the small volume of the etched vias. Combined with top-side diamond cooling, this process could provide an efficient thermal management solution for power switching GaN devices.

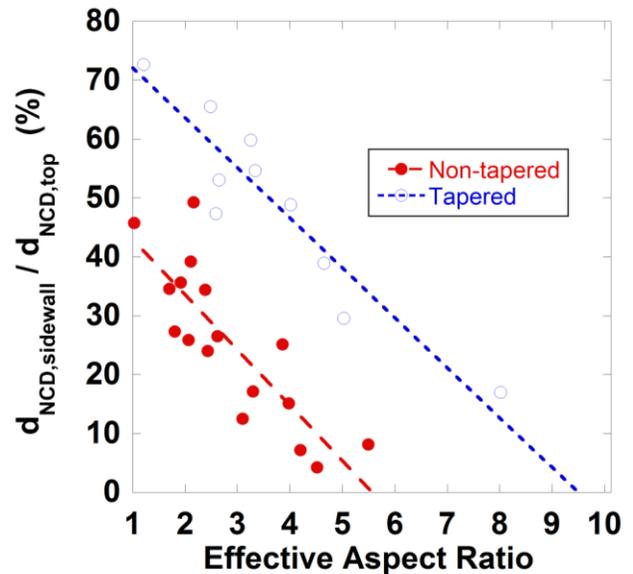


Fig. 6. Aspect ratio improvement by means of via tapering, measured by sidewall diamond thickness as a percentage of top-side diamond thickness at a given diameter and depth (i.e., effective aspect ratio) inside a Si via.

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ACRONYMS

NCD: Nanocrystalline diamond
 HEMT: High electron mobility transistor
 TSV: Through Silicon via