High Speed Highly Parallel Multi-site GaAs Diesort Testing

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Abstract

We report here on improved test productivity and lowered diesort test cost from using large numbers of SMUs so that each circuit contacted by a multi-site probecard can be tested almost simultaneously.

'Tis not sleepy business;
But must be look'd to speedily and strongly.
Shakespeare, Cymbeline, Act III, Sc. 5

INTRODUCTION

On-wafer DC screening of GaAs integrated circuit die is crucial for cost-effective fabrication of multi-chip modules. However, cost of that test must be tightly controlled and it must be done "speedily and strongly". Traditional switch matrix – based test systems have small numbers of DC IV source measurement units (SMU's). Users of those systems can reduce test time and lower cost by contacting multiple (typically 4, 6, or 8) die at each step then testing them serially. That reduction is only in the probe stepping time component of total test time.

We report on our development of high-SMU-count Keithley S500 parallel test systems for this application. These systems have no switch matrix and test all contacted die simultaneously, allowing for significant test time reduction in addition to the stepping time reduction from multi-site probing.

SYSTEM DESCRIPTION

Our systems are configured in 6 parallel groups each with 10 SMU's for hex-site diesort testing of our 150 mm GaAs wafers using cantilever, vertical, or pyramid probe cards. Each group's SMU's are arranged with a single master SMU and 9 slaves, giving 10 independent SMU's per site. The test code is pre-loaded into the master SMU of each group and is executed under its control when strobed by the system controller, as shown in Figure 1. Each die under test is then tested essentially simultaneously with only status checking and data transfer done serially. The tester is pictured in Figure 2 below.

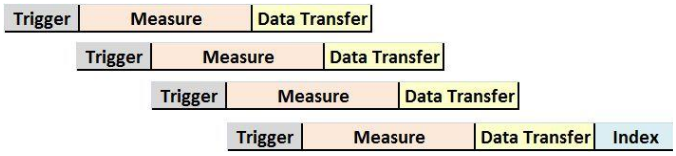

Figure 1. Timing Cartoon for Quad-site Parallel Test

Our first approach used the script language resident in these SMUs to perform measurements with sequential commands at runtime. This combined with quad-site parallel test led to an estimated 10-fold increase in the throughput of the traditional single site switch matrix-based systems. Further optimization followed, increasing sites contacted to 6 and employing best practices in test code to further speed up the test.

Using six parallel groups of the Keithley Instruments S500 System SMU's with hex-site probing, we have demonstrated 100 msec total test time per die for basic diesort test (total time per wafer divided by number of die tested). This has substantially reduced test time and cost for our HBT Power Amplifier wafers, which typically have 15 – 30,000 testable die per wafer.

From a manufacturing cost-of-test perspective, these 6x10 SMU test systems are built from arrays of 30 relatively inexpensive dual-SMU boxes with most of the system

Figure 2. 6x10 SMU configured S500 diesort test system

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definition and control done in commercial off-the-shelf hardware and software system components from Keithley Instruments. So, capital costs are comparable to mid-scale switch-matrix-based test systems. By developing a commercially-integrated system, we have preserved a test process traceable to calibration standards and with a viable maintenance strategy.

Key to optimization of test throughput, the Keithley Instruments 2600 series SMU's have on-board test script processing (TSP) and a proprietary synchronization method called TSP-Link to tightly couple source and measurement operations between multiple units. By off-loading measurement instructions and responses to on-board scripts via TSP, we minimize communication with the system controller and allow each group to run in parallel. Also, by minimizing the duration of these measurement tasks, we maximize the total test throughput and parallelization.

These test systems combine the 2636A Dual-Channel System Source Meters with ACS (Automated Characterization Suite) Software along with appropriate cabling, power, and a 9139A Probe Card Adapter. The ACS software is capable of controlling multiple Source Meter group masters in parallel, pre-loading TSP scripts to the System Source Meters, and retrieving data in a parallel for logging to test data files. Wafer and Die descriptions are defined in ACS to support graphical representation of test results and prober control. Production user and Engineering user access modes are available based on log-in, and facilities are provided for command-line control. Interactive modes and fully automated modes provide useful tools for development and full production operation.

The Keithley testers are coupled with TEL DP wafer probers to complete the test systems. Those probers allow testing of full thickness wafers, thinned wafers on metal support plates, or thinned wafers on saw tape.

By achieving higher throughput with multi-site parallel test and the Keithley S500 system architecture, we need fewer test systems for given wafer volumes, gaining significantly higher test productivity and lower test cost per die.

OUR DIESORT TEST

Avago's basic diesort test for GaAs Power Amplifiers (PA's) is a simple test of quiescent current for each PA stage and operational mode (usually High Power Mode (HPM) and Low Power Mode (LPM)) and Leakage current for each PA stage. It is normally done as "Force Voltage – Measure Current."

Previously, this was done as a single site test on Agilent 4070 platforms, taking as much as 6 hours per wafer. At low fab volume, that very long test time was not a big concern, but as volumes increased we had to drastically speed up that test step by going to multi-site test and changing to Keithley S500 semi-parallel test.

We have found that quiescent and especially leakage currents measured in our system are not stable after applying voltages unless we apply delay times in the 15 – 25 msec range. This results in a situation where stepping time reduction, an assumed benefit of multi-site test, is not a big factor in total wafer test time.

To investigate that, we evaluated different stepping patterns for "X-stacked" quad -site probe cards, as illustrated for one reticle in Figure. 3. One can either take a large number of long steps in X with a small number of small steps in Y ("X-Stepped") or a large number of small steps in Y with a small number of larger steps in X ("Y-Stepped"). The total stepped distance is substantially less for the latter. For example, for a large 1.28 x 0.78 mm die on a 160 x 20 die array tested quad site, we expect a 4.0 meter indexing distance for X-stepping vs. 0.7 meters indexing distance for Y-stepping.

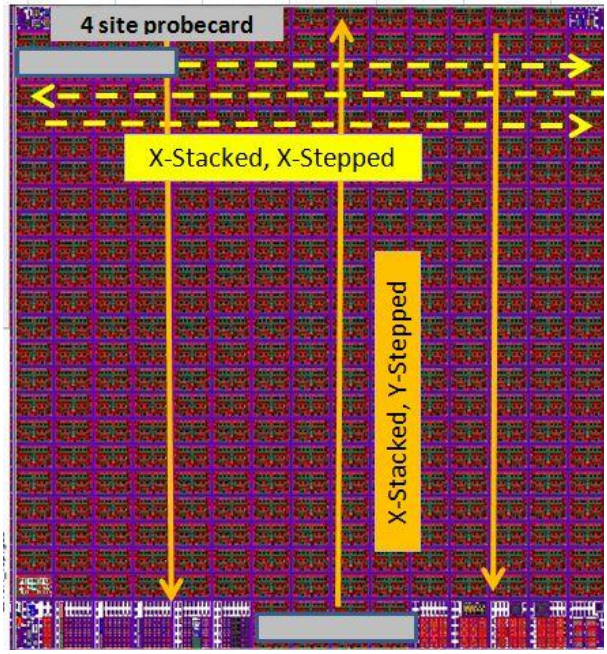

Figure 3. Stepping Options (Quad-site test shown)

However, we observed a negligible difference in wafer test time for the two approaches testing a die of that size over a whole wafer (over 14,000 die). This led to our focus on minimizing test time rather than index time. Test overhead ("Trigger" and "Data Transfer" in Figure 1) could also be reduced in the next improvement step.

RESULTS FROM NEW SYSTEMS

Examples of data comparisons for the two approaches are shown in Figure 4 and 5 for typical quiescent current and leakage current tests on the same wafer. The plots are cumulative probability plots for an old system APT10 and two new systems WS01 and 02. One can see that the new system results are in good agreement with the old for the same wafer.

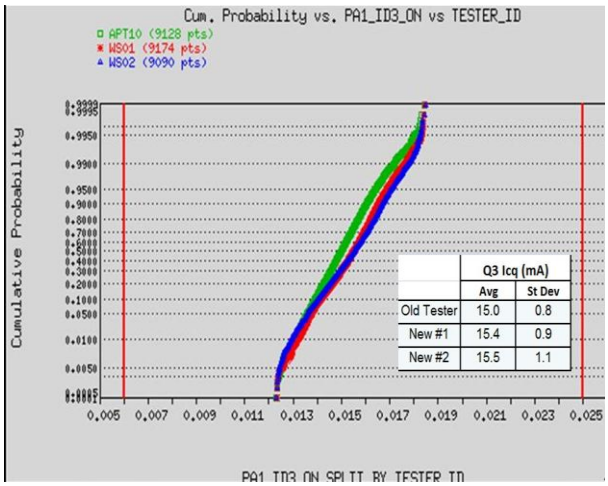

Figure 4. System Matching – PA Quiescent Current

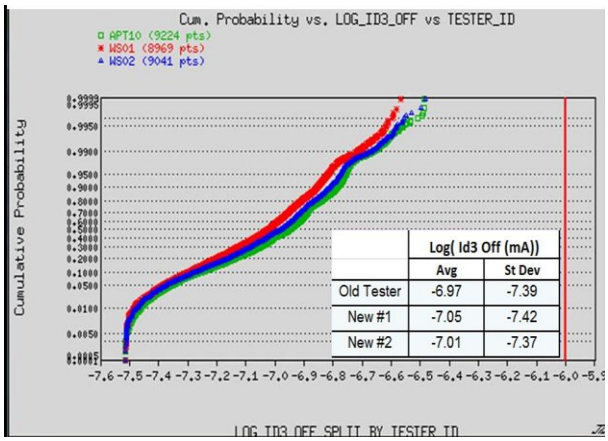

Figure 5. System Matching – Log(PA Leakage Current)

Resistor Diagnostic Board Repeat Tests using PA Quad Site Test

all currents in mA

	R1	R2	R3	R4
count	1005	1005	1005	1005
Average	0.8001	3.4013	6.8038	10.1997
Sdev	0.0005	0.0004	0.0010	0.0013
% Sdev	0.067%	0.013%	0.015%	0.013%

Table 1. Tester Repeatability for Resistor Test

SYSTEM CHALLENGES

The biggest challenge in this approach is matching Probe Card (PC) site to site test. In the old system, every DUT was tested with the same SMU's and same probe pins so matching was not an issue. In the new system, different sets of SMU's, cables, and PC pathways measure each DUT site.

Special precision resistor PCs with multiple sites were made for system diagnostic measurements. These resistor DC measurements match very well from site to site (Table 1), and fall within SMU specification limits, de-rated to accommodate cable length and PC uncertainties.

However, when DC testing is done on high bandwidth / high gain devices, which are susceptible to RF instabilities, site to site matching is difficult to achieve due to factors such as differing parasitics between each site's connection pathways, measurement devices, and DUTs. Interactions of pin-to-pin combinations can also contribute. Therefore, special care has to be paid to suppression of these instabilities through shunt capacitors in series with resistors

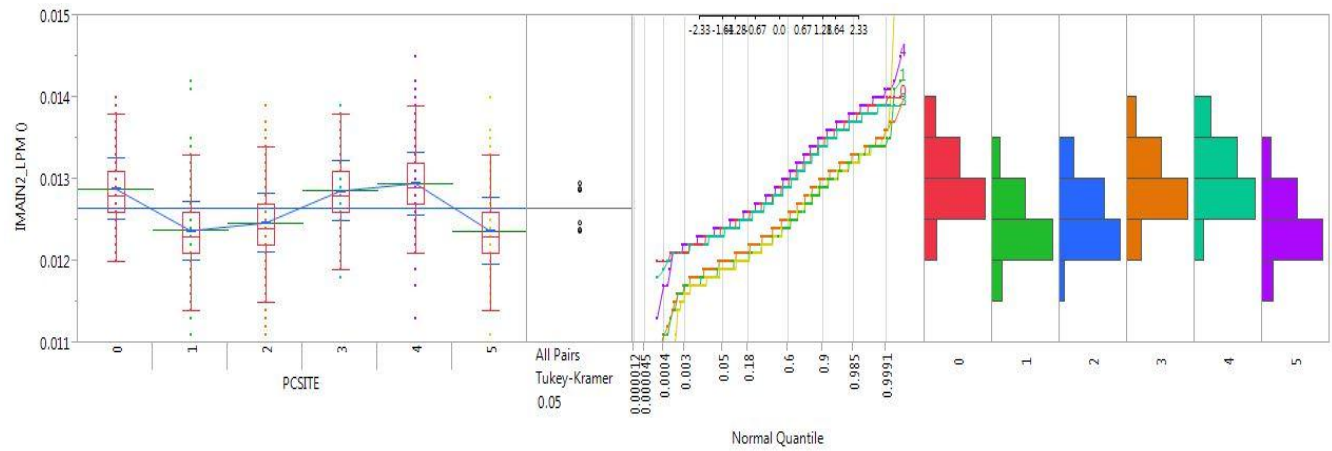

Figure 6. Diesort site to site matching (~13 mA Icq)

as RF ground and tip inductance de-Q'ing elements. These suppression devices themselves become part of the overall site characteristics.

Figure 6 shows site to site variation over a wafer (30,189 sites tested) for a hex-site test of a PA mode with about 13 mA of quiescent current. One can see that this part has about 0.6 mA variation from lowest to highest site means (12.4 to 13.0 mA). More work can be done at a system level to further understand and improve the site-to-site measurement variability.

CONCLUSIONS

We have successfully installed multi-site, highly parallel diesort test in a production GaAs IC fab resulting in increased efficiencies and lowered die test costs. Work continues to understand and minimize both test time and probe card site to site variations.

ACKNOWLEDGEMENTS

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ACRONYMS

ACS: Advanced Characterization Suite
DUT: Device Under Test
HBT: Heterojunction Bipolar Transistor
HPM: High Power Mode
LPM: Low Power Mode
PA: Power Amplifier
PC: Probe Card
SMU: Source Measurement Unit
TEL: Tokyo Electron Ltd.
TSP: Test Script Processor