Process-dependent properties of InAlN surface and ALD-Al_2O_3/InAlN interface

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Abstract

We report that the properties of the InAlN surface and the ALD-Al_2O_3/InAlN interface are dependent on the interface formation process. XPS revealed that the native oxide layer on the air-exposed InAlN surface was mainly composed of Al hydroxide and was efficiently removed by HF-based chemical treatment. The electrical characterization on MOS diodes indicated that the electronic properties of the ALD-Al_2O_3/InAlN interface were much affected by the formation process and that the properties can be improved by the atomic-layer-level structural control combined with annealing.

INTRODUCTION

InAlN lattice matched to GaN is promising material to achieve a high-power/high-frequency III-nitride HEMT, owing to its ability to achieve a high electron barrier and a high-density polarization charge resulting in high density 2DEG [1]. In the application to HEMTs, the leakage current through the InAlN barrier is a residual problem if we use the metal-InAlN Schottky barrier contact as the gate structure. This problem can be avoided by the usage of a gate insulator to form a MOS gate [2]. Actually, a high cut-off frequency of an InAlN/GaN MOSHEMT has been achieved [3]. Beside the demonstration of the high performance, knowledge on the surface/interface properties that is useful for the device process design is not fully investigated. Especially, the insulator/InAlN interface properties are quite important to control the device characteristics, e.g. the threshold voltage, the sub-threshold swing, and the long-term stability of the MOSHEMTs. For the preparation of the insulator/InAlN interface, an appropriate control of the InAlN surface is unavoidable in the practical process design for the III-nitride device fabrication.

We would like to present the process-dependent properties of the InAlN surface and the ALD-Al_2O_3/InAlN interface. ALD is the most precise insulator deposition method, whereas Al_2O_3 is one of the promising insulators. For the fabrication of the InAlN MOS structure, the chemical composition of the native oxide layer was analyzed based on the XPS measurement to find the removal method. Then we present the effect of annealing on the properties of the Al_2O_3/InAlN interface. Finally, two-step ALD combined with high-temperature annealing is introduced as a control method for the Al_2O_3/InAlN interface with avoiding the microcrystallization of the Al_2O_3 layer.

EXPERIMENTAL

The XPS measurement was performed using a monochromated Al-*Kα* X-ray source (1486.6 eV). The Al_2O_3 layer was formed by ALD at 350 ^oC using H_2O and trimethylaluminum. The SiN_x layer used as a cap layer for ohmic contact annealing was deposited by ECRCVD at 270 ^oC using a SiH_4/Ar and N_2 gas mixture. Ohmic contact annealing was performed at 850 ^oC for 1 min in nitrogen flow in a separate furnace. Annealing for Al_2O_3/InAlN interface prior to the formation of the Ni/Au electrodes, including that for an ultrathin Al_2O_3 layer, was also done at 850 ^oC because this temperature was harmless for InAlN as was guaranteed by ohmic annealing.

RESULTS AND DISCUSSION

Removal of native oxide layer on InAlN surface

The XPS O1s spectral intensity was reduced efficiently by HF-based solution at room temperature as shown in Fig. 1, compared with that from the as-served $In_{0.17}Al_{0.83}N$ surface. However, HCl (at room temperature) and NH_4OH (at 50 ^oC) treatments were not effective, which seems to be related to the chemical properties of oxide components. In fact, we found that the native oxide layer on the air-exposed InAlN surface mainly consisted of Al hydroxide components [4] as shown in Fig. 2. Since hydroxides are not stable thermally and chemically, native oxide formed upon air exposure should be removed before interface formation. We confirmed that the HF-based treatment removed the native oxide layer efficiently leaving only the absorbed water component. Furthermore, native oxides were not generated in air for 1 hour on the HF- or BHF-treated InAlN surfaces [5]. The existence of the surface native oxide layer on the air-exposed surface implied the possibility of an uncontrolled surface oxidation during a careless device fabrication process. Actually, during high-temperature ($\geq$ 800 ^oC) annealing, the bare InAlN surface was oxidized by the trace contamination in a furnace even in nitrogen flow. Such uncontrolled oxidation leads to the generation of the surface/interface states to deteriorate the device performance. For example, if the device fabrication needs ohmic-contact annealing at a high temperature, the InAlN surface should be protected by an appropriate insulator layer to achieve cap annealing.

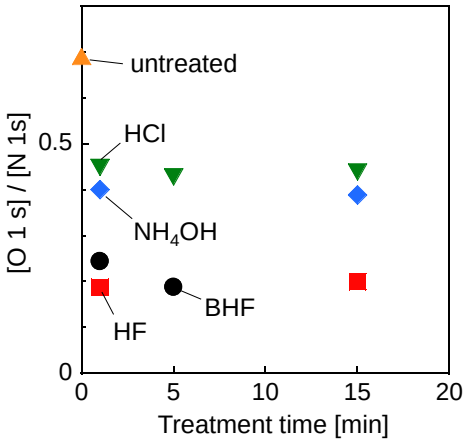

Fig. 1 [O 1s]/[N 1s] vs treatment time.

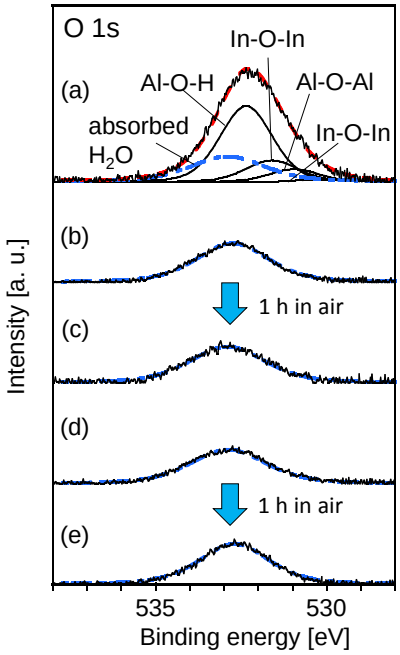

Fig. 2 O1s spectra obtained for (a) as-served InAlN surface and surfaces treated with (b) HF for 1 min, (c) 1-h air exposure after 1-min HF treatment, (d) BHF for 5 min, and (e) 1-h air exposure after 5-min BHF treatment.

Control of ALD-Al_2O_3/InAlN interface

XPS for the interface between an ultrathin ALD Al_2O_3 layer and the host InAlN layer revealed that the conduction band offset was as large as 1 eV as shown in Fig. 3, which indicated that the ALD-Al_2O_3 layer was suitable as a barrier for electrons. However, the interface properties are found to be sensitive to the interface formation process.

To investigate the process-dependent properties of the Al_2O_3/InAlN interface, MOS diodes with ALD-Al_2O_3 layers

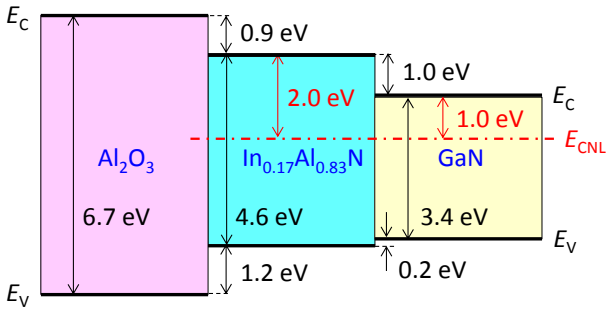

Fig. 3 Band line-up of Al_2O_3-InAlN-GaN system.

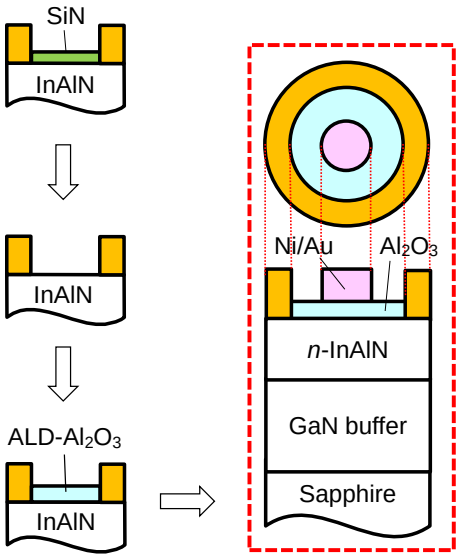

Fig. 4 Fabrication sequence for MOS diodes.

were fabricated and tested. The optimized fabrication sequence and the sample structure of the tested MOS diode, having the ALD-Al_2O_3/$In_{0.17}Al_{0.83}N$ interface, are illustrated in Fig. 4. To investigate the Al_2O_3/InAlN interface separately from the heterointerface, the InAlN layer was highly doped (n = 2.0 ×10^{18} cm^{-3}) and sufficiently thick (160 nm). A circular Ni/Au (20 nm/50 nm) electrode was formed on the Al_2O_3 layer keeping the concentric gap to the surrounding Ti/Al/Ti/Au (20 nm/50 nm/20 nm/100 nm) ohmic electrode. The 160-nm-thick Si-doped epitaxial InAlN layer and an underlying 2-µm-thick GaN buffer layer were grown on a sapphire substrate by MOVPE.

As has been reported previously [6, 7], annealing the amorphous Al_2O_3 layer at the high temperature (≥ 800 °C) led to high leakage current in the completed MOS diode as shown in Fig. 5. The possible reason was microcrystallization of the Al_2O_3 layer [7]. Therefore, ohmic-contact annealing should be carried out prior to ALD of Al_2O_3 for achieving an improved performance of the MOS diode. However, we found that capless annealing led

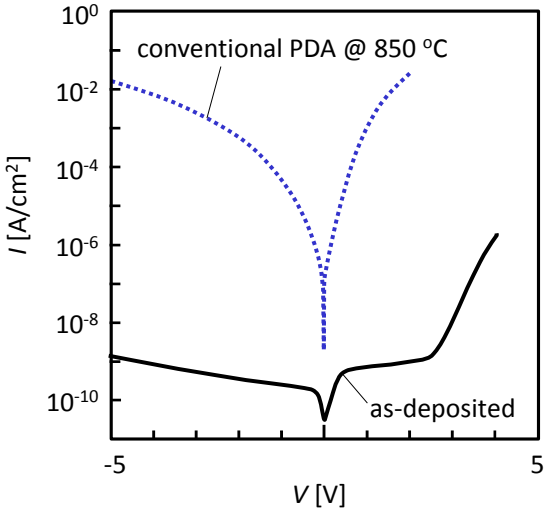

Fig. 5 I-V characteristics of MOS diodes.

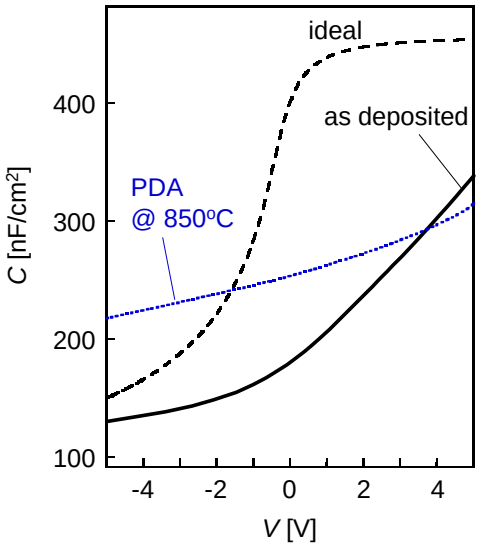

Fig. 6 C-V curves of MOS diodes.

to an unintentional oxidation of the InAlN surface due to the trace contamination inside the furnace as is discussed above. As the surface protection layer during ohmic-contact annealing, the SiN_x layer deposited by ECRCVD was found to be appropriate [8]. In this ohmic-first manner, the leakage current was reduced well as is also shown in Fig. 5. Figure 6 summarizes the C-V curves measured at 1 MHz for the MOS diodes. The solid line shows that for the sample fabricated by the process shown in Fig. 4 before PDA, which indicates that the slope is not sufficiently steep compared with the ideal curve. Even the ALD-Al_2O_3 layer was formed after the ohmic-contact annealing using the SiN_x cap layer, a mere ALD of the Al_2O_3 layer did not lead to a sufficiently low interface states. Though annealing can improve the interface properties, we found that PDA at 850 °C led to a deterioration of the interface properties resulting in a small capacitance change as shown by dotted line in Fig. 6.

Nevertheless, our XPS study showed the possibility that the Al_2O_3/InAlN interface is not deteriorated by high temperature annealing if the Al_2O_3 thickness is very thin. Figure 7 shows the coincidence of the example core-level spectral shapes before and after annealing at 850 °C for the structure with a 2-nm thick Al_2O_3 layer on InAlN. No sign of intermixing caused by annealing was seen. Based on these results, to reduce interface states at the Al_2O_3/InAlN interface efficiently, we developed the two-step ALD process [9] as shown in Fig. 8. In this process, annealing at the high temperature (850 °C) for the initial ultrathin ALD-Al_2O_3 layer was done prior to the subsequent deposition of the thicker outer layer. The C-V curve measured for the MOS diodes fabricated by this process is shown in Fig. 9. Improved characteristics indicated the reduction of interface states.

Figure 10 shows the evaluated interface state density (D_{it}) distributions for three kinds of samples. By the appropriate formation process, D_{it} lower than 10^{12} $cm^{-2}eV^{-1}$ was obtained in the energy range within 1 eV from the conduction band edge as shown in Fig. 7. Since the charge neutrality level E_{CNL} locates 2.0 eV below the conduction band edge, these states behave as acceptor-like states. We would like to stress that the Al_2O_3/InAlN interface properties are sensitive to or dependent on the fabrication process and thermal treatment.

CONCLUSIONS

The properties of the InAlN surface and the ALD-Al_2O_3/InAlN interface are dependent on the device fabrication process. The native oxide layer on the InAlN surface is dominated by hydroxides and can be efficiently removed by the HF-based treatment prior to the device fabrication. It has been also shown that the electronic properties of the ALD-Al_2O_3/InAlN interface can be improved by the two-step ALD process combined with annealing.

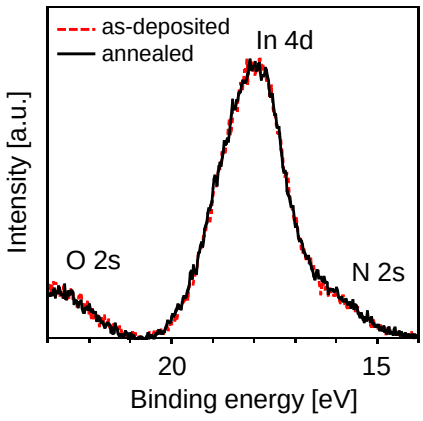

Fig. 7 In 4d, O 2s, and N 2s core-level spectra from ultrathin-Al_2O_3/InAlN structure.

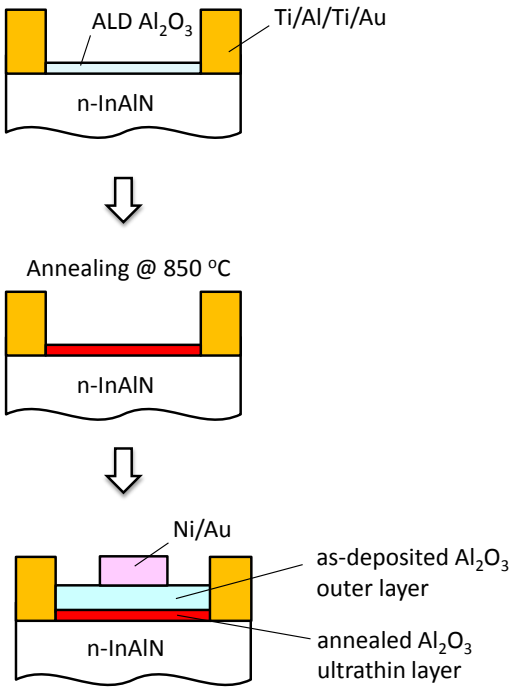

Fig. 8 Two-step ALD process.

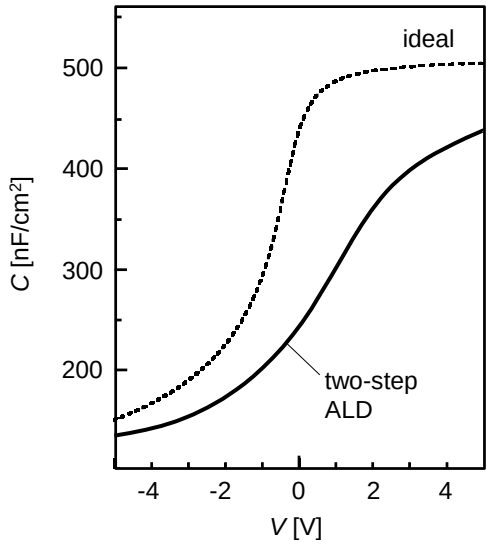

Fig. 9 C-V curve measured for MOS diode fabricated by two-step ALD process.

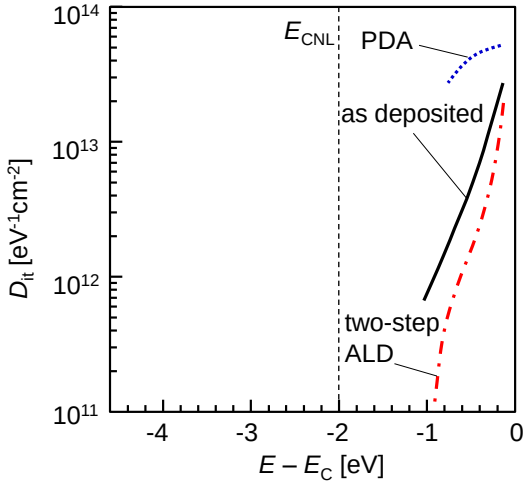

Fig. 10 D_{it} distribution derived from C-V curves.

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ACRONYMS

ALD: atomic layer deposition
ECRCVD: electron-cyclotron-resonance chemical vapor deposition
HEMT: high-electron-mobility transistor
MOVPE: metal-organic vapor-phase epitaxy
MOS: metal oxide semiconductor
XPS: X-ray photoelectron spectroscopy