Fabrication of GaN MISHEMTs Fabricated From GaN Grown By MOCVD on High Resistance 200mm <111> Si Substrates

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ABSTRACT

Raytheon has demonstrated 0.25µm GaN MISHEMTs fabricated on 200mm diameter, 725µm thick, high resistance <111> Si substrates. The GaN epitaxial layers were grown by metal organic chemical vapor deposition (MOCVD), by IQE, the leading commercial GaN epi vendor. The wafers display low wafer bow (≤23µm) and excellent mobility (1,600 $cm^2/V*s$). The wafers were fabricated at Novati Technologies, a commercial CMOS foundry, using a fully subtractive, Au-free, Si-like fabrication approach.

INTRODUCTION

Over the last decade gallium nitride (GaN) has garnered considerable interest for use in power electronics and high power density RF applications. The use of large feature (≥1µm gate, ≥10 µm source/drain gap) horizontal GaN HEMT transistors in switching applications is projected to be attractive for drain voltages up to ~650V.

In the RF application space, MMICs fabricated from deep submicron GaN HEMTs (≤0.25µm gate, ≤3 µm source/drain gap) have demonstrated power amplifiers (PAs) and low noise amplifiers (LNAs) with excellent characteristics at frequencies ranging from S-band to W-band and beyond. In general the GaN PAs exhibit gain and efficiencies equivalent to GaAs PAs at ~5X the power density. Meanwhile, GaN based LNAs demonstrate excellent noise figures, but with much higher linearity and survivability than their GaAs based counterparts. Finally, it should be noted that the device cross sections developed for RF applications could be adapted to low voltage, high frequency power switching applications and enable the use of smaller transformers.

As GaN device technology matures and proliferates into commercial and defense markets, cost reduction efforts will become increasingly more important. To that end, manufacturing GaN devices in a Si foundry with high yield subtractive processes, large diameter wafers, and a (Moore's law based) culture of rapid development seems like a natural evolutionary path for the technology. This is particularly true for medium power applications suitable for fabrication on 200mm Si substrates where the enhanced thermal conductivity of not yet available 200mm semi-insulating SiC substrates is not needed.

Building on our previous GaN on Si work[1,2,3,4], Raytheon designed a deep submicron, Au-free subtractively processed device cross section and released the mask at Novati, its partner Si foundry, in 2013. This coplanar waveguide (CPW) 0.25µm process cross section utilized an ALD high k gate dielectric to reduce gate leakage, MIM capacitors, thin film resistors, and a three metal Cu interconnects.

RESULTS AND DISCUSSION

In order to minimize gate leakage without negatively impacting critical RF device characteristics a charge balance model was used to design Schottky layer thickness in conjunction with the gate dielectric stack. This was done so that the overall gate capacitance, I_{DSS}, I_{MAX}, and V_T were similar to typical microwave GaN HEMT processes.

The material was grown by the commercial epi vendor, IQE on 200mm diameter, 725µm thick, high resistance <111> Si substrates. The material had excellent mobility (1,600 $cm^2/V*s$) and critically for device fabrication tools in a 200 mm Si foundry, very low wafer bow (≤23µm) as shown in figure 1.

The processing for this demonstration was done entirely in Novati's 200 & 300mm Si foundry, in a subtractive manner using Au-free processes. More importantly, this was done at Novati's foundry without contaminating or otherwise adversely affecting a diverse array of background Si based products. A post ohmic photograph of a 200mm GaN on Si wafer in process inside the Si foundry is shown in figure 2. Ohmic contact resistances of ~0.4-0.5 ohm-mm have

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initially been achieved without ohmic contact optimization experimentation. The transistor IV characteristics we achieved late last year is shown in figure 3. Since then, we have continued front end optimization experiments and expect the transistor characteristics to continue to improve as the process matures.

Additionally, with the expectation of completing a MMIC demonstration, we have begun integrating the copper back end of line (BEOL) and passive components. As shown in figure 4 we have made progress towards demonstrating an integrated damascene copper BEOL through experiments executed on both Si test wafers and full flow GaN on Si wafers. Finally, with regards to passive components integrated within the Cu BEOL, we completed initial capacitor and TaN resistor integration experiments. A cross section of TaN etched in Novati's foundry is shown in Figure 5.

CONCLUSIONS

Substantial progress had been made towards a Au-free 0.25µm gate GaN on Si MMIC foundry process fabricated fully subtractively in a 200mm Si foundry and integrated with a copper damascene back end.

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IQE Run No.	200mm Si Wafer Bow after GaN Epi (µm)
38-gos-164	-19.6
38-gos-211	-2.6
38-gos-216	2.4
38-gos-218	17.6
38-gos-221	-22.5
38-gos-221	-19.5
38-gos-221	-20.9
38-gos-225	7.8
38-gos-225	20.5
38-gos-225	19.0

Figure 1. <111> Si wafer bow after GaN on Si epitaxial growth. These wafer bow characteristics are well below the wafer bow limitations of 193nm lithography tools.

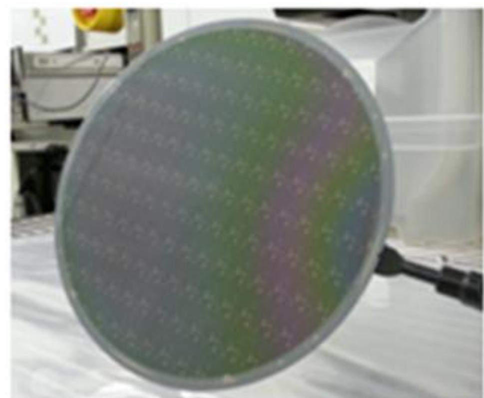

Figure 2. Picture of in process 200mm GaN on Si wafer in Novati's Si Foundry.

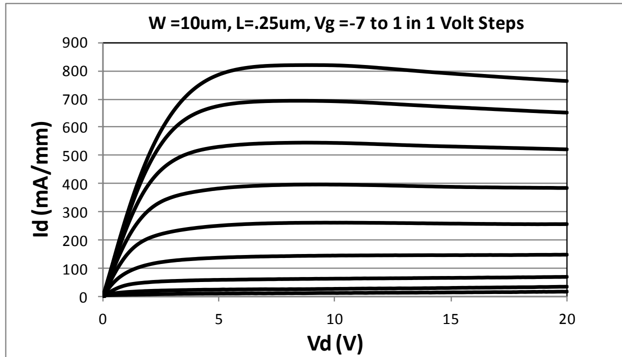

Figure 3. Transistor I-V characteristics for a Au-free, GaN MISHEMT fabricated on a 200 mm Si substrate.

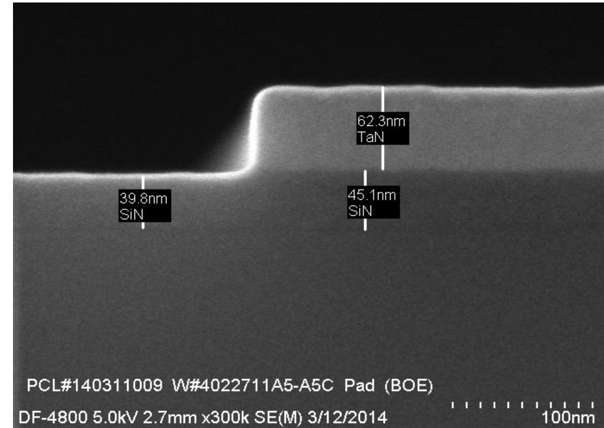

Figure 5. Micrograph cross section of etched TaN.

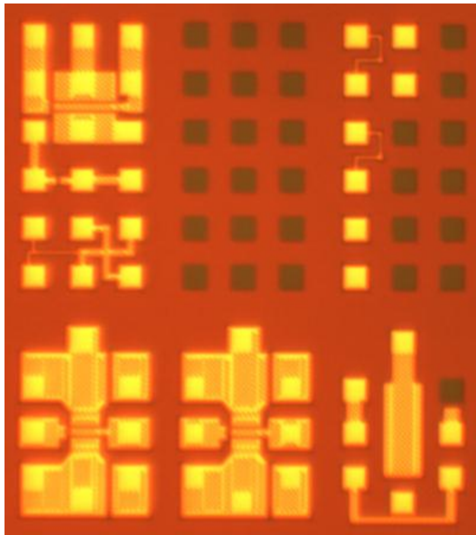

Figure 4. Microscope picture of PCM test structures post metal 1 copper CMP on a short loop development wafer.