The DARPA Diverse Accessible Heterogeneous Integration (DAHI) Program: Status and Future Directions

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***Abstract* — The DARPA Diverse Accessible Heterogeneous Integration (DAHI) program is developing transistor-scale heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices, as well as other emerging materials and devices, with high-density silicon CMOS technology. This technology is currently enabling RF/mixed signal circuits with revolutionary performance. For example, InP HBT + CMOS technology is being utilized in advanced DACs and ADCs with CMOS-enabled calibration and self-healing techniques for correcting static and dynamic errors in situ. Such CMOS-enabled self-healing techniques are expected to more generally enable improved CS-based circuit performance and yield in the presence of process and environmental variability, as well as aging. DAHI is also expected to enable the integration of high power CS devices with silicon-based linearization techniques to realize highly power efficient transmitters. By enabling this heterogeneous integration capability, DAHI seeks to establish a new paradigm for microsystems designers to utilize a diverse array of materials and device technologies on a common silicon-based platform.**

The compound semiconductor (CS) electronics industry has a long history of driving advancements in RF/mixed signal systems. A number of major RF/mixed signal achievements, including large-scale phased arrays [1], satellite communications [1], commercial mobile telephones [2], and solid-state RF power electronics [3] have been made possible using CS materials such as GaAs, InP, and GaN. The success of CS materials in these systems is due in large part to the many superior properties of these materials relative to silicon. For example, high electron mobility and peak velocity of InP-based material systems have resulted in transistors with f_{max} above 1THz [1][4] as well as ultra-high-speed mixed-signal circuits (see, for example, [5]). The wide energy bandgap of GaN has enabled large voltage swings as well as high breakdown voltage RF power devices [6]. Excellent thermal conductivity of SiC also makes tens of kilowatt-level power switches possible [7]. Additionally, on-chip high-Q micro-electromechanical resonators and switches in various materials, such as AlN, have been demonstrated that potentially can be used for clock references and frequency selective filters [8].

However, despite the advantages of CS materials, Si CMOS-based technologies have increasingly been employed in high-performance RF/mixed signal systems. These technologies have leveraged the enormous investments in digital CMOS device scaling and process development to achieve tremendous levels of complexity and integration, while also demonstrating far higher levels of yield and manufacturability than any CS technology. Additionally, scaling has driven device speeds of RF CMOS [9] and SiGe HBTs [10] into the multi-100 GHz regime, albeit at the expense of breakdown voltage. The integration density of Si-based technologies has enabled novel on-chip digital correction and linearization techniques (for example, [11]), producing excellent RF and mixed-signal circuit performance despite the limitations of silicon's material properties.

Such correction techniques have the potential to produce dramatic RF and mixed-signal performance improvements in CS electronics as well; however, CS technologies lack the integration density and yield to implement these circuit concepts. Given these trends, it is our view that the future of high-performance RF and mixed-signal electronics lies in the integration of compound semiconductors with silicon technology in a way that will allow the advantages of the two technology types to be optimally combined.

As an example of the potential benefits of heterogeneous integration, consider the plot of Johnson figure of merit (product of transistor cutoff frequency and breakdown voltage) [12] versus integrated circuit complexity (as measured by transistor count) for several semiconductor material and device types, as shown in Figure 1. Si CMOS is by far the superior technology in terms of integration complexity, exceeding the most advanced CS material (InP) by over five orders of magnitude. However, its Johnson figure of merit is exceeded by several CS device types by an order of magnitude. Nitride-based semiconductor devices (represented by GaN in Figure 1) possess the highest Johnson figure of merit of currently utilized semiconductor materials; however, nitrides have only

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small-scale integration complexity to date. CS materials such as GaN and InP would benefit greatly from leveraging novel silicon-enabled circuit or system architectures to enhance the performance of advanced CS-based RF/mixed signal circuits.

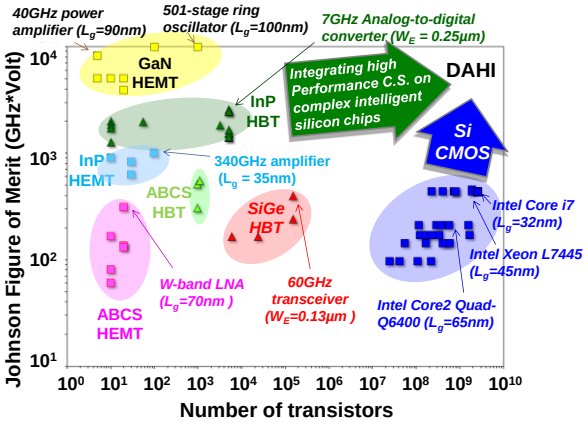

Figure 1. Plot of Johnson Figure of Merit (product of transistor cutoff frequency and breakdown voltage) vs. Integration Complexity (number of transistors per circuit) classified by a variety of material and device technologies.

Figure 2 and Table 1 illustrates the potential impact of heterogeneous integration in RF/mixed signal systems, using a representative transceiver as an example. Essentially all major components in a typical transceiver can potentially benefit from the reduced parasitics of heterogeneous integration, utilizing the benefits of high-performance CS materials with the control and calibration capabilities of Si CMOS.

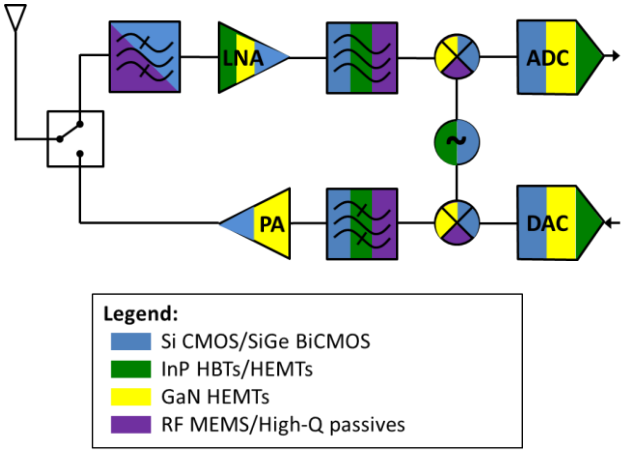

Figure 2. Diagram of a representative transceiver illustrating the preferred set of device technologies for optimal performance of each transceiver component.

Table 1 – Representative transceiver components and their heterogeneous device selections for optimal performance

Component	Heterogeneous Device Selection
Low-noise amplifier	InP HBTs for low noise; GaN for survivability; Si CMOS for control and reconfigurability
Pre-select filter	RF MEMS for high-Q filtering; Si CMOS for control
Tunable filter	InP HBTs for op-amps with high gain-bandwidth product; Si CMOS for programmability
Mixer	GaN HEMT for Gilbert cell high-voltage swing; RF MEMS for high-Q; Si CMOS for control
ADC	InP HBTs for high-speed track-and-hold; Si CMOS for ADC interleaving
Local oscillator	InP HBTs; High-Q MEMS; Si CMOS
DAC	InP HBTs for high-speed current switching and deglitching; Si CMOS for static and dynamic error correction
Power amplifier	GaN for high power density, speed, and thermal performance; Si CMOS for control and linearization

Heterogeneous integration of compound semiconductors with silicon has been explored in past decades [13], but its main practical implementation today is through the use of multi-chip modules or similar assembly techniques. Multi-chip module techniques have been prevalent in various microwave/millimeter-wave RF systems, but performance for high-speed/bandwidth mixed-signal systems has been limited by I/O parasitic effects between chips in such modules and by device and interconnect variability issues. Many of the limitations (including I/O parasitics and phase mismatch) of multi-chip module approaches to heterogeneous integration are governed by the length of separation between CS and Si CMOS devices, and as such, the reduction of this separation is expected to yield dramatic improvements in performance of heterogeneous integrated circuits.

To that end, the U.S. Defense Advanced Research Projects Agency (DARPA) Diverse Accessible Heterogeneous Integration (DAHI) program is developing transistor-scale heterogeneous integration processes to **intimately** combine advanced compound semiconductor (CS) devices, as well as other emerging materials and devices, with high-density silicon CMOS technology. The ultimate goal of DAHI is to establish a manufacturable, accessible foundry technology for the monolithic heterogeneous co-integration of diverse (e.g., electronic, photonic, MEMS) devices, and complex silicon-enabled architectures, on a common substrate platform for defense and commercial users. The DAHI transistor-level heterogeneous integration approach must overcome a number of difficult technical challenges associated with integration process technology (accurate device-level placement, robust heterogeneous interfaces, dense heterogeneous interconnects, thermal management), manufacturing (transfer of integration

technology to state-of-the-art foundries, heterogeneous process yield enhancement, process design kit development, compatibility with computer-aided design tools), and design innovation (innovative circuit design methodologies and architectures for heterogeneous circuits). If this vision can be achieved with high yield and at reasonable cost, this revolutionary technology will allow circuits in which the optimum device is chosen for each specific function within integrated microsystems encompassing RF/mixed signal, photonics, and MEMS technology. This capability will not only have significant impacts on the performance of both military and commercial microsystems, but it also represents a new paradigm for the CS electronics community.

II. Program Overview

The DAHI program is composed of several thrusts which are developing the integration technologies, design innovations, and manufacturing technologies and expertise which will be required to realize the DAHI vision. One element of DAHI, the Compound Semiconductor Materials on Silicon (COSMOS) thrust, has demonstrated three different approaches (shown in Figure 3) to achieving InP BiCMOS integrated circuit technology featuring InP HBTs and deep submicron Si CMOS [14][15][16] for RF and mixed signal circuits.

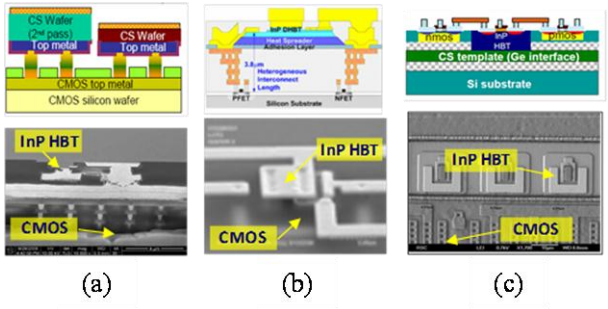

Figure 3. Heterogeneous integration processes being pursued in the DAHI/COSMOS thrust, (a) micrometer scale assembly, (b) epitaxial layer printing, and (c) monolithic epitaxial growth using a multi-layered lattice-engineered substrate.

DAHI/COSMOS performers have demonstrated complex heterogeneously integrated mixed-signal circuit designs, including digital-to-analog converters (DACs) with unprecedented SFDR performance in the GHz output frequency regime [17]. These DACs are utilizing a number of advanced calibration and self-healing techniques that are enabled by the heterogeneous integration of deep submicron Si CMOS with high-speed InP HBTs. Due to the required circuit complexity, these techniques would not be possible in a DAC implemented in a purely InP-based technology. However, the InP HBTs provide higher speed, higher breakdown voltage, and intrinsically better transistor matching than could be accomplished with a purely CMOS-based DAC. DAHI/COSMOS is presently developing advanced ADC designs with revolutionary performance in the InP BiCMOS technology. DAHI performers have also demonstrated the world's first GaN + CMOS RF amplifier using monolithic heterogeneous integration of GaN HEMTs with Si pMOS gate bias control [18].

DAHI has also initiated an InP BiCMOS multi-project wafer (MPW) activity based on the HRL Laboratories DAHI/COSMOS technology using 90nm CMOS and 0.25µm InP HBTs. In this effort, InP BiCMOS technology is being utilized by a number of external expert circuit design teams.

Recent measurements of fabricated COSMOS MPW designs have illustrated the potential for high-performance heterogeneously integrated mixed signal circuits. A team at the University of California, San Diego recently demonstrated a 30GSPS track-and-hold amplifier on the InP BiCMOS platform [19]. Differential output spectra with 1GHz and 31GHz inputs are shown in Figure 4. This InP track-and-hold amplifier on InP BiCMOS platform represents a key building block for interleaved ADCs, enabling complex interleaving using advanced Si CMOS for high-bandwidth, high-resolution performance.

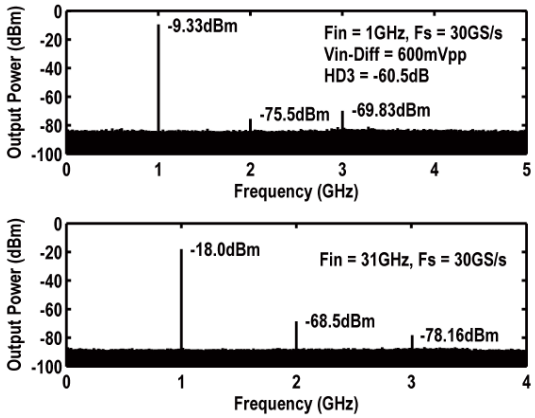

Figure 4. Differential output spectra for InP BiCMOS T/H amplifier (from [19], used with permission)

An additional circuit design recently fabricated through the DAHI/COSMOS MPW effort is a four-stage W-band low-noise amplifier (LNA), designed by a team from the Air Force Research Laboratory [20]. Measured results indicate a noise figure as low as 5.7dB at 92GHz (NF < 7.2dB across 75-100GHz band), peak gain fo 27.7dB (gain > 20dB across 75-100GHz band), and power dissipation of 19.2mW across 75-100GHz band. Plots of gain and noise figure versus frequency are shown in Figure 5. This device demonstrated superior noise figure, gain-bandwidth product, and power dissipation compared to SiGe BiCMOS W-band LNAs.

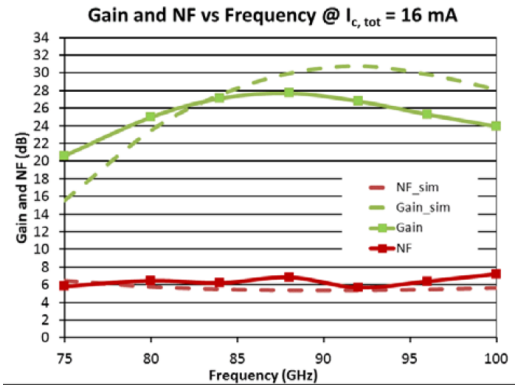

Figure 5. Plot of gain and noise figure versus frequency for InP BiCMOS W-band LNA (from [20], used with permission).

Recently, a new DAHI Foundry Technology thrust was initiated [21] to advance the diversity of heterogeneous device and materials available in a silicon-based platform and make this technology available to the greater DoD and commercial microsystems design community through the establishment of an accessible, manufacturable foundry offering for device-level heterogeneous integration. This foundry will seek to include a wider array of materials and devices (including, GaN and MEMS technologies) with complex silicon-enabled (e.g. CMOS) architectures and thermal management structures on a common silicon substrate platform. The goal of the DAHI Foundry Technology thrust is to develop a mature, reliable heterogeneous integration technology in a cost-effective foundry.

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REFERENCES

[1] E. D. Cohen. "The MIMIC Program: A Retrospective", *IEEE Microw. Mag.,* pp. 77-88, June 2012.

[2] L. Wirbel, "GaAs RF chips fit for cellular markets," *Electron. Eng. Times*, p. 54, Apr. 1994.

[3] Mishra, U.K.; Shen, L.; Kazior, T.E.; Yi-Feng Wu, "GaN-Based RF Power Devices and Amplifiers," *Proc. of the IEEE*, vol.96, no.2, pp.287-305, 2008.

[4] R. Lai, et al, "Fabrication of InP HEMT Devices with Extremely High Fmax", 2008 International Conference on InP and Related Materials, Versailles, France.

[5] S.E. Turner, D.E. Kotecki, "Direct Digital Synthesizer With Sine-Weighted DAC at 32-GHz Clock Frequency in InP DHBT Technology," *IEEE J. Solid-State Circuits*, Vol. 41, No. 10, 2006, pp. 2284-90.

[6] Y.F. Wu; M. Moore, A. Saxler, T. Wisler, P. Parikh, "40W/mm Double Field Plated GaN HEMTs," *64th Device Research Conference*, 2006, pp. 151-152.

[7] Cree's SiC Schottky Diode Chip CPW2-1200-S050B.

[8] Crespin, E. R.; Olsson, R. H.; Wojciechowski, K. E.; Branch, D. W.; Clews, P.; Hurley, R.; Gutierrez, J.; , "Fully integrated switchable filter banks," 2012 IEEE MTT-S International, pp.1-3, 17-22 June 2012.

[9] C.-H. Jan, et al, "A 45nm Low Power System-On-Chip Technology with Dual Gate (Logic and I/O) High-k/Metal Gate Strained Silicon Transistors," *IEDM Tech. Dig*., pp. 637-40, 2008.

[10] Chevalier, P.; et al. "Towards THz SiGe HBTs," *IEEE BCTM Digest*, pp.57-65, 2011.

[11] Adrian Tang, et al. , "A Low Overhead Self-Healing Embedded System for Ensuring High Performance Yield and Long- Term Sustainability of a 60GHz 4Gbps Radio-on-a-Chip", *2012 ISSCC Digest*, 2012.

[12] E.O. Johnson, "Physical limitations on frequency and power parameters of transistors", *RCA Review*, vol. 26, pp. 163-177, 1965.

[13] Fang, S. F. and Adomi, K. and Iyer, S. and Morkoç, H. and Zabel, H. and Choi, C. and Otsuka, N., "Gallium arsenide and other compound semiconductors on silicon" *J. Appl. Phys.*, **68**, R31-R58 (1990).

[14] A. Gutierrez-Aitken, et al., "Advanced heterogeneous integration of InP HBT and CMOS Si technologies for high performance mixed signal applications," *IEEE Microwave Symposium Tech. Dig.*, pp. 1109-1112, 2009.

[15] T.E. Kazior, et al., "A high performance differential amplifier through the direct monolithic integration of InP HBTs and Si CMOS on silicon substrates," *IEEE Microwave Symposium Tech. Dig*., pp. 1113-1116, 2009.

[16] J.C. Li, et al., "Heterogeneous wafer-scale integration of 250nm, 300GHz InP DHBTs with a 130nm RF-CMOS technology," *IEDM Tech. Dig*., pp. 944-946, 2008.

[17] Oyama, B., et al. "InP HBT/Si CMOS-Based 13-Bit 1.33Gsps Digital-to-Analog Converter with >70 dB SFDR," *2012 CSICS Tech. Dig.*, pp.1-4, 2012.

[18] W. E. Hoke, et al. "Monolithic integration of silicon CMOS and GaN transistors in a current mirror circuit", *J. Vac. Sci. Tech. B 30(2)*, pp. 02B101-1-6, 2012.

[19] T.D. Gathman, K.N. Madsen, J.C. Li, T.C. Oh, J.F. Buckwalter. "A 30GS/s Double-Switching Track-and-Hold Amplifier with 19dBm IIP3 in an InP BiCMOS Technology", *2014 ISSCC Tech. Digest*, 2014.

[20] P. Watson, A. Mattamana, R. Gilbert, Y. Royter, M. Lau, I. Valles, J. Li. "A Wide-Bandwidth W-band LNA in InP/Si BiCMOS Technology", *2014 IMS Digest.*, 2014.

[21] DARPA DAHI Foundry Technology thrust description. http://www.darpa.mil/Our_Work/MTO/Programs/DAHI/DAHI_Foundry_Technology.asp.