Low-Voltage and Low-Cost ZnO based Ultra-Thin-Film Transistors

Gem Shoute*[1], Alex Ma[1], Amir Afshar[2], Ken Cadien[2] and Douglas Barlage[1]

[1]Department of Electrical and Computer Engineering, University of Alberta, Edmonton, Alberta, Canada T6G 2V4

[2]Department of Chemical and Materials Engineering, University of Alberta, Edmonton, Alberta, Canada T6G 2V4

*EMAIL: shoute@ualberta.ca

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Abstract

We highlight the transfer characteristics of an extremely thin high-k-ZnO TFT (<100 nm), and methods to control the material notwithstanding less than ideal material properties such as relatively high doping concentration ($>10^{18}$), amorphous substrate, and general issues arising from ultra-thin films. We show a successful geometrical approach by extending gate-to-source overlaps over the active film which results in improved device characteristics including better on/off ratio (10^5 times improvement), an almost one order improvement in subthreshold swing, a more favourable threshold voltage and reduced DIBL effect. Further investigations were also made for defect densities and its influence on key junction properties.

INTRODUCTION

The transfer characteristics of a low voltage and easily manufacturable novel zinc oxide (ZnO) extremely thin film transistor (TFT) are investigated. The active and insulating films are fabricated on a less than ideal surface using atomic layer deposition (ALD) without exceeding 130 ºC, making this process compatible with a wide variety of applications. They are considered "ultra" thin because their maximum vertical height does not exceed 100 nm from the top-gate to the source/drain-bottom. Furthermore, the ZnO film exhibits a relatively high doping concentration ($>10^{18}$ cm^{-3}) which allows for the scaling of the drain-gate spacing with a manageable series resistance [1]. In this study, we examine the electrical behaviour of two different top-gate overlaps: the essential switching metrics, threshold voltage V_{TH}, current on/off ratio ($I_{ON/OFF}$), subthreshold slope (SS), and drain induced barrier lowering (DIBL) are presented and contrasted. The performance of the device, although largely dependent on the quality of the material and interfaces, at such ultra-thin dimensions, we show that modifying some key geometrical dimensions can respectably compensate of some deficiencies. This is especially important for the emerging source-gated transistors (SGT) devices that rely on the formation of Schottky barriers with thin, poly-crystalline to amorphous films exhibiting inhomogeneous surfaces [1,2].

This work examines the large-signal effects of sizeable overlaps of the gate over the source regions of a top-gated staggered high-κ-oxide/ZnO TFT. The extremely small thickness (<100nm) allows for easy integration into numerous emerging applications, although there are challenges in controlling its behaviour. We aim to improve the electrical performance of these ultra-thin devices architecturally with minimal dependence on the material properties.

What we present and elaborate on are: better transfer characteristics for larger overlaps; major improvement in $I_{ON/OFF}$, SS and DIBL. Furthermore, the source-gated architecture gives rise to a "reverse" DIBL effect, which is dictated by the modulation of the built-in potential at the source rectifying junction. All measurements were taken using the Keithley 4200 SCS.

METHODS AND MANUFACTURING

The manufacturing goal for these ultra-thin devices was to simplify the process for extremely low costs while still maintaining respectable device characteristics. The critical paramerter here is the gate-to-source overlap. However, the gate-to-drain disstance can also be scaled to manipulate breakdown behaviour of the device.

We first sputtered 12 nm of titanium tungsten (TiW) metal for the source and drain on amorphous silicon dioxide/silicon wafer. The active layer ZnO is a thermal ALD film grown at 130 ºC, as is the high-κ dielectric gate oxide deposited *in-situ* with thicknesses of 20 nm and 5 nm, respectively. An aluminum top-gate TFT was constructed, with a gate-to-source and drain overlap of L_{OV} 10 µm, with L_{Gate} of 22 µm (designated D1) and 20 µm with L_{Gate} of 42 µm (D2). Common dimensions are W = 10 µm, and L_{SD} = 2 µm, with a maximum device height of H = 100 nm. The top-down and cross-sectional view with relevant dimensions of the final device are shown in Fig. 1.

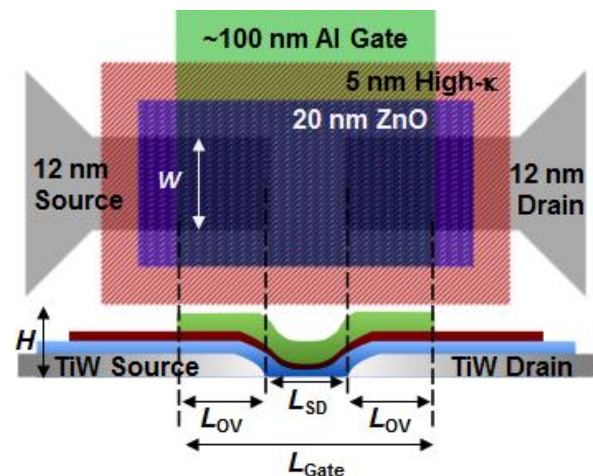

Fig. 1: Top-down and cross-section view of the ZnO TFT device; common dimensions include L_{SD} = 10 µm, W = 10 µm, H = 100 nm. The critical parameter in this study being L_{OV}.

RESULTS AND DISCUSSION

Fig. 2(a) and (b) shows the transfer characteristics (IV_{GS}) of gate overlaps 10 μm and 20 μm, with varying drain-to-source voltage V_{DS}. The inset within each figure shows the $\sqrt{I_{DS}}$ dependence on the gate voltage, which determines the threshold voltage V_{TH} of each device through a linear fit which intercepts at the V_{TH} of the device. D1's behaviour is characteristic of a depletion-mode transistor, with a negative threshold voltage of -2.3 V; and, while D2's threshold voltage also exhibits a small negative threshold of -0.2 V, this can be rectified by either increasing the oxide's thickness or improving the quality of the oxide-semiconductor interface.

The SS and $I_{ON/OFF}$ are also much improved with an increased overlap. SS was determined using (1).

$$SS = \frac{\partial V_{GS}}{\partial \log_{10}\left(I_{DS}\right)} \tag{1}$$

D1 was evaluated at $I_{ON/OFF\text{-}D1} = 10^2$ and $SS_{D1} = 1392$ mV/dec, while D2 revealed that $I_{ON/OFF\text{-}D2} = 10^7$ and $SS_{D2} = 183$ mV/dec as shown in Fig. 3(a) and (b), respectively. The vastly improved subthreshold swing suggests that a larger overlap is much suitable for switching applications.

The SS of D2 is comparable with those reported for indium-gallium-zinc-oxide (IGZO) based TFTs used in current display technology that do not employ an additional passivation layer and is among the best for ZnO TFTs [3]. Many design strategies for reducing SS for ZnO-based transistors have succeeded, some of which include the "double-gate" architecture, which sees a gate situated both at the top and the bottom of the device, with the gate oxide directly below and above it and the active channel film sandwiched between the two [4]. The addition of SiO_2 buffer layers on metal-oxide TFTs to reduce defects contributing to poor subthreshold behaviour have resulted in superior SS, reaching values of less than 100 mV/dec [5]. However, due to the additional device layer required and the associated increase in process complexity, these strategies remain incompatible with the aims of this study—to minimize the thickness of the full TFT to enable itself as a flexible electronic device.

TiW was specifically chosen as the metal for especially the source, and also the drain electrode because recent reports have demonstrated the formation of Schottky barriers when interfaced with ZnO [6]. In both of the aforementioned design strategies, the mechanism in which the switching behaviour is improved is through the reduction of defects and full-depletion of excess carriers. The lower SS in the device D2 discussed here can be attributed to the depletion of carriers due to the nature of Schottky barrier ideally formed at the source and drain region. The enhanced performance of D2 in comparison to D1 is likely an effect of better Schottky barrier formation due to larger exposed

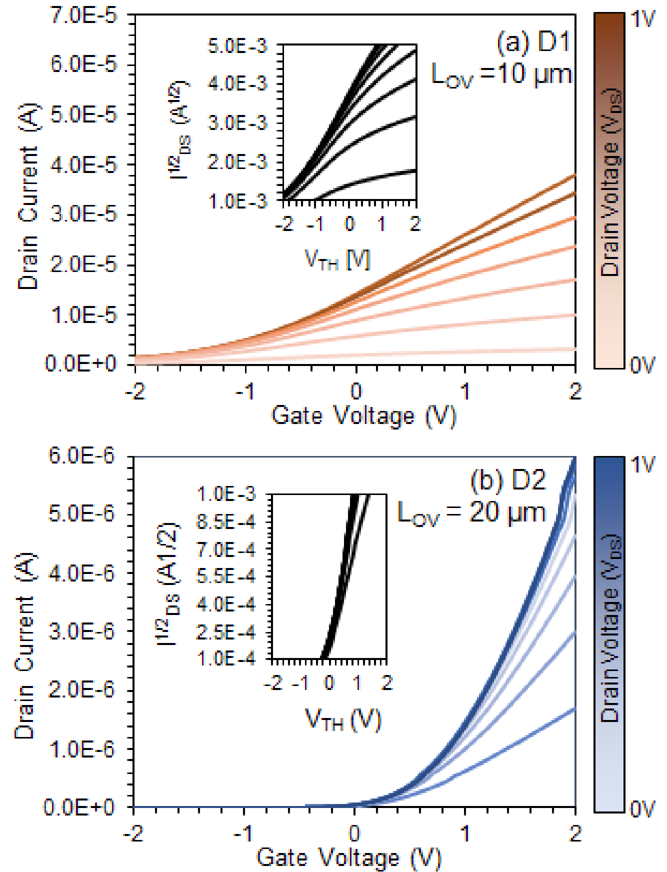

Fig. 2: Transfer characteristics of device with the drain voltage varying from 0 V to 1 V for (a) D1 with L_{OV} = 10 μm; and, (b) D2 with L_{OV} = 20 μm. The inset shows the device's threshold voltage V_{TH}.

surface area. This further implies that the ZnO layer may suffer from surface and film in homogeneities. This is especially problematic for low temperature processes but it can eventually be circumvented by extending the overlaps to increase exposure of the active film to the Schottky metal.

The superior switching qualities were further investigated. In addition to transfer and SS characteristics, the drain-induced barrier lowering (DIBL) using (2) was also closely examined for both devices.

$$\text{DIBL}(V_{DS}) = -\frac{V_{\text{TH}}^{DS} - V_{\text{TH}}^{low}}{V_{DS} - V_{DS}^{low}} \tag{2}$$

The comparison between D1 and D2 are shown in Fig. 3(c) and (d). It is apparent that D2's larger overlap provides a significant improvement. Whereas the DIBL evaluated for D1 was a 1.4 V/V, D2 exhibited a $DIBL_{D2}$ of 0.06 V/V.

It is interesting to note that, unlike the transfer curve of D1, in D2, before a certain gate voltage, we can observe that the output current I_{DS} is lower for higher V_{DS}, until it reaches a "crossing point" where after it behaves as one would expect given the DIBL effect. For D2, the V_{GS} where the

crossing point V_{CROSS} is observed is -0.6V (Fig. 3(b), captioned marker).

becomes more susceptible to trap-assisted conduction induced by the gate voltage.

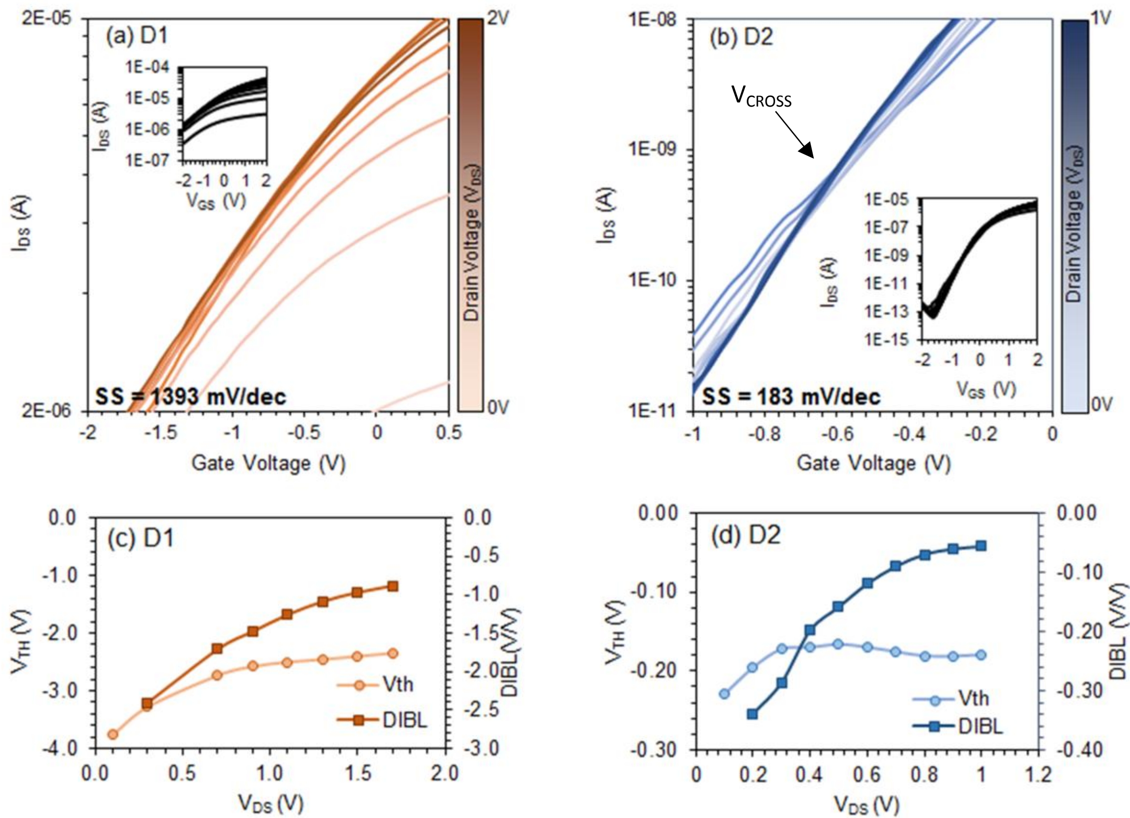

Fig. 3: Subthreshold swing SS and DIBL observed in the transfer characteristics for (a) D1 with L_{OV} = 10 µm and (b) D2 with L_{OV} = 20 µm and V_{CROSS} indicating the voltage where the DIBL reverses, the insets shows the full transfer curve in a linear-log scale; (c) the variance of threshold voltage V_{TH} and DIBL on drain voltage V_{DS} for D1 and (d) D2.

It is worth noting that as the V_{DS} is increased, the V_{TH} for both devices also increase. This is the opposite of what would be expected given the DIBL effect. The mechanism which occurs for such an effect to take place is directly related to the behavior of the Schottky barrier that is formed at the source which is modulated by V_{GS}. The source barrier is reversed biased at a positive V_{GS}, which increases the built-in potential at the source. However, increasing V_{GS} also reduces the depletion width at the source due the accumulation of n-type carriers underneath the gate oxide through the injection of electrons from the source metal. The barrier continues to increase with V_{GS} until the pinch-off voltage. In this condition, the accumulation layer and depletion width no longer changes. The saturation of the DIBL effect shown in Fig. 3(a) and (b) occurs when the V_{GS} no longer has influence on the source as it is counteracted by V_{DS}.

In the context of SGTs, the dependency of DIBL on the drain voltage is an indication of the number of trap states existing at the Schottky interface. The junction barrier deviates from the ideal $\phi_B = \phi_M - \chi_s$ because the number of traps causes surface inhomogeneities. As a result, the barrier height is lowered leading to insufficient charge control and it

To determine whether the disparity in device performance between D1 and D2 is not related to any non-uniformities that may exist in within the 20 nm ZnO film, the density of interface traps (D_{it}) was evaluated using the conductance method (3).

$$D_{it} = \frac{2}{qA}\left(\frac{G_p}{\omega}\right)_{\max}\left(G_{p_{\max}}C_{ox}\right)^2 + \left(1 - \frac{C_{p-G_{p\max}}}{C_{ox}}\right)^2 \quad (3)$$

Where A is the gate area, G_{pmax} is the peak conductance, $(G_p/\omega)_{\max}$ is the normalized parallel conductance peak, the oxide capacitance is C_{ox} and $C_{p\text{-}Gpmax}$ is the capacitance at peak conductance.

The comparison between the two devices is shown in Fig. 4. The D_{it} of D1 is observed to be less than ten times greater than that of D2. Additionally, the energy level of the traps in D1 extends up to 0.7 eV further than in D1 from the conduction band edge E_C of ZnO. The limitations of the D_{it} conductance method, however, is that it is unable to discriminate between traps originating at the interface, and

traps existing within the dielectric itself, resulting in a artificially inflates D_{it}. Evidence suggesting this is that the difference in gate leakage is the same ratio as observed in devices' extracted D_{it} ($I_{leakage-D1}$ = 40 pA, $I_{leakage-D2}$ = 6 pA).

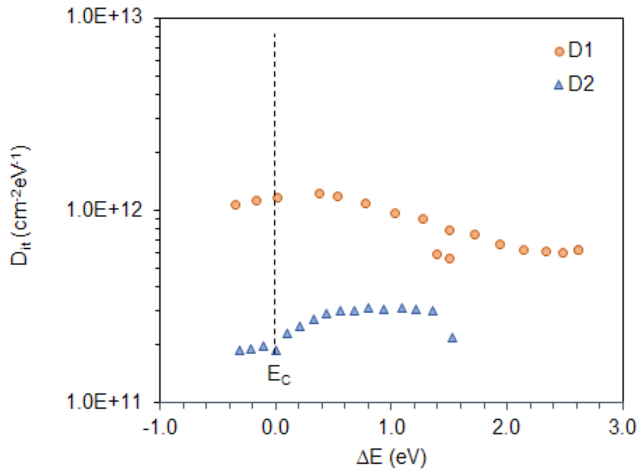

Fig. 4: Comparison of density of interface traps (DiT) of the device D1 and D2 and its energy level with respect to the ZnO conduction band edge E_C.

We do not see significant amount of non-uniformity in the film which suggests that the overlap does play a non-trivial role in the behavior output. The study conducted here further suggests that a "critical" gate-to-source overlap which vastly improves the device performance lies anywhere between 10 µm to 20 µm for thin films with doping concentrations of >10^{18} cm^{-3}.

CONCLUSIONS

We show that to better control the transfer characteristics of the low-voltage, low-cost and extremely thin device, extending overlaps and utilizing thin high-κ gate dielectrics on a ZnO-based ultra TFT can improve its switching performance substantially. The difference in performance provide us insights into the role of both the Schottky barrier situated at the source contact and the gate-insulator. For better control over the majority carriers of ZnO, the contribution of both the Schottky interface and gate insulator towards the depletion of thereof are crucial for more desirable TFT characteristics.

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ACRONYMS

TFT: Thin-film Transistor
ALD: Atomic Layer Deposition
SS: Subthreshold Swing
mV/dec: Millivolts per decade
DIBL: Drain Induced Barrier Lowering
V_{TH}^{DS} : Threshold voltage at V_{DS}
V_{TH}^{low} : Threshold voltage at drain voltage
V_{DS}^{low} : V_{DS} Low drain-voltage