Homogeneity Control of Powerelectronic Device Structures by Advanced In-situ Metrology

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Abstract

The impact of strain related homogeneity imperfections across the wafer during device growth and their correlation with wafer quality and device level properties were investigated by advanced in-situ metrology. We found a significant impact of the wafer curvature and the related temperature distribution across the wafer during MOVPE growth on the crystalline quality of the layer structure measured with XRD. These results were correlated with drastic changes of the leakage currents of GaN-HEMTs on Si(111) substrates.

INTRODUCTION

GaN-based devices grown on Si gain more and more interest in compound semiconductor industry. Light emitting diodes with similar performance as on sapphire can be grown on 8'' Si(111) [1]. Beyond optoelectronic applications, the use of III-Ns on Si for power-electronic applications, especially for low-cost power switches with high switching efficiencies, is of large interest. The low price, large diameter and simple processing as well as a good thermal and electrical conductivity of silicon substrates in contrast to electrically and thermally insulating sapphire and expensive SiC can lead to a substantial cost advantage. However, the significant III-N/Si misfit in thermal expansion coefficients which can lead to cracking during down-cooling of MOVPE grown layers in excess of 1 µm in thickness. Hence more elaborate layer structures are required to induce compensating compressive stress during epitaxial growth. For an overview on different strain engineering techniques see, e. g., ref. 2. The required compression during growth affects the wafer bow which can be beneficial for In-containing layers to be grown at lower and extremely uniform temperatures. However, it also limits the thickness of such GaN layers because silicon can undergo plastic deformation under high stresses [3].

AlInN is the most promising active layer material for high power FETs to induce high electron concentrations in the 2DEG [4-7] and enable low resistance devices or reduce the device area.

Here we investigate MOVPE grown GaN FET structures with an AlInN active layer on different types of Si substrates. These structures are analyzed by in-situ curvature, temperature, reflectance and ex-situ XRD measurements of the symmetric (0002) and in-plane ($10\bar{1}0$) reflections. In addition some samples were processed and electrically characterized.

EXPERIMENTAL

FET structures (Fig. I) were grown using an AIXTRON AIX 200/4 RF-S MOVPE system and standard precursors. On the Si substrate an AlN seeding and buffer layer followed by AlGaN and an iron doped GaN buffer were grown. The buffer is interrupted by two LT-AlN interlayers of ~ 10 nm in thickness for strain compensation. The active region consists of an undoped GaN layer followed by approx. 1 nm AlN and 5 nm AlInN with a nominal In concentration of 13 %.

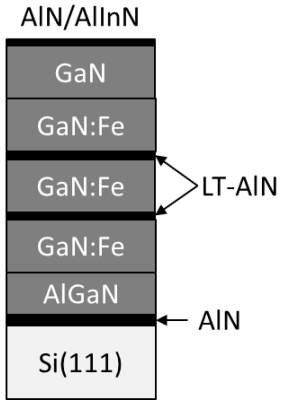

FIGURE I
FET STRUCTURE GROWN ON DIFFERENT SI(111) SUBSTRATES. THE TOTAL THICKNESS OF THE STACK IS 3.1µM.

While the buffer and undoped GaN and AlN spacer layers were all grown in a hydrogen atmosphere, the AlInN layer was grown in nitrogen ambient (for details on the growth of AlInN see ref. 8).

In-situ characterization of reflectivity, surface temperature, curvature and asphericity was performed using a LayTec EpiCurve® TT SP AR 3W with three different wavelengths for reflectivity measurements (405, 633, 950 nm) and a three spot curvature measurement system which enables the measurement of asphericity of the wafer.

Three different substrates for epitaxial growth were used: 500 µm thick highly resistive (R ≈ 10 MΩ cm) float zone (FZ) and highly As-doped (n-type, R < 0.01 Ω cm) Czochralski (CZ) Si substrates as well as a 275 µm thick highly As-doped CZ substrate (R < 0.01 Ω cm).

Nomarski microscopy and x-ray diffraction measurements of the (0002) and (10$\bar{1}$0) reflections were performed for ex-situ analysis. Additionally, for electric device characteristics some samples were processed.

RESULTS

To enable high-voltage operation a sufficient GaN buffer layer thickness is prerequisite for high breakdown field strength. The breakdown field strength for AlGaN / GaN based high-power FETs on Si has been reported to up to 150 V/µm or 1.5x10^6 V/cm [3]. In contrast to FETs on sapphire this is required because breakdown does not only occur laterally between the contacts but, due to the high conductivity and low breakdown field strength of Si, also vertically. For an FET operating up to 1500 V a 5 µm thick buffer at a contact distance of 10 µm is required when using a floating or insulated substrate. Even thicker buffer layers or substrate removal is required for higher voltages, the latter is reported to increase the breakdown field strength from 1x10^6 V/cm to 2.5x10^6 V/cm [9].

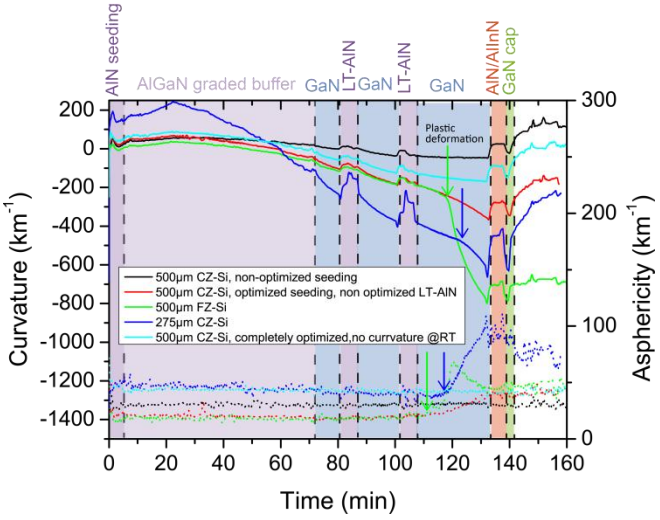

FIGURE II
TOP (SOLID):IN-SITU CURVATURE MEASUREMENTS OF AN FET STRUCTURE GROWN ON DIFFERENT SI SUBSTRATES; BOTTOM (DOTTED): ASPHERICITY DATA OF THE CURVATURE MEASUREMENTS .

Apart from a low dislocation density to maximize breakdown field strength, high voltage operation also requires thick GaN layers. Even for high frequency operation a thicker and highly insulating GaN buffer layer is beneficial to minimize high-frequency operation losses. These are always present because of the remaining conductivity of the Si substrate, which is expected to be lower on highly resistive FZ Si substrates but still high if compared to highly insulating GaN layers.

In our test we used a ~ 3.1 µm thick FET structure (Fig. I). With such a thickness in principal high voltage operation above 900 V should be possible. To achieve such a layer thickness just using graded AlGaN buffer layers is usually not sufficient to avoid cracking. We therefore apply additional AlN interlayers to increase compressive stress and avoid cracking. In situ data obtained during the growth of a FET structure on three different Si substrates (CZ and FZ and 500 as well as 275 µm thick) is shown in Figure 2. In particular the 500 µm thick FZ substrate undergoes plastic deformation at ~ 120 min of growth. This leads to a high curvature of ~ -700 km^{-1} after cool down to room temperature. When grown on on 500 µm thick CZ Si the remaining curvature yields ~ -200 km^{-1}. Also here some weak plastic deformation is visible in the increased negative slope at ~ 120 min of growth and more pronounced in asphericity data (Fig. II bottom). As can be expected a steeper curvature right from the start and a kink after 130 min of growth is observed for the 275 µm thick substrate. Investigating the asphericity data shows that for this sample plastic deformation starts before 120 min of growth and the curvature after cool down is below -200 km^{-1}. By carefully optimizing the thickness of the AlN interlayers inducing sufficient, but not too high compression to avoid cracking, we obtained a wafer with nearly zero curvature and asphericity after growth, which is ideally suited for processing.

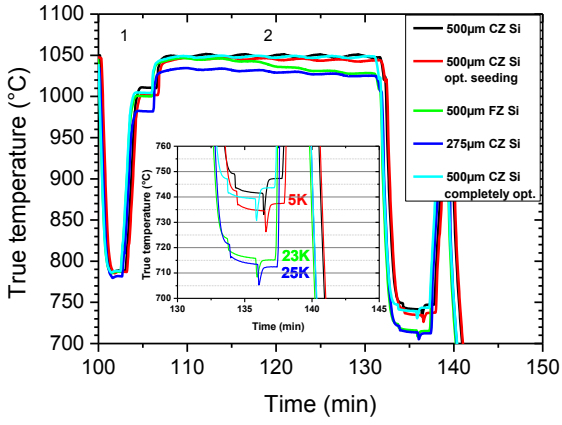

FIGURE III
IN-SITU DETERMINED TRUE TEMPERATURE MEASURED IN THE WAFER CENTER. THE PERIOD FROM THE SECOND LT-ALN LAYER (1), THE LAST GAN BUFFER (2) AND THE ALINN ACTIVE LAYER (INSET) IS SHOWN.

An optimized curvature is also important for device functionality. In AlInN the In concentration is very sensitive

to the growth temperature and inhomogeneities. A detailed look at in-situ temperature (Fig. III) reveals that already GaN growth is impacted by temperature changes originating in high bow values after strong plastic deformation or when having excessive bow due to the low substrate thickness (275 µm substrate). Only the temperature of the optimized sample remains stable during the growth of the last GaN layer. All other samples, which are plastically deformed, show a decrease in temperature between 3 to 18 K. A drastic reduction in growth temperature of 4.5 to 25 K is observed for AlInN when comparing the plastically deformed samples with the optimized sample on 500 µm CZ Si. Such temperature changes and with it gradients across the wafer lead to an increased In inhomogeneity [10] as shown in Fig. IV.

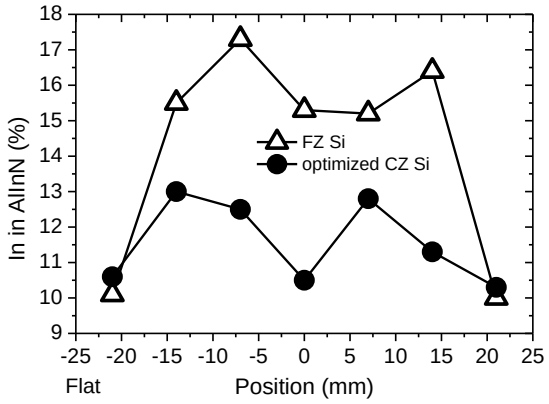

FIGURE IV
LINE SCAN OF THE ALINN CONTENT OF THE ACTIVE LAYER ACROSS THE WAFER AS DETERMINED BY XRD MEASUREMENTS. APART FROM SOME NONLINEARITY OF OUR GROWTH SYSTEM THE DEVIATION IN IN CONTENT IS MUCH MORE SIGNIFICANT FOR THE STRONGLY BOWED PLASTICALLY DEFORMED DEVICE STRUCTURE ON FZ SI. FOR THIS SAMPLE DIFFERENCE OF THE SURFACE TEMPERATURE IN THE WAFER CENTER IS ABOVE -20 K WHICH LEADS TO A MORE THAN 3 % INCREASE IN IN-CONTENT.

The difference in In-content of the AlInN layer has an impact on device performance. When comparing the sample on FZ Si and the optimized one we find a 1 to 2 orders of magnitude lower gate leakage and a better homogeneity in transconductance for the sample on CZ Si. For the sample on FZ Si it varies strongly for different positions across the wafer. We attribute this mostly to the differences in In-content of the AlInN layers.

TABLE I
LEAKAGE CURRENTS (AT U_{GS}=-2V) FOR THE FET GROWN ON FZ-SI AND THE OPTIMIZED ONE ON CZ-SI (MEASURED IN BETWEEN WAFER CENTER AND EDGE)

Si growth method	Gate leakage (A)	Source-Drain leakage (A)
Float zone	$1.5 \cdot 10^{-6}$	$1.8 \cdot 10^{-4}$
Czochralski	$1.1 \cdot 10^{-9}$	$1.3 \cdot 10^{-6}$

CONCLUSIONS

We have demonstrated the importance of avoiding plastic substrate deformation by strain control using precise in-situ wafer bow and temperature monitoring. These deformations lead to strong bow hampering device processing and also leading to cracks. In addition they also cause a significant inhomogeneity of ternary In-containing alloys which has a direct impact on device performance of FETs.

ACKNOWLEDGEMENTS

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