High Breakdown Voltage ZnO Thin Film Transistors Grown by Low Temperature Atomic Layer Deposition

Alex Ma, Mourad Benlamri, Amir Afshar, Gem Shoute, Kenneth Cadien, and Douglas Barlage

Department of Electrical and Computer Engineering
University of Alberta, Edmonton, Alberta, Canada
Email: alex.ma@ualberta.ca, Phone: 780-492-4081

Keywords: ZnO, thin film transistors, source-gated transistor, high-κ dielectric

Abstract

Low temperature atomic layer deposition processes (< 130°C) are employed for the fabrication of ZnO source-gated thin film transistors (SGTFTs) that utilize a TiW Schottky barrier source contact and a thin (~ 5 nm thick) high-κ gate dielectric (ZrO_2). The devices demonstrate good transistor characteristics with low operating voltages (< 2 V gate bias) and mobilities as high as 5 $cm^2V^{-1}s^{-1}$. High breakdown voltages exceeding 30 V for a gate-to-drain spacing of 9 µm were also observed by utilizing this unique device architecture.

INTRODUCTION

Zinc oxide (ZnO) thin film transistors (TFTs) are a promising technology for various electronic applications such as flat panel displays (FPDs) [1] and high frequency microwave devices [2] because of their good electrical characteristics. In particular, ZnO-based TFTs have demonstrated moderately high mobilities exceeding that of conventional hydrogenated amorphous silicon (a-Si:H) TFTs [3]. Moreover, their compatibility with low temperature processes and high transparency in visible light are highly attractive for next generation FPD technologies such as transparent and flexible electronics.

In this work, a novel device architecture based on the source-gated thin film transistor (SGTFT) architecture [4] is utilized with low temperature atomic layer deposition (ALD) films to fabricate top-gated ZnO TFTs with many distinctive and attractive properties. The ZnO SGTFT device reported herein employs a titanium tungsten (TiW) Schottky barrier contact for the source electrode, which leads to different device operating physics and unique device characteristics compared to the conventional TFT. A key feature of this device structure was the high breakdown voltages observed for the relatively small device dimensions. Based on our measurements, the ZnO SGTFT is a promising route for the manufacturing of high performance TFTs suitable for many applications beyond display technologies.

DEVICE FABRICATION

The top-gated ZnO SGTFTs were fabricated on an insulated silicon (Si/SiO_2) substrate. Firstly, 12 nm of TiW was deposited by sputtering and patterned with lift-off to form the Schottky bottom source contact. Thermal ALD was then used to grow the ZnO channel at 130°C with a thickness of 20 nm before it was etched with ferric chloride ($FeCl_3$) for mesa isolation. A 5 nm thick high-κ zirconium oxide (ZrO_2) thin film was utilized for the gate insulator layer, which was deposited by plasma-enhanced ALD at 100°C and then patterned with lift-off. Finally, a metal stack consisting of Al/Au (20 nm/60 nm) was sputtered at room temperature and patterned with lift-off to form the ohmic contacts for the top gate and drain electrodes. No post-deposition annealing was done so as to keep the processing temperature low enough to be compatible with inexpensive flexible substrates. A schematic cross-section image of the SGTFT is shown in Fig. 1. For this study, the device's width (W), source-to-drain distance (L_{SD}), and gate-to-source overlap (L_{SG}) were held constant while the gate-to-drain distance (L_{GD}) was changed to examine its effect on the transistor characteristics.

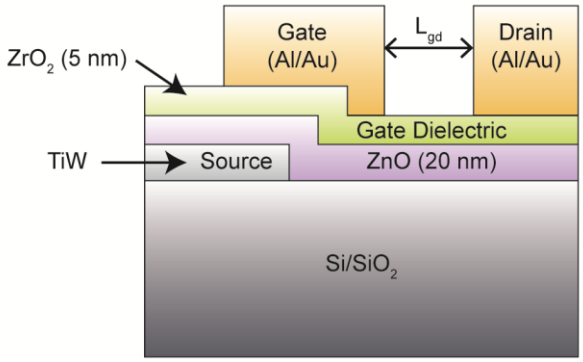

Fig. 1. Cross-section schematic image of the ZnO SGTFT.

MEASUREMENTS AND RESULTS

Fig. 2 shows the output characteristics of the ZnO SGTFTs. The W, L_{SG}, and L_{SD} of the measured devices were 50 µm, 15 µm, and 32 µm respectively; whereas, L_{GD} was varied from 9 µm to 30 µm. All of the devices were well-behaved and exhibit good transistor characteristics. The drain current (I_{DS}) during saturation reached on the order of 10^{-5} A for all of the devices, which is similar to other ALD ZnO TFTs [5], [6]. Although only L_{GD} was manipulated for this study, we observed a noticeable and

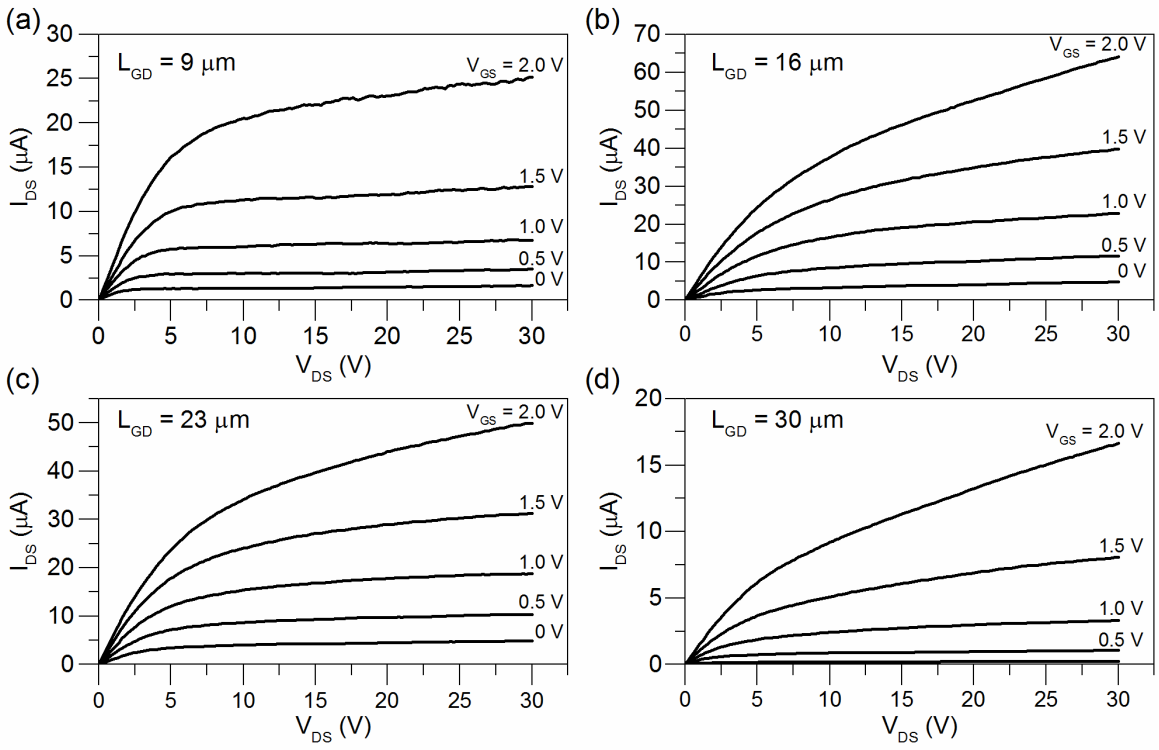

Fig. 2. Output Characteristics of the ZnO SGTFT with a gate-to-drain spacing of (a) 9 µm, (b) 16 µm, (c) 23 µm, and (d) 30 µm.

random variance in output characteristics between devices, which implies that processing inconsistencies and device non-uniformities impacted the device characteristics more than the dimensions of the device itself. For instance, it is evident that the device with L_{GD} = 9 µm displayed the highest output impedance of all the devices (which is seen by the flatness of the curves in the saturation regime). Particularly, the output characteristics of this device most closely resemble the curves expected of SGTFTs [4]. In the SGTFT, when the drain voltage (V_{DS}) is increased, the depletion region from the Schottky barrier formed at the source extends towards the insulator and reduces the concentration of carriers there. Hence, the current can saturate at a lower V_{DS} from being pinched off at the source rather than in the channel. This results in very distinct output characteristics featuring low saturation voltages and high output impedances similar to the curves shown in Fig. 2(a) [7]. Nevertheless, most of the devices depicted in Fig. 2 do not show pure SGTFT characteristics, which implies that the quality of the TiW-ZnO Schottky junction at the source was inconsistent and the channel conductance still played a major role in the transistor characteristics of our SGTFTs.

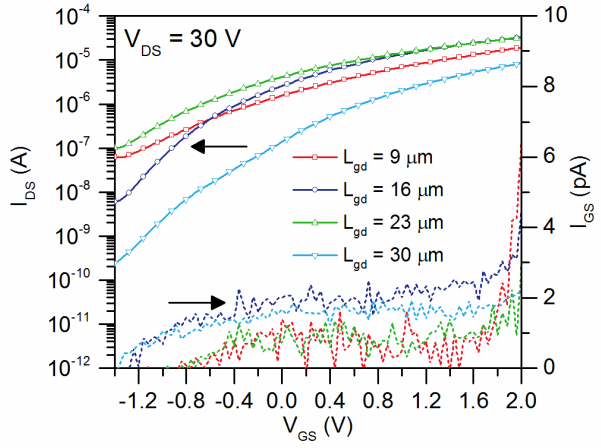

Fig. 3. Left (solid lines + symbols): Transfer characteristics of the ZnO SGTFTs. Right (dashed lines): Gate leakage characteristics of the ZnO SGTFTs.

Fig. 3 displays the transfer (I_{DS} vs gate voltage (V_{GS})) characteristics of the same devices at V_{DS} = 30 V. It can be seen from this figure that the current on-to-off ratios ($I_{on/off}$) of the devices ranged from 10^3 to 10^5. The relative high off current in the devices reduced $I_{on/off}$ and was most likely the result of the ALD ZnO's high residual electron concentrations, which were determined to be on the order of 10^{17} cm^{-3} (using the Hall effect). From the square root of the transfer characteristics at V_{DS} = 30 V, the threshold voltage (V_{th}) and saturation mobility (μ_{sat}) of each device was calculated, and the results are shown in Table I. The V_{th} of all the measured devices was negative, which again is presumably caused by the high doping concentration of the ALD ZnO channel. However, this can be alleviated by reducing the channel thickness [8]. Moreover, if the quality of the TiW Schottky barrier can be improved, then the depletion region from the source potential barrier can also restrict current flow when the device is off [9]. All of the measured devices demonstrated mobilities in the range of 3.5 to 5 $cm^2V^{-1}s^{-1}$, which is also comparable to other

reported TFTs that employed ALD-grown ZnO channels [5], [6].

An ultrathin ZrO_2 film of 5 µm was utilized for the gate insulator layer to improve the charge control in the channel (via larger electric fields compared to thicker films). Consequently, the devices were able to switch at significantly lower V_{GS} values compared to TFTs utilizing conventional gate dielectrics (e.g. SiO_2), which is an important advantage for high performance electronics. This was possible because of the high quality dielectric properties exhibited by the ALD ZrO_2, for instance high capacitance densities [10]. Fig. 3 also shows the gate leakage current (I_{GS}) characteristics of the devices. In the measurement range, all of the devices revealed low leakage currents (< 4 pA) despite the ultrathin ZrO_2. Consequently, we were able to take advantage of a thinner gate dielectric film without considerably large gate leakage currents.

Each device's breakdown voltage (V_{BD}) was determined at zero gate bias by increasing V_{DS} until the current rapidly increases as shown by Fig. 4. The V_{BD} of each device extracted from Fig. 4 is tabulated in Table I. All of the devices exhibit high V_{BD} for their device structure, and thus, are highly promising circuit applications with high drive voltage requirements. The high V_{BD} is most likely due the top gate and drain device structure; from simulation studies, the electric field at the drain edge is reduced compared to the traditional staggered TFT configurations as there is no gate-to-drain overlap. This results in better stability in these top-gated SGTFTs at high V_{DS}.

CONCLUSIONS

We report ALD-grown ZnO SGTFTs utilizing a bottom TiW Schottky barrier source contact and an ultrathin ZrO_2 gate dielectric that demonstrate good transistor characteristics with mobilities as high as 5 $cm^2V^{-1}s^{-1}$. Both the ZnO channel and ZrO_2 gate dielectric were deposited using ALD processes at temperatures less than 130°C. The devices exhibit very low operating voltages associated to the high quality gate oxide. Device breakdown measurements revealed uniquely high breakdown voltages (> 31.8 V) for their dimensions and are promising for future ZnO-based electronics applications.

ACKNOWLEDGEMENTS

The authors would like to thank Natural Science and Engineering Research Council (NSERC) and Alberta Innovates Technology Futures nanoBridge Fund for their support.

TABLE I.
Summary of the ZnO SGTFT properties

L_{GD} (µm)	V_{th} (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{BD} (V)
9	-0.61	3.6	31.8
16	-0.76	4.0	34.6
23	-1.14	3.8	40.5
30	-0.07	5.0	45.7

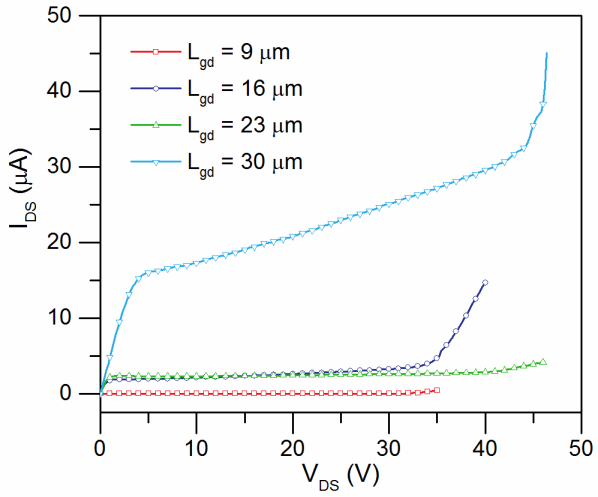

Fig. 4. Breakdown characteristics of the ZnO SGTFTs with varying gate-to-drain spacing at zero gate bias.

REFERENCES

[1] T. Hirao, M. Furuta, T. Hiramatsu, T. Matsuda, C. Li, H. Furuta, H. Hokari, M. Yoshida, H. Ishii, and M. Kakegawa, "Bottom-Gate Zinc Oxide Thin-Film Transistors (ZnO TFTs) for AM-LCDs," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3136–3142, 2008.

[2] B. Bayraktaroglu, K. Leedy, and R. Neidhard, "Microwave ZnO Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1024–1026, 2008.

[3] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: a review of recent advances.," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–86, 2012.

[4] J. Shannon and F. Balon, "Source-gated thin-film transistors," *Solid. State. Electron.*, vol. 52, no. 3, pp. 449–454, 2008.

[5] N. Huby, S. Ferrari, E. Guziewicz, M. Godlewski, and V. Osinniy, "Electrical behavior of zinc oxide layers grown by low temperature atomic layer deposition," *Appl. Phys. Lett.*, vol. 92, no. 2, p. 023502, 2008.

[6] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, and L. M. Irving, "Stable ZnO thin film transistors by fast open air atomic layer deposition," *Appl. Phys. Lett.*, vol. 92, no. 19, p. 192101, 2008.

[7] T. Lindner, G. Paasch, and S. Scheinert, "Simulated operation and properties of source-gated thin-film transistors," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 47–55, 2005.

[8] A. M. Ma, M. Gupta, A. Afshar, G. Shoute, Y. Y. Tsui, K. C. Cadien, and D. W. Barlage, "Schottky barrier source-gated ZnO thin film transistors by low temperature atomic layer deposition," *Appl. Phys. Lett.*, vol. 103, no. 25, p. 253503, 2013.

[9] A. M. Ma, M. Gupta, F. R. Chowdhury, M. Shen, K. Bothe, K. Shankar, Y. Tsui, and D. W. Barlage, "Zinc oxide thin film transistors with Schottky source barriers," *Solid. State. Electron.*, vol. 76, pp. 104–108, 2012.

[10] P. von Hauff, A. Afshar, A. Foroughi-Abari, K. Bothe, K. Cadien, and D. Barlage, "ZrO2 on GaN metal oxide semiconductor capacitors via plasma assisted atomic layer deposition," *Appl. Phys. Lett.*, vol. 102, no. 25, p. 251601, 2013.

ACRONYMS

SGTFT: Source-gated Thin Film Transistor
FPD: Flat Panel Displays
ALD: Atomic Layer Deposition
ZnO: Zinc oxide
ZrO_2: Zirconium oxide
TiW: Titanium tungsten