

Manufacturing Progress for InP-based 500 Gb/s Photonic Integrated Circuits

J. Pleumeekers, E. Strzelecka, K.-P. Yap, A. James, P. Studenkov, P. Debackere, T. Nguyen, S. Agashe, N. Kim, V. Lal, J. Won, C. Hill, Z. Wang, I. Dudley, A. Dentai, Q. Chen, D. Christini, R. Salvatore, D. Lambert, M. Lai, M. Missey, R. Muthiah, J. Rossi, P. Liu, S. Craig, R. Schneider, M. Reffle, F. Kish

Infinera Photonic Integrated Circuit Group, jpleumeekers@infinera.com, +1 408 572 5200
Infinera Corporation, 1322 Bordeaux Drive, Sunnyvale, CA 94089 USA

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Abstract

The status and progress of InP photonic integration is reviewed. Infinera has previously reported on the manufacturing of 100 Gb/s InP-based large-scale photonic integrated circuits. These PICs, based on amplitude modulation and with more than 50 discrete functions per chip, have now reached a high level of manufacturing maturity, and have furthermore redefined reliability standards for InP components, having achieved more than 900 million field hours without a single failure as of this writing.

In this paper, we will describe manufacturing status for the 3rd generation of Infinera's LS-PICs, which feature 500 Gb/s capacity using phase modulation on the transmitter chip, and coherent detection on the receiver chip, and which now form the heart of Infinera's 500G DTN-X transport system, released in mid-2012. These new PICs have an order-of-magnitude increase in chip complexity, and a commensurate increase in fabrication complexity from III-V epitaxy through wafer fab, die fab, and test. The architecture and performance of Infinera's PICs will be described, along with relevant yield and production metrics that demonstrate this platform is at once manufacturable and scalable.

INTRODUCTION

At the 2006 CS-Mantech conference, Infinera reported on the manufacturing and status of their large-scale photonic integrated circuits (LS-PICs) which were the first commercially deployed InP LS-PICs [1]. Those LS-PICs included 10 channels of 10 Gb/s amplitude modulated data for both transmitter (Tx) and receiver (Rx) chips, for a total aggregate data rate of 100 Gb/s. Over 50 different discrete functions were integrated onto a single monolithic InP chip. It was demonstrated that the integration platform was manufacturable and reliable, as well as scalable.

Since then, Infinera has released a second generation of PICs which adds semiconductor optical amplifiers (SOA) to the amplitude modulated transmit PIC, increasing the

integrated device count and complexity to over sixty functions per chip [3].

With the advent of high speed Si ASICs and digital advanced signal processing algorithms in the mid 2000s, efficient high-capacity coherent optical fiber communication became feasible. Various advanced modulation schemes exist but polarization-multiplexed quadrature phase-shift keying (PM-QPSK) quickly became the modulation format of choice due to its balance between spectral efficiency, required optical signal-to-noise ratio (enabling long-haul reach >3000km), and implementation complexity. During the last few years, Infinera has designed and manufactured a new set of LS-PICs to implement the PM-QPSK modulation format into their new telecommunication transport system, DTN-X, released in mid-2012 and supporting 500 Gb/s super-channels [2].

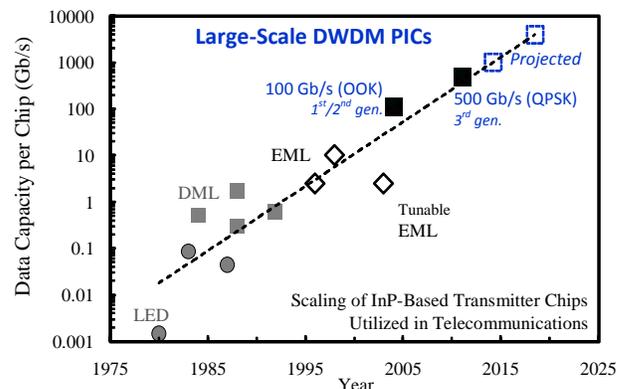


Fig. 1. Scaling of the data capacity / chip for InP-based transmitter chips utilized in optical telecommunications networks. The data capacity per chip has doubled an average of every 2.2 years and is targeted to continue at this rate. The 100 Gb/s PICs are based on on-off-keying (OOK), whereas the 500 Gb/s utilize polarization-multiplexed quadrature phase-shift keying (PM-QPSK).

In this paper we describe the architecture and manufacturing status for these so-called third generation LS-PICs, which feature 500 Gb/s capacity using phase modulation on the transmit chip, and coherent detection on the receive chip. These new PICs have an order of magnitude increase in complexity and integration density, and 5x the data capacity as compared to the first and second generation of LS-PICs (see Fig. 1) and so present significant new design and manufacturing challenges.

ARCHITECTURE OF 500 GB/S TX-PIC

The schematic block diagram of the 500 Gb/s PM-QPSK Transmitter InP chip is shown in Fig. 2. Each monolithically integrated chip contains 10 wavelengths, and each wavelength channel consists of a tunable distributed feedback (DFB) laser, a backside power monitor, a TE/TM-to-be splitter which routes light to a nested pair of Mach-Zehnder modulators (MZMs) in each path, and two arrayed waveguide grating (AWG) multiplexers which separately combine the TE/TM-to-be channels into two output waveguides. The resulting two output signals are then combined off-chip via discrete polarization rotator and polarization beam combiner components.

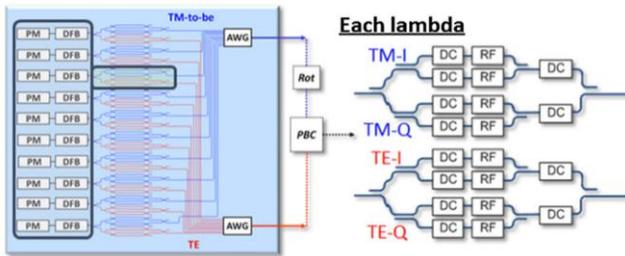


Fig. 2. Schematic block diagram of the 500 Gb/s PM-QPSK Transmitter chip. PM = Power Monitor,

ARCHITECTURE OF 500 GB/S RX-PIC

The schematic block diagram of the 500 Gb/s PM-QPSK Receiver InP chip is shown in Fig. 3. The input block is common to all channels. The TE (H pol) and TM (V pol) signal components are split off-chip using an external polarization beam splitter, and are launched into the TE waveguide mode of the PIC. The ten wavelengths are then separated using a spectral demultiplexer. The individual channels are then routed to processing blocks where they are mixed with local oscillators (LOs) through 90° optical hybrids. The 90° hybrid outputs are terminated in balanced high speed photo detector (HSPD) pairs. The HSPD outputs are wire bonded to a high-speed trans-impedance amplifier (TIA) array off-PIC. The TIA outputs are then sampled using a real-time, high-speed analog-to-digital converter and electronically processed in real time using a DSP ASIC. The

LOs are tunable DFB lasers integrated on the same InP substrate, and are tuned to the incoming signal frequencies. Within a channel, a single LO is split to mix with both the V and H polarizations. The output power of the DFB lasers is monitored on-PIC using the integrated back-PIN Photodiode (BPIN) and controlled by means of a variable optical attenuator (VOA).

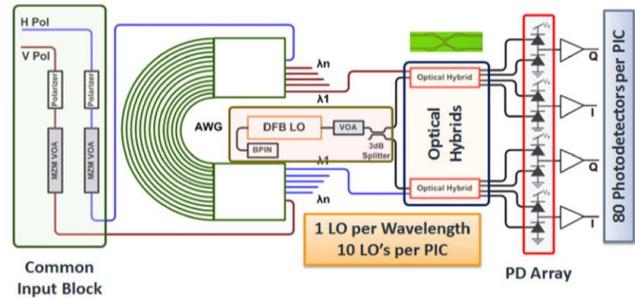


Fig. 3. Schematic block diagram of the 500 Gb/s PM-QPSK Receiver chip.

The PIC receiver chip therefore has 10 DFB LOs, 10 VOAs, 10 BPINs, 10 optical 90° hybrids, 80 high-speed photodiodes, and one AWG demultiplexer. All these devices are monolithically integrated onto a single InP chip.

MANUFACTURING PROCESS AND YIELD MANAGEMENT

As mentioned in the introduction, the manufacturing platform developed for the first generation of amplitude modulated LS-PICs is inherently scalable. The third generation of LS-PICs uses optical phase modulation to encode the data, has substantially more diverse optical functions to be integrated, contains a larger density of device elements on a chip, and employs an increased amount of electrical control and monitor signals. These third generation phase modulated PICs are manufactured side-by-side along with the first and second generation amplitude modulated PICs in the same cleanroom fab with many of the same tools and processes. This is a great benefit of the scalable processes developed early on, and we are confident that the platform will continue to scale as we are moving towards 1 Tb/s PICs and beyond in the next few years.

The primary manufacturing steps to fabricate, test, and package the LS-PICs are shown in Fig. 4. Each step represents a multitude of actual operational steps. This diagram applies to first, second, and third generation PICs. The increased complexity of the third generation of PICs is reflected in the manufacturing process by having increased number of actual operational steps within the Epitaxial, Wafer Fab, Assembly, and Test steps.

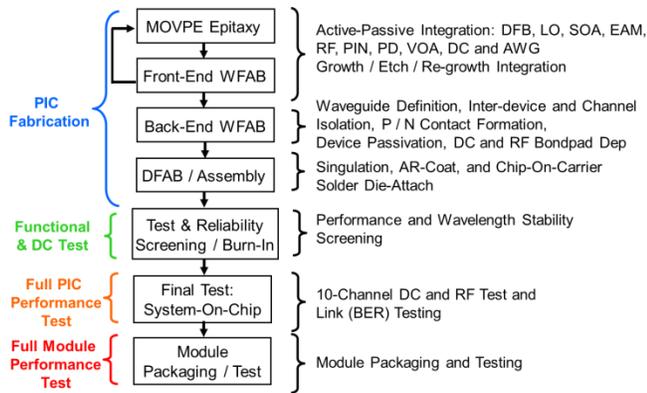


Fig. 4. Main sequence of primary manufacturing steps to fabricate, test, and package the LS-PICs. WFAB = wafer fab, DFAB = die fab.

Yield is a key metric for cost-effective manufacturing, and Infinera has embraced a rigorous yield management and analysis methodology. There are several important differences between InP LS-PIC manufacturing and the Si IC industry. First, the InP manufacturing processes are not as mature as the ones employed in the Si industry. Unlike Si ICs, photonic device integration often requires multiple epitaxial growth and regrowth steps. The InP tool set is less sophisticated, less automated, and less standardized than for Si processing, and the InP wafer size is substantially smaller than for Si wafers. All of these items combined will lead to higher random defect densities in InP LS-PIC manufacturing than for Si ICs. However, this does not necessarily mean that InP manufacturing will suffer from low product yields. There are two differences that play in favor of InP LS-PICs. First, since PICs use optical waveguides for routing the data signals, the inherent occupied critical area density of an InP PIC is significantly lower than for a Si device. Secondly, the optical signal wavelength inside the InP waveguides is roughly 500nm, which means that the minimum killer defect size is significantly higher than for Si devices where the minimum killer defect density size scales with the technology node (currently at 22nm, going to 14nm). These two differences enable realization of high manufacturing product yields for InP LS-PICs, despite the less sophisticated manufacturing processes and higher overall defect density. This is not only vital for successful commercial deployment of InP LS-PICs but is also essential for continued scaling of the devices to accommodate future data rates in excess of 1 Tb/s.

In 2011 we published a multi-year killer defect density reduction trend for the first generation of InP LS-PICs [3] and noted that the extracted killer defect density was similar to that in the Si industry in ~1988, and more importantly that the rate of killer defect density reduction was slightly faster than that in the Si industry during the 1970s. Recently we extracted the killer defect density trend for the third generation 500 Gb/s transmitter LS-PIC over the first 1.5 years of production manufacturing and obtained average random killer defect densities similar to the first generation

of transmit PICs despite the increased manufacturing complexity, and the increased critical area density. More importantly, the rate of killer defect density reduction was also comparable with that obtained for the first generation of LS-PICs. Fig. 5 shows those extracted trends and also shows a data point which represents some of the better yielding 3rd generation PIC wafers, highlighting the defect density capability. This not only demonstrates that the manufacturing platform is scalable to next generation devices, it also ensures that one can expect the defect density reduction to continue over the next few years. This will enable continued scaling of device complexity and density for future generations of LS-PICs while ensuring cost-efficient manufacturing with viable production yields.

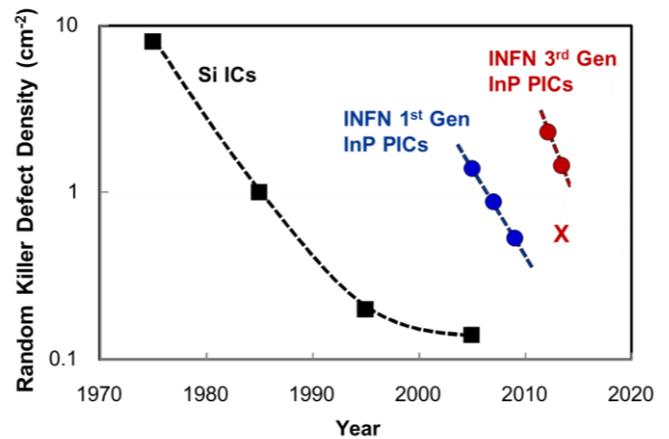


Fig. 5. Average random killer defect density trend for first and third generation LS-PICs, compared to Si IC industry. The red 'x' corresponds with the better yielding 3rd generation PIC wafers and demonstrates the capability and trajectory for ongoing defect density improvements.

PERFORMANCE METRICS AND RELIABILITY

Typical performance metrics for the third generation LS-PICs have already been reported elsewhere [3]-[6]. Here we briefly want to highlight some of the key results.

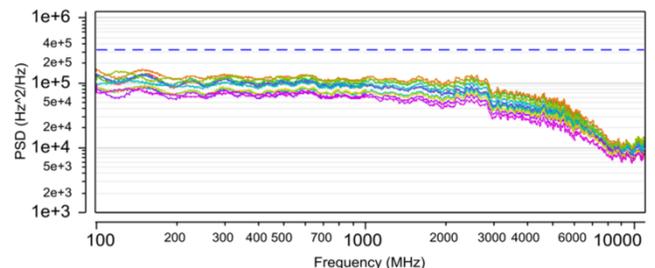


Fig. 6. DFB frequency noise single-sided power spectral density (PSD) spectra for the transmit PIC. The dashed line is a reference to 1 MHz linewidth.

In Fig. 6 the laser frequency noise power spectral density of the transmit PIC is shown. The white noise level between

100 and 3,000 MHz translates into a linewidth of ~ 600 kHz and meets the performance demands of ultra-long haul links. In addition to excellent phase noise characteristics, the laser arrays in the PICs also exhibit high power and side-mode-suppression ratios in excess of 50 dB.

Similarly, for the receive PIC a critical performance parameter is the LO linewidth. In Fig. 7 the distribution of the LO linewidth is shown for a sample of test structures from several different production wafers. A median linewidth of 200 kHz is observed and the linewidth distribution is sufficiently tight to ensure high quality coherent detection of the PM-QPSK data signal.

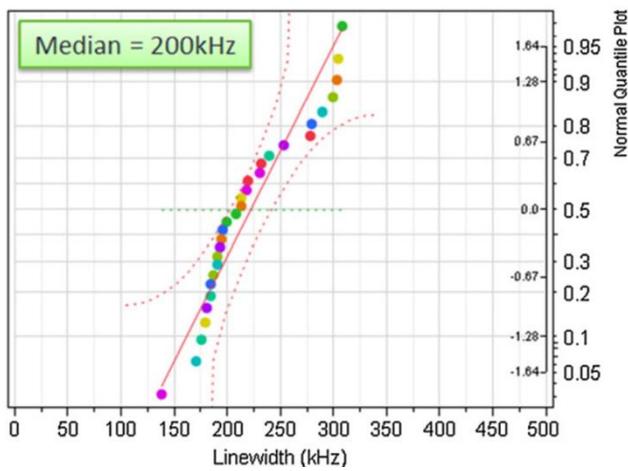


Fig. 7. Local oscillator linewidth distribution for the receive PIC. Samples were taken from test structures over multiple production wafers.

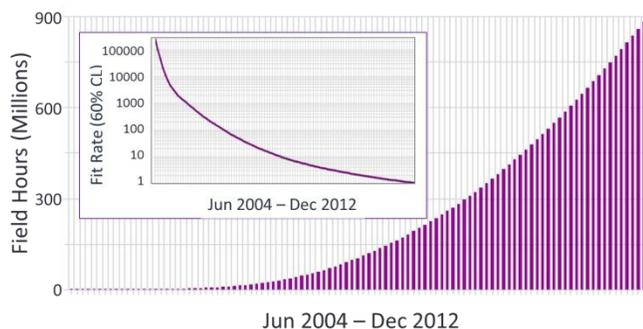


Fig. 8. Reliability performance of first and second generation of LS-PICs. The main plot shows the total number of accumulated field hours over time, and the inset shows the resulting FIT rate over time.

In 2006 we mentioned that the first generation of LS-PICs had passed GR-468 qualification and that zero PIC field failures had occurred in the first year of shipments, which constituted over one million hours of total field hours at that time. Since then over 900 million total field hours have been collected on first and second generation LS-PICs and

still not a single PIC has failed in the field (see Fig. 8). This translates into a FIT (failures in time per billion hours) rate of less than one, which is on-par with or better than the best results reported for single discrete DFB lasers. However, the quoted PIC FIT rate is for the PIC pair which contains over 60 functions. This industry-leading reliability record indicates that the Infinera LS-PIC manufacturing platform is exceptionally capable for meeting the stringent reliability requirements of modern telecommunications networks.

CONCLUSIONS

We have shown that Infinera’s LS-PIC manufacturing platform has been scaled to a third generation of LS-PICs, employing PM-QPSK for a data rate of 500 Gb/s per PIC. Despite the new functionality, higher complexity, and increased critical area density, the platform was able to produce high performing devices able to meet the stringent requirements and specs imposed by the system design. Continued defect reduction has played a key role in achieving viable yields and we are confident that the Infinera platform will continue to scale to our next generation of LS-PICs of 1 Tb/s and beyond.

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